intel®

Silicon Gate MOS 8107B-4

FULLY DECODED RANDOM ACCESS 4096 BIT DYNAMIC MEMORY

* Access Time -- 270 ns max.
* Read, Write Cycle Times -- 470 ns max.
* Refresh Period -- 2 ms

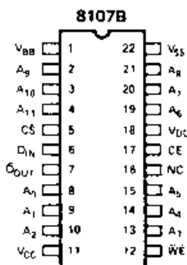
- **Low Cost Per Bit**
- **Low Standby Power**
- **Easy System Interface**
- **Only One High Voltage Input Signal – Chip Enable**
- **TTL Compatible -- All Address, Data, Write Enable, Chip Select Inputs**
- **Read-Modify-Write Cycle Time -- 590 ns**
- **Address Registers Incorporated on the Chip**
- **Simple Memory Expansion – Chip Select Input Lead**
- **Fully Decoded – On Chip Address Decode**
- **Output is Three State and TTL Compatible**
- **Industry Standard 22-Pin Configuration**

The Intel 8107B is a 4096 word by 1 bit dynamic n-channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. The 8107B uses dynamic circuitry which reduces the standby power dissipation.

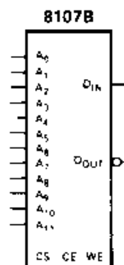
Reading information from the memory is non-destructive. Refreshing is most easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic one or a logic zero.

The 8107B is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than other MOS technologies. The 8107B uses a single transistor cell to achieve high speed and low cost. It is a replacement for the 8107B.

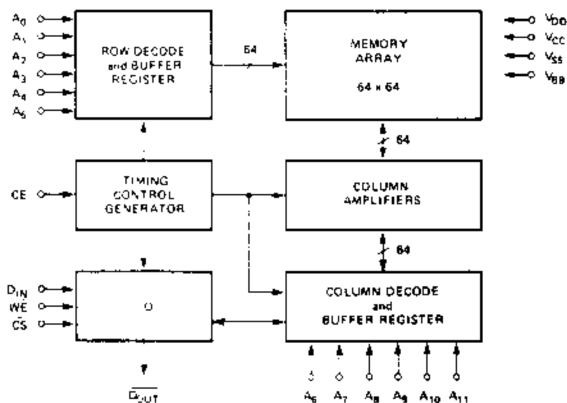
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{11}	ADDRESS INPUTS*	V_{BB}	POWER (-5V)
CE	CHIP ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}$	CHIP SELECT	V_{DD}	POWER (+12V)
D_{IN}	DATA INPUT	V_{SS}	GROUND
$\overline{D_{OUT}}$	DATA OUTPUT	$\overline{WE}$	WRITE ENABLE
NC	NOT CONNECTED		

*Refresh Address A_0-A_5.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . . 0°C to 70°C
Storage Temperature . . . . . . −65°C to +150°C
All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB} . . . . . . +25V to −0.3V
Supply Voltages V_{DD}, V_{CC}, and V_{SS} with Respect to V_{BB} . . . . . . +20V to −0.3V
Power Dissipation 1.25W

**COMMENT:*
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

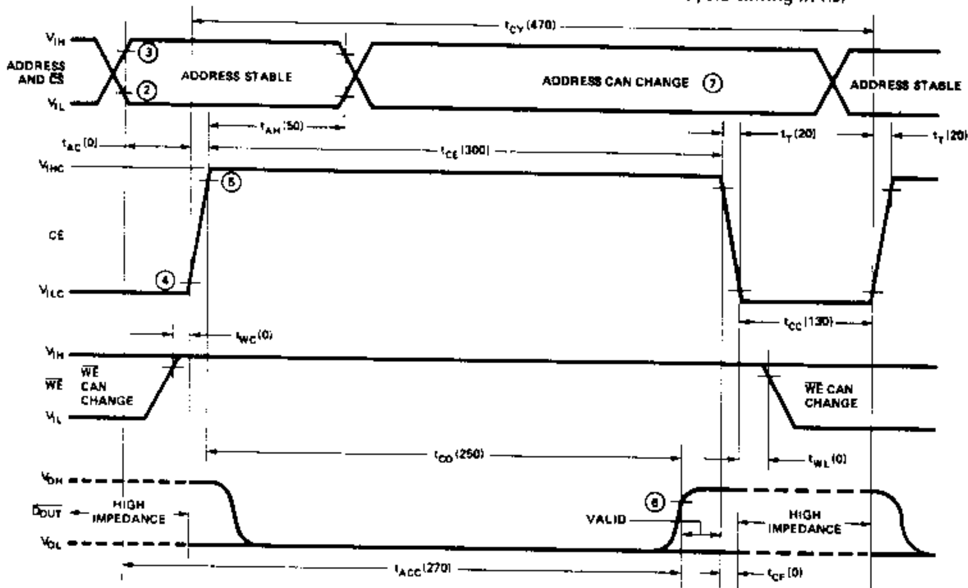
D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB}[1] = -5V ± 5%, V_{SS} = 0V, unless otherwise noted.

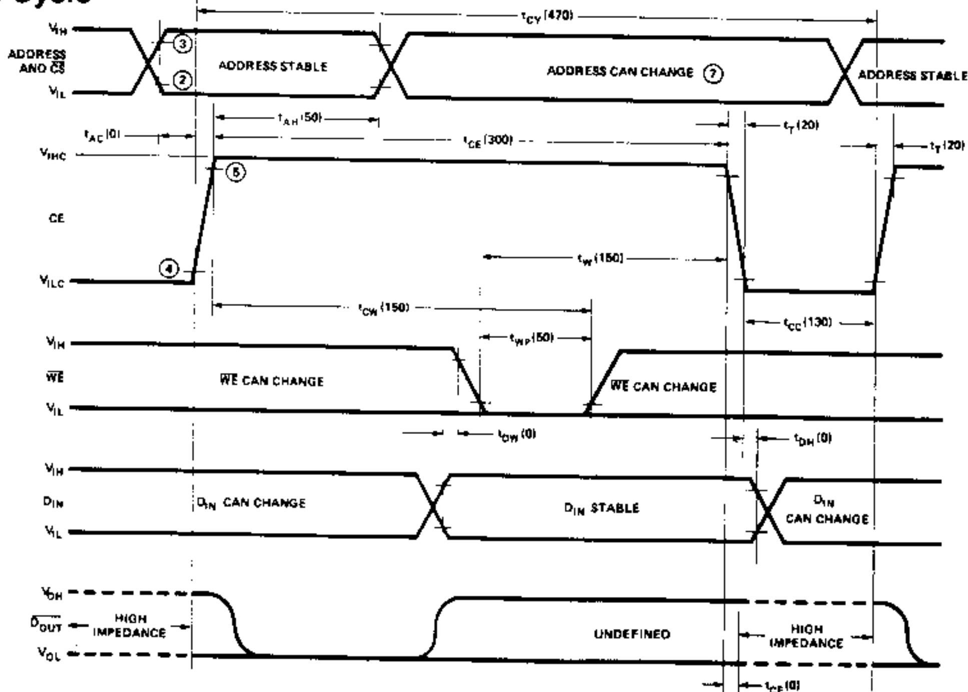
Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)		.01	10	µA	$V_{IN} = V_{IL\,MIN}$ to $V_{IH\,MAX}$
I_{LC}	Input Load Current		.01	10	µA	$V_{IN} = V_{IL\,MIN}$ to $V_{IH\,MAX}$
$\lvert I_{LO}\rvert$	Output Leakage Current for high impedance state		.01	10	µA	CE = V_{ILC} or $\overline{CS} = V_{IH}$; V_O = 0V to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		110	200	µA	CE = −1V to +.6V
I_{DD2}	V_{DD} Supply Current during CE on		80	100	mA	CE = V_{IHC}, T_A = 25°C
$I_{DD\,AV1}$	Average V_{DD} Current		55	80	mA	Cycle time=470ns, t_{CE} = 300ns; T_A = 25°C
$I_{DD\,AV2}$	Average V_{DD} Current		27	40	mA	Cycle time=1000ns, t_{CE} = 300ns; T_A = 25°C
I_{CC1}[4]	V_{CC} Supply Current during CE off		.01	10	µA	CE = V_{ILC} or $\overline{CS} = V_{IH}$
I_{BB}	V_{BB} Supply Current		5	100	µA	
V_{IL}	Input Low Voltage	-1.0		0.6	V	t_T = 20ns — See Figure 4
V_{IH}	Input High Voltage	2.4		V_{CC}+1	V	
V_{ILC}	CE Input Low Voltage	-1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD}−1		V_{DD}+1	V	
V_{OL}	Output Low Voltage	0.0		0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = −2.0mA

NOTES.
1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. During CE on V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

Read and Refresh Cycle [1] (Numbers in parentheses are for minimum cycle timing in ns)



Write Cycle



NOTES:
1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.
7. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 5\%$,

READ, WRITE, AND READ MODIFY/WRITE CYCLE $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		2	ms	
t_{AC}	Address to CE Set Up Time	0		ns	t_{AC} is measured from end of address transition
t_{AH}	Address Hold Time	100		ns	
t_{CC}	CE Off Time	130		ns	
t_T	CE Transition Time	10	40	ns	
t_{CF}	CE Off to Output High Impedance State	0		ns	

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{CY}	Cycle Time	470		ns	$t_T = 20ns$
t_{CE}	CE On Time	300	4000	ns	
t_{CO}	CE Output Delay		250	ns	$C_{load} = 50pF$, Load = One TTL Gate,
t_{ACC}	Address to Output Access		270	ns	Ref = 2.0V,
t_{WL}	CE to $\overline{WE}$	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$
t_{WC}	$\overline{WE}$ to CE on	0		ns	

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{CY}	Cycle Time	470		ns	$t_T = 20ns$
t_{CE}	CE On Time	300	4000	ns	
t_W	$\overline{WE}$ to CE Off	150		ns	
t_{CW}	CE to $\overline{WE}$	150		ns	
t_{DW} [2]	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	50		ns	

Read Modify Write Cycle

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}	Read Modify Write(RMW) Cycle Time	590		ns	$t_T = 20ns$
t_{CRW}	CE Width During RMW	420	4000	ns	
t_{WC}	$\overline{WE}$ to CE on	0		ns	
t_W	$\overline{WE}$ to CE off	150		ns	$C_{load} = 50pF$, Load = One TTL Gate,
t_{WP}	$\overline{WE}$ Pulse Width	50		ns	Ref = 2.0V
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{CO}	CE to Output Delay		250	ns	
t_{ACC}	Access Time		270	ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$

Typical Characteristics

Fig. 1. I_{DD} AV VS. TEMPERATURE

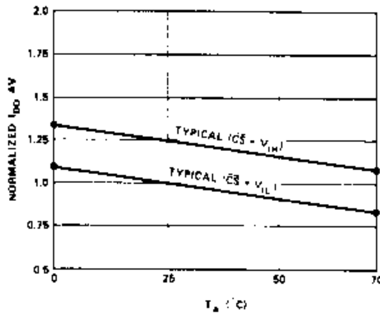


Fig. 2. TYPICAL I_{DD} AVERAGE VS. CYCLE TIME

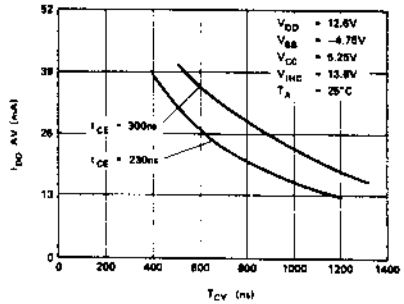


Fig. 3. I_{DD2} VS. TEMPERATURE

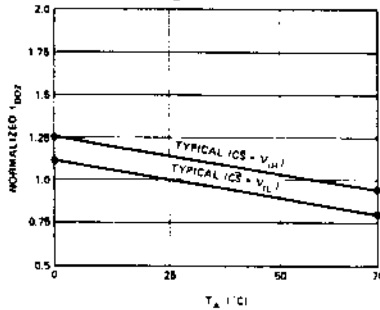


Fig. 4. TYPICAL V_{IL} MAX VS. CE RISE TIME

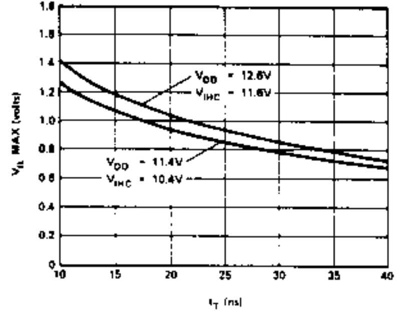


Fig. 5. TYPICAL I_{OH} VS. V_{OH}

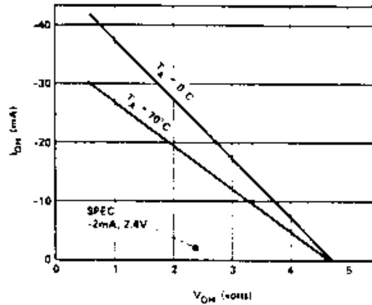


Fig. 6. TYPICAL I_{OL} VS. V_{OL}

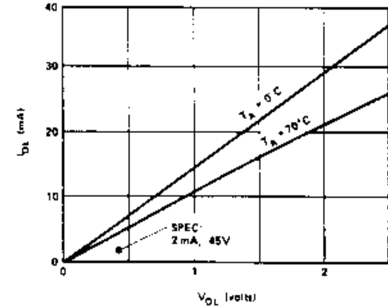


Fig. 7. TYPICAL REFRESH VS. TEMPERATURE

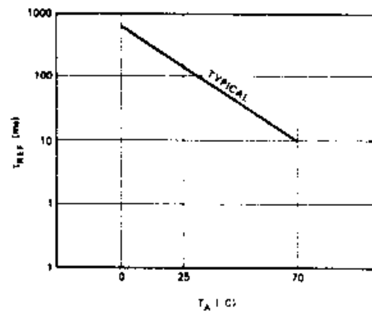
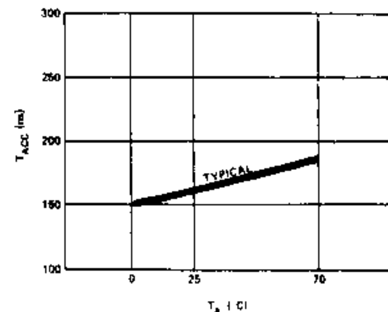


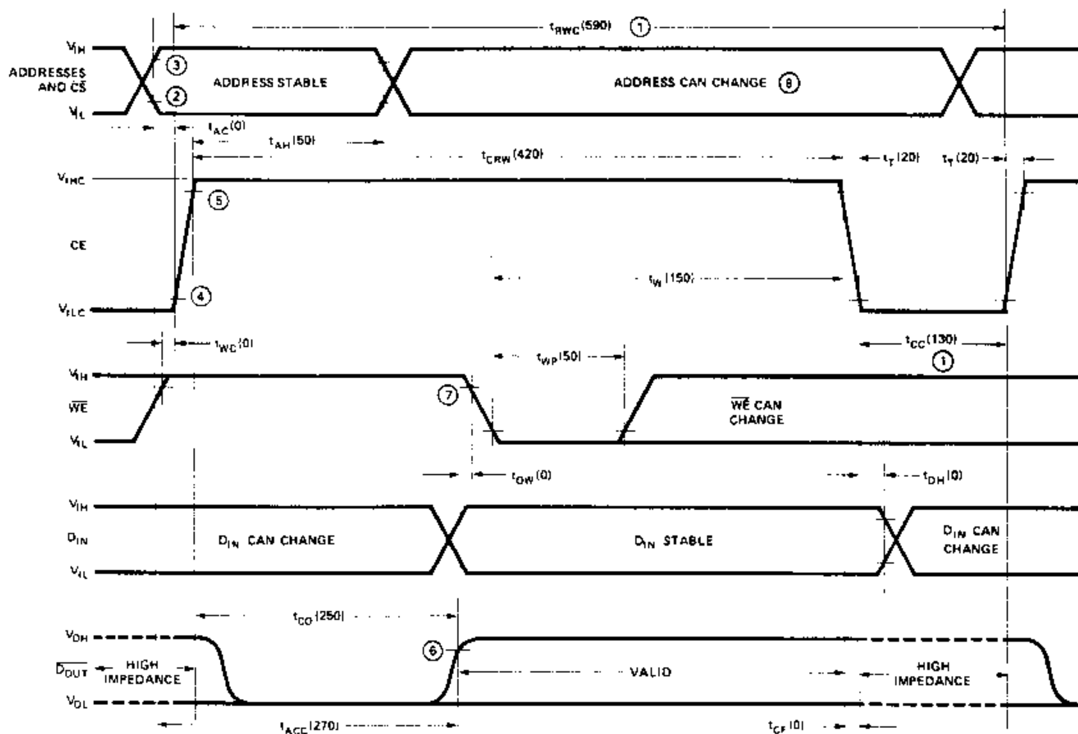
Fig. 8. TYPICAL ACCESS TIME VS. TEMPERATURE



Read Modify Write Cycle [1]

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}	Read Modify Write(RMW) Cycle Time	590		ns	t_T = 20ns
t_{CRW}	CE Width During RMW	420	3000	ns	
t_{WC}	$\overline{WE}$ to CE on	0		ns	
t_W	$\overline{WE}$ to CE off	150		ns	C_{load} = 50pF, Load = One TTL Gate, Ref = 2.0V
t_{WP}	$\overline{WE}$ Pulse Width	50		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{CO}	CE to Output Delay		250	ns	
t_{ACC}	Access Time		270	ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$

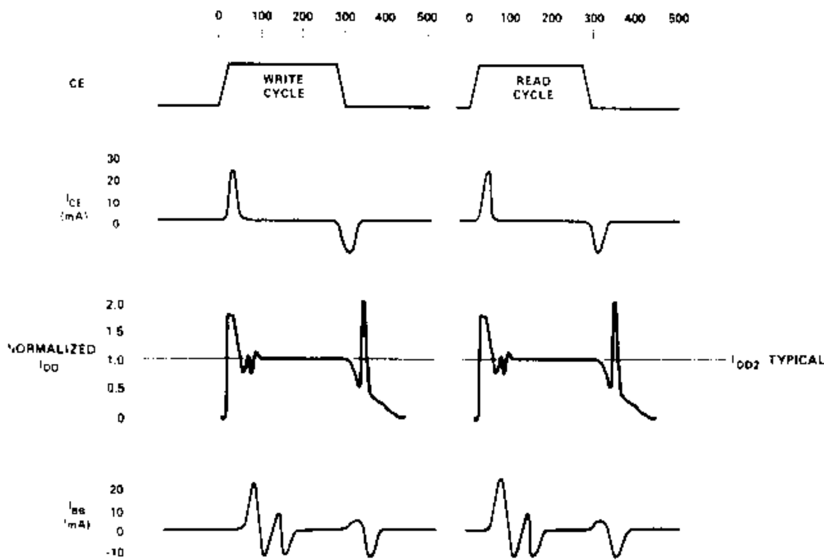
(Numbers in parentheses are for minimum cycle timing in ns.)



NOTES:

1. A.C. characteristics are guaranteed only if cumulative CE on time during t_{REF} is $\leq$65% of t_{REF}. For continuous Read-Modify-Write operation, t_{CC} and t_{RWC} should be increased to at least 185ns and 645ns, respectively.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} −2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.
7. $\overline{WE}$ must be at V_{IH} until end of t_{CO}.
8. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

Typical Current Transients vs. Time



Applications

Refresh

The 8107B-4 is refreshed by either a read cycle, write cycle, or read-modify write cycle. Only the selected row of memory array is refreshed. The row address is selected by the input signals A_0 thru A_5. Each individual row address must receive at least one refresh cycle within any two milliseconds time period.

If a read cycle is used for refreshing, then the chip select input, $\overline{CS}$, can be a logic high or a logic low. If a write cycle or read-modify write cycle is used to refresh the device, then $\overline{CS}$ must be a logic high. This will prevent writing into the memory during refresh.

Power Dissipation

The operating power dissipation of a selected device is the sum of V_{DD} x I_{DDAV} and V_{BB} x I_{BB}. For a cycle of 400ns and t_{CE} of 230ns typical power dissipation is 456mW.

Standby Power

The 8107B-4 is a dynamic RAM therefore when $V_{CE} = V_{ILC}$ very little power is dissipated. In a typical system most devices are in standby with V_{CE} at V_{ILC}. During this time only leakage currents flow (i.e., I_{DD1}, I_{CC1}, I_{BB}, I_{LO}, I_{L1}). The power dissipated during this inactive period is typically 1.4mW. The typical power dissipation required to perform refresh during standby is the refresh duty cycle, 1.3%, multiplied by the operating power dissipation, or 5.9mW. The total power dissipation during standby is then 7.3mW typical.

System Interfaces and Filtering

On the following page is an example of a 16K x 8 bit memory system. Device decoding is done with the CE input. All devices are unselected during refresh with CS. It is recommended that 1μF high frequency, low inductance capacitors be used on double sided boards. V_{CC} to V_{SS} decoupling is required only on the devices located around the periphery of the array. For each 36 devices a 100μF tantalum or equivalent capacitor should be placed from V_{DD} to V_{SS} close to the array.

Typical System

Below is an example of a 16K × 8 bit memory circuit. Device decoding is done with the CE input. All devices are unselected during refresh with CS input. The 8210, 8205 and 8212 are standard Intel products.