

## 1024 x 4 Static Random Access Memory

### Features

- 45 ns Maximum Access Time
- No Clocks or Strobes Required
- Automatic  $\overline{CE}$  Power Down
- Identical Cycle and Access Times
- Single +5V Supply ( $\pm 10\%$ )
- Pinout and Function Compatible to SY2148
- Performance Upgrade for SY2148
- Industry Standard 2114 Pinout
- Totally TTL Compatible All Inputs and Outputs
- Common Data Input and Output
- High Density 18-Pin Package
- Three-State Output

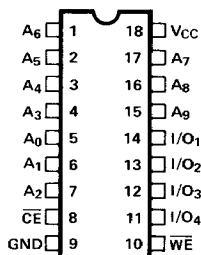
### Description

The Synertek SY2148H is a 4096-Bit Static Random Access Memory organized 1024 words by 4 bits and is fabricated using Synertek's new scaled n-channel silicon gate technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Common data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

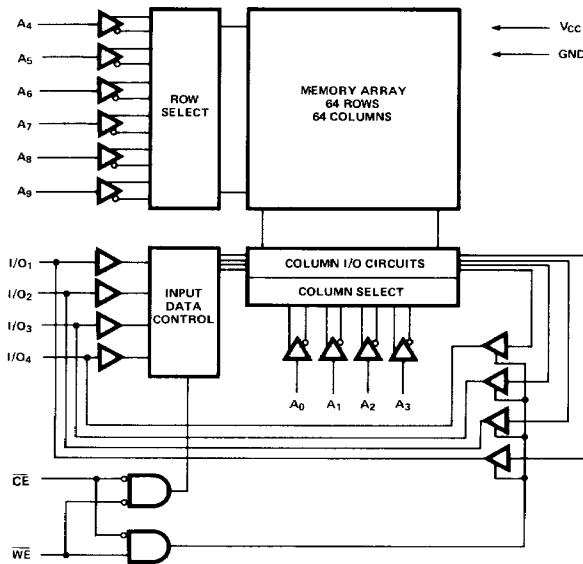
The SY2148H offers an automatic power down feature. Power down is controlled by the Chip Enable input. When Chip Enable ( $\overline{CE}$ ) goes high, thus deselecting the SY2148H, the device will automatically power down and remain in a standby power mode as long as  $\overline{CE}$  remains high. This unique feature provides system level power savings as much as 85%.

The SY2148H is packaged in an 18-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

### Pin Configuration



### Block Diagram



MEMORIES

**Absolute Maximum Ratings\***

Temperature Under Bias . . . . . -10°C to 85°C  
 Storage Temperature . . . . . -65°C to 150°C  
 Voltage on Any Pin with  
 Respect to Ground . . . . . -3.5V to +7V  
 Power Dissipation . . . . . 1.0W  
 Electrostatic Discharge Rating (ESD)\*\*  
 Inputs to Ground . . . . . ±2000V

**Comment\***

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

\*\*Test Condition: MIL-STD-883B Method 3015.1

**D.C. Characteristics**

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$  (Unless otherwise specified) (note 8)

Symbol	Parameter	2148H/H-2/H-3		2148HL/HL-3		Unit	Conditions	
		Min.	Max.	Min.	Max.			
$I_{LI}$	Input Load Current (All input pins)		10		10	$\mu\text{A}$	$V_{CC} = \text{Max}$ , $V_{IN} = \text{Gnd to } V_{CC}$	
$ I_{LO} $	Output Leakage Current		50		50	$\mu\text{A}$	$\overline{CE} = V_{IH}$ , $V_{CC} = \text{Max}$ $V_{OUT} = \text{Gnd to } 4.5\text{V}$	
$I_{CC}$	Power Supply Current		140		115	mA	$T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$	$V_{CC} = \text{Max}$ , $\overline{CE} = V_{IL}$ Outputs Open
			150		125			
$I_{SB}$	Standby Current		30		20	mA	$V_{CC} = \text{Min to Max}$ , $\overline{CE} = V_{IH}$	
$I_{PO}$	Peak Power-on Current (Note 9)		50		30	mA	$V_{CC} = \text{Gnd to } V_{CC} \text{ Min}$ $\overline{CE} = \text{Lower of } V_{CC} \text{ or } V_{IH} \text{ Min}$	
$V_{IL}$	Input Low Voltage	-3.0	0.8	-3.0	0.8	V		
$V_{IH}$	Input High Voltage	2.0	6.0	2.0	6.0	V		
$V_{OL}$	Output Low Voltage		0.4		0.4	V	$I_{OL} = 8\text{mA}$	
$V_{OH}$	Output High Voltage	2.4		2.4		V	$I_{OH} = -4\text{mA}$	

**Capacitance**

$T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$

Symbol	Test	Typ.	Max.	Unit
$C_{OUT}$	Output Capacitance		7	pF
$C_{IN}$	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested.

**A.C. Characteristics**

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$  (Unless otherwise specified) (note 8)

**READ CYCLE**

Symbol	Parameter	2148H-2		2148H-3/HL-3		2148H/HL		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{RC}$	Read Cycle Time	45		55		70		ns	
$t_{AA}$	Address Access Time		45		55		70	ns	
$t_{ACE1}$	Chip Enable Access Time		45		55		70	ns	Note 1
$t_{ACE2}$	Chip Enable Access time		55		65		80	ns	Note 2
$t_{OH}$	Output Hold from Address Change	5		5		5		ns	
$t_{LZ}$	Chip Selection to Output in Low Z	10		10		10		ns	Note 7
$t_{HZ}$	Chip Deselection to Output in High Z	0	20	0	20	0	20	ns	Note 7
$t_{PU}$	Chip Selection to Power Up Time	0		0		0		ns	
$t_{PD}$	Chip Deselection to Power Down Time		30		30		30	ns	

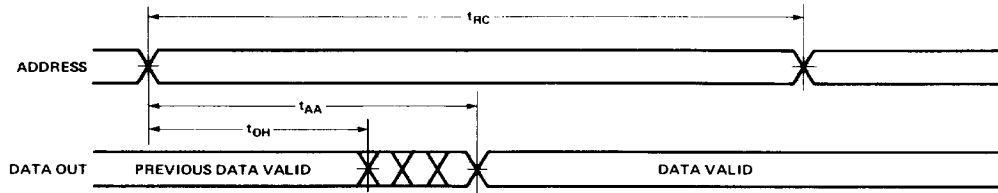
**WRITE CYCLE**

$t_{WC}$	Write Cycle Time	45		55		70		ns	
$t_{CW}$	Chip Enabled to End of Write	40		50		65		ns	
$t_{AW}$	Address Valid to End of Write	40		50		65		ns	
$t_{AS}$	Address Setup Time	0		0		0		ns	
$t_{WP}$	Write Pulse Width	35		40		50		ns	
$t_{WR}$	Write Recovery Time	5		5		5		ns	
$t_{DW}$	Data Valid to End of Write	20		20		25		ns	
$t_{DH}$	Data Hold Time	0		0		0		ns	
$t_{WZ}$	Write Enabled to Output in High Z	0	15	0	20	0	25	ns	Note 7
$t_{OW}$	Output Active from End of Write	0		0		0		ns	Note 7

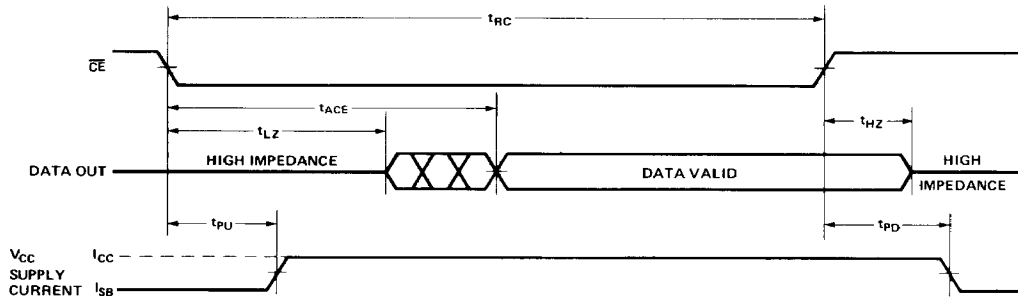
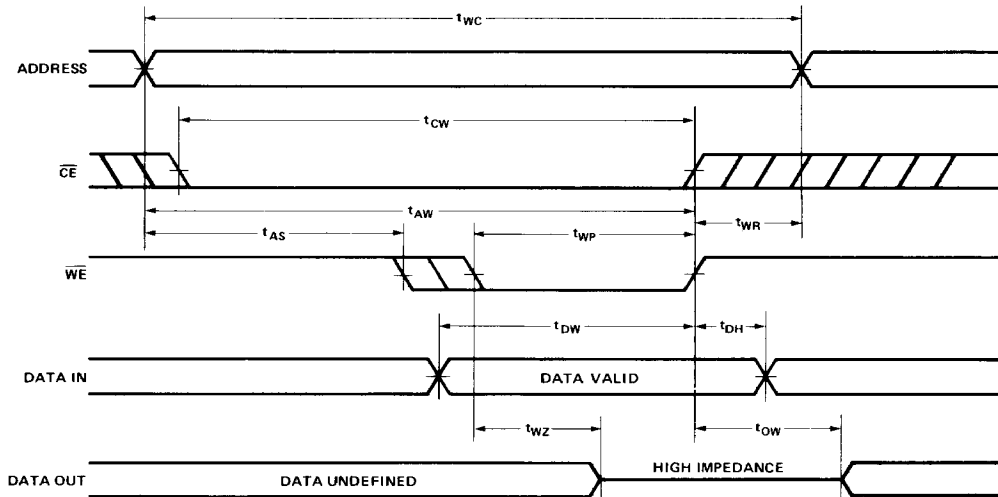
(See following page for notes)

## Timing Diagrams

## READ CYCLE NO. 1 (NOTES 3 AND 4)



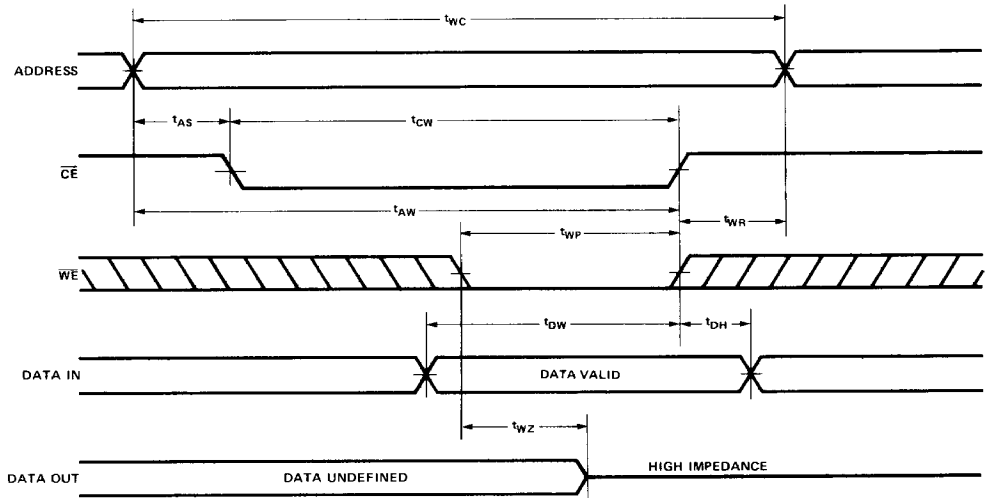
## READ CYCLE NO. 2 (NOTES 3 AND 5)

WRITE CYCLE NO. 1 ( $\overline{WE}$  CONTROLLED) (NOTE 6)

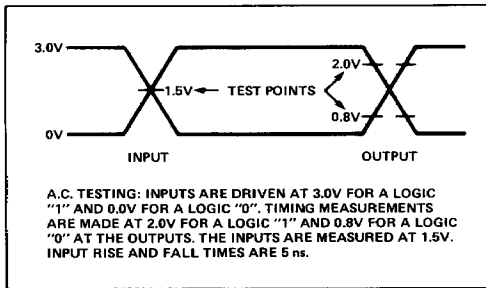
## NOTES:

1. Chip deselected for greater than 55ns prior to selection.
2. Chip deselected for a finite time that is less than 55ns prior to selection. (If the deselect time is 0ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)
3.  $\overline{WE}$  is high for Read Cycles.
4. Device is continuously selected,  $\overline{CE} = V_{IL}$ .
5. Addresses valid prior to or coincident with  $\overline{CE}$  transition low.
6. If  $\overline{CE}$  goes high simultaneously with  $\overline{WE}$  high, the outputs remain in the high impedance state.
7. Transition is measured  $\pm 500mV$  from low or high impedance voltage with load B. This parameter is sampled and not 100% tested.
8. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
9. A pullup resistor to  $V_{CC}$  on the  $\overline{CE}$  input is required to keep the device deselected; otherwise, power-on current approaches  $I_{CC}$  active.
10. A minimum 0.5 ms time delay is required after application of  $V_{CC}$  (+5V) before proper device operation is achieved.

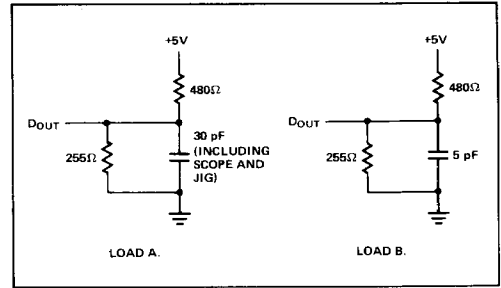
WRITE CYCLE NO. 2 ( $\overline{CE}$  CONTROLLED) (NOTE 6)



A.C. Testing Input, Output Waveform



A.C. Testing Load Circuit



Package Availability 18 Pin Ceramic  
18 Pin Cerdip  
18 Pin Plastic

Ordering Information

Order Number	Access Time (Max)	Operating Current (Max)	Standby Current (Max)	*Package Type
SYC2148H	70ns	150mA	30mA	Ceramic
SYD2148H	70ns	150mA	30mA	Cerdip
SYC2148H-2	45ns	150mA	30mA	Ceramic
SYD2148H-2	45ns	150mA	30mA	Cerdip
SYC2148H-3	55ns	150mA	30mA	Ceramic
SYD2148H-3	55ns	150mA	30mA	Cerdip
SYC2148HL	70ns	125mA	20mA	Ceramic
SYD2148HL	70ns	125mA	20mA	Cerdip
SYC2148HL-3	55ns	125mA	20mA	Ceramic
SYD2148HL-3	55ns	125mA	20mA	Cerdip

\*Also available in plastic