M27C128
128K (16K x 8) CHMOS PRODUCTION AND UV ERASABLE PROMs

- **CHMOS Microcontroller and Microprocessor Compatible**
- **Low Power Consumption**
  - **100 μA Maximum Standby Current (CMOS)**
- **Maximum Latch-Up Immunity Through EPI Processing**
  - **± 1V Input Protection**
  - **14V V_{PP} Protection**
- **CHMOS II-E* Technology**
- **Fast Programming**
  - **int$_e$ligent Programming™ Algorithm**
  - **Quick-Pulse Programming™ Algorithm**
- **int$_e$ligent Identifier™ Mode**
  - **Automated Programming Operations**
- **Compatible with M2732A, M27C64A, M27C256**
- **Available in 28-Pin Cerdip Package**
  (See Packaging Spec. Order #231369)

Intel's M27C128 CHMOS EPROM is a 128 K-bit, 5V-only memory, organized as 16,384 words of 8 bits each. The M27C128 is ideal for systems requiring low power, high performance, and noise immunity due to its CHMOS *II-E processing, and it is pin compatible with the HMOS Intel M27128A.

Several advanced features have been designed into the M27C128 that allows fast and reliable programming —the int$_e$ligent Programming Algorithm and the int$_e$ligent Identifier Mode. Programming equipment that takes advantage of these innovations will electronically identify the M27C128 and then rapidly program it using an efficient programming method. The M27C128 can also be programmed using the Quick-Pulse™ Programming Algorithm.

Intel's unique EPI processing provides excellent latch-up immunity. Prevention of latch-up is guaranteed for stresses up to 100 mA on address and data pins from $-1V$ to $V_{CC} + 1V$ and for V_{PP} voltage overshoot up to 14V.

*HMOS and CHMOS are patented processes of Intel Corporation.

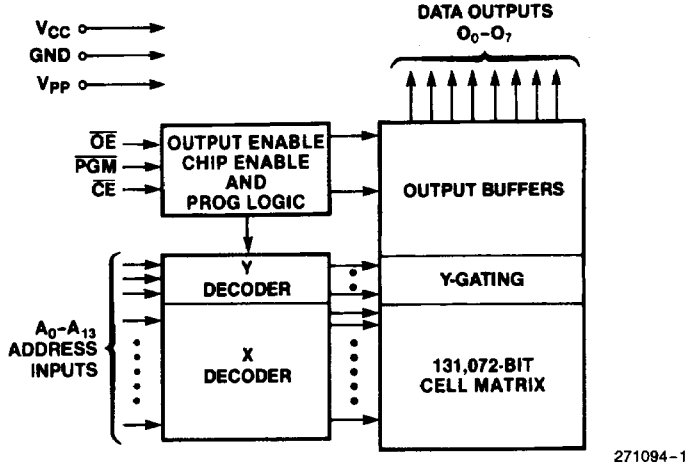

Figure 1. Block Diagram

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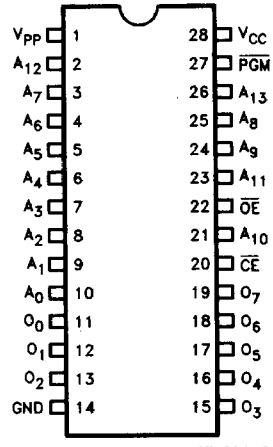
February 1991
Order Number: 271094-002

Pin Names

A_0–A_{13}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
N.C.	No Internal Connect
D.U.	Don't Use

M27C256	M27C64A	M2732A
V_{PP}	V_{PP}	
A_{12}	A_{12}	
A_7	A_7	A_7
A_6	A_6	A_6
A_5	A_5	A_5
A_4	A_4	A_4
A_3	A_3	A_3
A_2	A_2	A_2
A_1	A_1	A_1
A_0	A_0	A_0
O_0	O_0	O_0
O_1	O_1	O_1
O_2	O_2	O_2
Gnd	Gnd	Gnd

M27C128



271094-2

M2732A	M27C64A	M27C256
	V_{CC}	V_{CC}
	$\overline{PGM}$	A_{14}
V_{CC}	N.C.	A_{13}
A_8	A_8	A_8
A_9	A_9	A_9
A_{11}	A_{11}	A_{11}
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7
O_6	O_6	O_6
O_5	O_5	O_5
O_4	O_4	O_4
O_3	O_3	O_3

NOTE:
Intel "Universal Site"-Compatible EPROM Pin Configurations are Shown in the Blocks Adjacent to the M27C128 Pins.

Figure 2. Cerdip(D) Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Case Temperature under Bias ..... −55°C to +125°C

Storage Temperature ..... −65°C to +150°C

Voltage on Any Pin with Respect to Ground ..... −2.0V to +7V(1)

Voltage on Pin A_9 with Respect to Ground ..... −2.0V to +13.5V(1)

V_{PP} Supply Voltage with Respect to Ground During Programming ..... −2.0V to +14V(1)

V_{CC} Supply Voltage with Respect to Ground ..... −2.0V to 7.0V(1)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION D.C. CHARACTERISTICS

$-55°C \le T_C^{(8)} \le +125°C$ and $V_{CC} = 5V \pm 10\%$

Symbol	Parameter		Notes	Min	Typ(2)	Max	Unit	Test Condition
I_{LI}	Input Leakage Current				0.01	1.0	µA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current					±10	µA	V_{OUT} = 0V to 5.5V
I_{PP_1}	V_{PP} Current Read		5			100	µA	$V_{PP} = V_{CC}$
I_{SB}	V_{CC} Current Standby with Inputs—	CMOS	4			100	µA	$\overline{CE} = V_{IH}$
		TTL	3			1.0	mA	
I_{CC1}	V_{CC} Current Active		5			25	mA	$\overline{CE} = V_{IL}$, f = 5 MHz, I_{OUT} = 0 mA
V_{IL}	Input Low Voltage (±10% Supply) (TTL)			−0.5		0.8	V	$V_{PP} = V_{CC}$
	Input Low Voltage (CMOS)			−0.2		0.2		
V_{IH}	Input High Voltage (±10% Supply) (TTL)			2.0		V_{CC} + 0.5	V	$V_{PP} = V_{CC}$
	Input High Voltage (CMOS)			V_{CC} −0.2		V_{CC} + 0.2		
V_{OL}	Output Low Voltage					0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage			3.5			V	I_{OH} = −2.5 mA
I_{OS}	Output Short Circuit Current		6			100	mA	
V_{PP}	V_{PP} Read Voltage		7	V_{CC} − 0.7		V_{CC}	V	

NOTES:

1. Minimum D.C. input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. Voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.
2. Typical limits are at V_{CC} = 5V, T_C = +25°C.
3. V_{IL}, V_{IH} levels at TTL inputs.
4. $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within spec.
5. Maximum Active power usage is the sum I_{PP} + I_{CC}. The maximum current value is with Outputs O_0 to O_7 unloaded.
6. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
7. V_{PP} may be one diode voltage drop below V_{CC}. It may be connected directly to V_{CC}.
8. Case temperatures are "instant on".

7

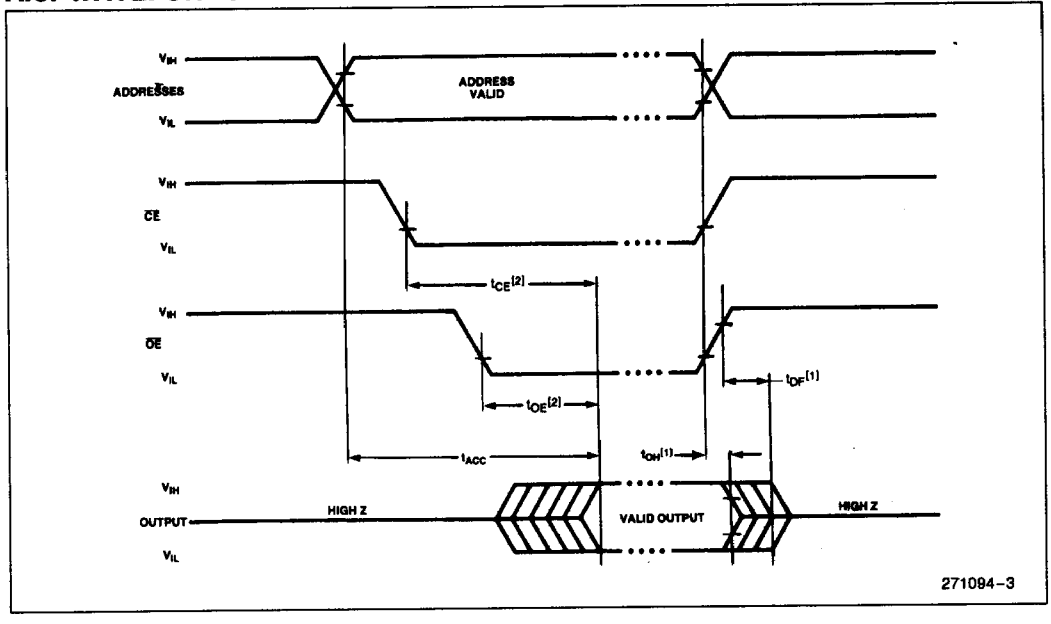
READ OPERATION

A.C. CHARACTERISTICS $-55°C \leq T_C \leq +125°C$

Versions		M27C128-20		M27C128-30		Unit
Symbol	Characteristic	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		300	ns
t_{CE}	$\overline{CE}$ to Output Delay		200		300	ns
t_{OE}	$\overline{OE}$ to Output Delay		75		100	ns
t_{DF}(2)	$\overline{OE}$ High to Output High Z		55		60	ns
t_{OH}(2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First	0		0		ns

NOTES:
1. A.C. characteristics tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$.
   Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed and sampled.

A.C. WAVEFORMS



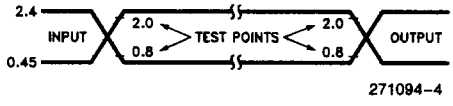
NOTES:
1. This parameter is only sampled and is not 100% tested.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

CAPACITANCE[1] T_C = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Address/Control Capacitance	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	12	pF	V_{OUT} = 0V

NOTE:
1. Sampled. Not 100% tested.

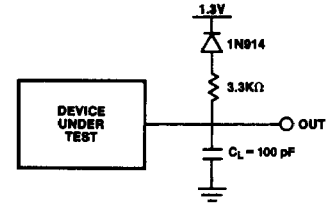
A.C. TESTING INPUT/OUTPUT WAVEFORM



271094-4

A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT



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C_L = 100 pF
C_L includes Jig Capacitance

DEVICE OPERATION

The modes of operation of the M27C128 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for int$_e$ligent Identifier mode.

Table 1. Mode Selection for M27C128

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	X[1]	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	(4)	(4)	D_{OUT}
Program Inhibit	V_{IH}	X	X	X	X	(4)	(4)	High Z
int$_e$ligent Identifier[3] -Manufacturer	V_{IL}	V_{IL}	V_{IH}	V_H[2]	V_{IL}	V_{CC}	V_{CC}	89 H
int$_e$ligent Identifier[3] Device	V_{IL}	V_{IL}	V_{IH}	V_H[2]	V_{IH}	V_{CC}	V_{CC}	FC H
int$_e$ligent Programming	V_{IL}	V_{IH}	V_{IL}	X	X	(4)	(4)	DIN

NOTES:
1. X can be V_{IL} or V_{IH}.
2. V_H = 12.0V ± 0.5V.
3. A_1–A_8, A_{10}–A_{13} = V_{IL}.
4. See Table 2 for V_{CC} and V_{PP} voltages.

7

READ MODE

The M27C128 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient and inductive current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low and $\overline{OE}$ = V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other devices from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{PGM}$ input with V_{PP} at its programming voltage and $\overline{CE}$ = V_{IL} will program the selected device.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{CC} and V_{PP} at their programming voltages. Data should be verified a minimum of t_{OE} after the falling edge of $\overline{OE}$.

inteligent Identifier™ Mode

The inteligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the inteligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

inteligent Programming™ Algorithm

The M27C128 inteligent Programming Algorithm rapidly programs Intel M27C128 using an efficient and reliable method particularly suited to the production programming environment. Typical programming time for individual devices is less than one and a half minutes. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flow-chart of the M27C128 inteligent Programming Algorithm is shown in Figure 3.

The inteligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{CE}$ pulse(s) is 1 ms, which will then be followed by a longer overprogram pulse of length 3X ms. X is an iteration counter and is equal to the number of the initial 1 ms pulses applied to a particular M27C128 location, before a correct verify occurs. Up to 25 1-ms pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V nominal. When the inteligent Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

The M27C128 can also be programmed using the Quick Pulse Programming Algorithm.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 400 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

HIGH RELIABILITY CHMOS

Special EPI processing techniques have enabled Intel to build CHMOS with features adding to system reliability. These include input/output protection to latch-up. Each of the data and address pins will not latch-up with currents up to 100 mA and voltages from −1V to V_{CC} + 1V.

Additionally, the V_{PP} (programming) pin is designed to resist latch-up to the 14V maximum device limit.

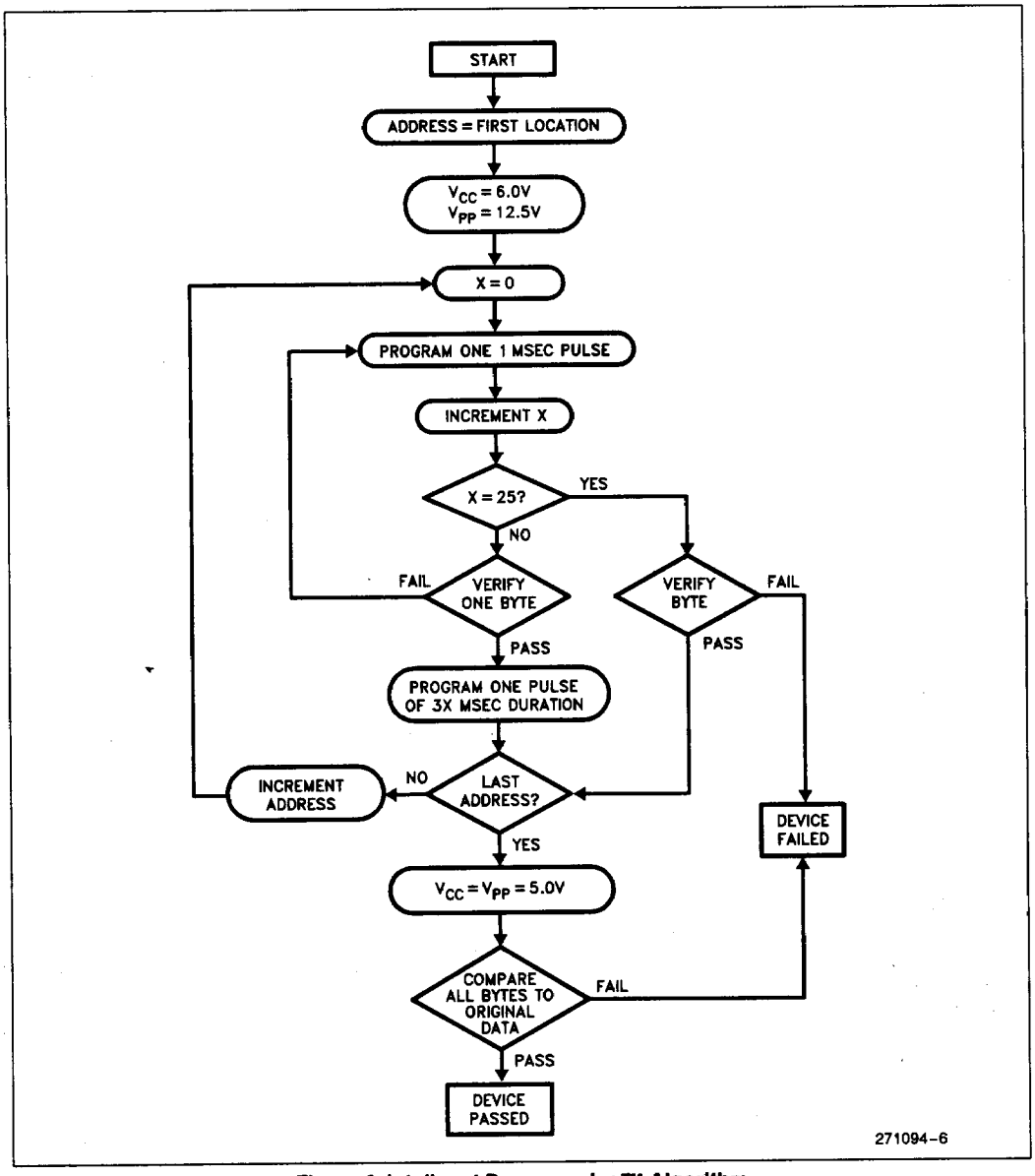


Figure 3. Intelligent Programming™ Algorithm

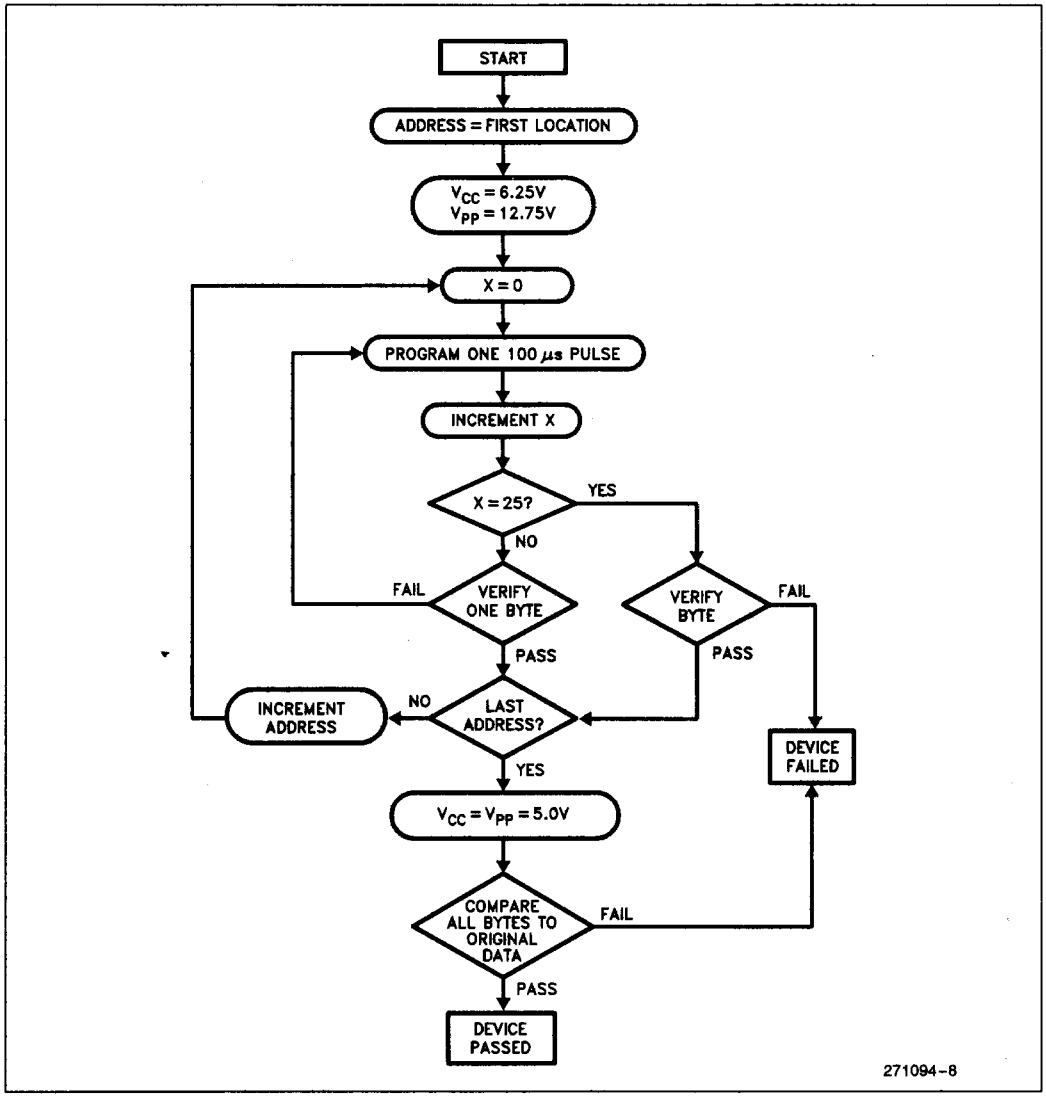


Figure 4. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm

Intel's M27C128 EPROM is programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 µs pulses per byte are provided before a failure is recognized. A flow chart of the Quick-Pulse Programming Algorithm is shown in Figure 4.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V (nominal). When programming of the EPROM has been completed, all bytes should be compared to the original data with V_{CC} = 5.0V ($V_{PP} \leq V_{CC}$).

7

D.C. PROGRAMMING CHARACTERISTICS T_C = 25°C ±5°C

Table 2

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		1.0	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High level	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	2.4		V	I_{OH} = −400 μA
I_{CC2}(3)	V_{CC} Supply Current		25	mA	
I_{PP2}(3)	V_{PP} Supply Current (Program)		30	mA	$\overline{CE} = V_{IL}$
V_{ID}	A9 intelligent Identifier Voltage	11.5	12.5	V	
V_{PP}	intelligent Programming Algorithm	12.0	13.0	V	$\overline{CE} = \overline{PGM} = V_{IL}$
	Quick-Pulse Programming Algorithm	12.5	13.0	V	
V_{CC}	intelligent Programming Algorithm	5.75	6.25	V	
	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

T_C = 25°C ±5°C, See Table 2 for V_{CC} and V_{PP} Voltages

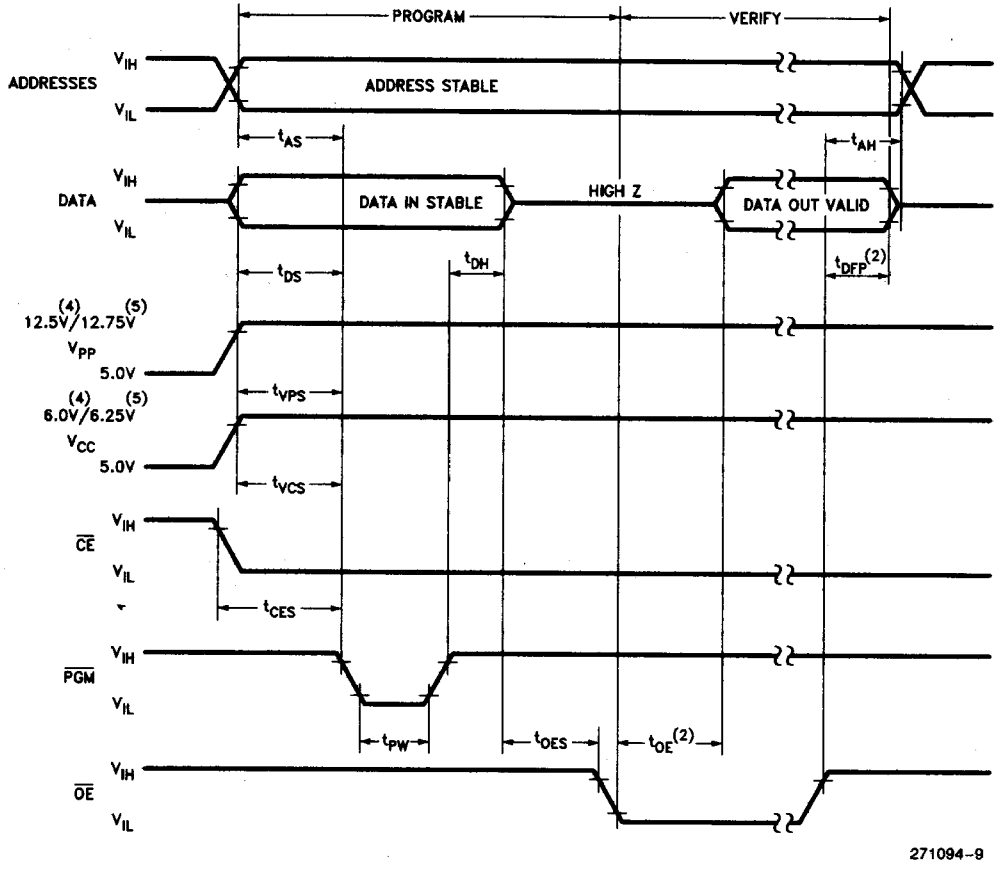
Symbol	Parameter	Limits				Conditions (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 2)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Intitial Program Pulse Width	0.95	1.0	1.05	ms	intelligent Programming Algorithm
		95	100	105	μs	Quick-Pulse Programming Algorithm
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	2.85		78.75	ms	intelligent Programming Algorithm
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with outputs O_0 to O_7 Unloaded.

PROGRAMMING WAVEFORMS



NOTES:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27C128, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.
4. int$_e$ligent Programming Algorithm voltage levels.
5. Quick-Pulse Programming Algorithm voltage levels.

7