CYPRESS SEMICONDUCTOR

CY7C291
CY7C292
2048 x 8 PROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— 35 ns (commercial)**
  - **— 50 ns (military)**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **EPROM technology 100% programmable**
- **Slim 300 mil or standard 600 mil packaging available**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2000V static discharge**

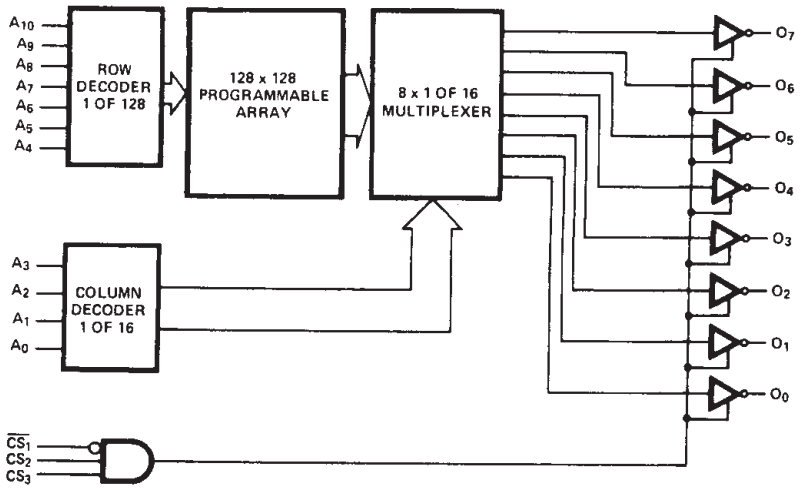
Product Characteristics

The CY7C291 and CY7C292 are high performance 2048 word by 8 bit CMOS PROMs. They are functionally identical, but are packaged in 300 mil and 600 mil wide packages respectively. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C291 and CY7C292 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW signal on $\overline{CS}_1$, and active HIGH signals on CS_2 and CS_3. The contents of the memory location addressed by the address lines (A_0–A_{10}) will become available on the output lines (O_0–O_7).

Logic Block Diagram



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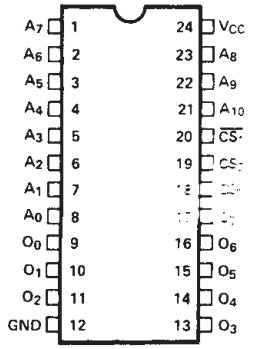
Pin Configurations



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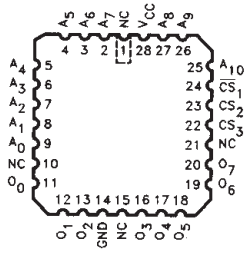

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Selection Guide

		7C291-35 7C292-35	7C291-50 7C292-50
Maximum Access Time (ns)		35	50
Maximum Operating Current (mA)	Commercial	100	90
	Military		120

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pins 18, 20) 14.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015.2)

Latchup Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to + 125°C	5V ±10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		7C291-35 7C292-35		7C291-50 7C292-50		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Level[2]			2.0		2.0		V
V_{IL}	Input LOW Level[2]				0.8		0.8	V
I_{IX}	Input Current	V_{CC} = Max., V_{CC} = GND		−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 3		Note 3		
I_{OZ}	Output Leakage Current	$V_{OL} \le V_{OUT} \le V_{OH}$, Output Disabled		−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		100		90	mA
			Military				120	mA

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. The CMOS process does not provide a clamp diode. However, the CY7C291 & CY7C292 are insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5. Measured on a sample basis.

Switching Characteristics Over the Operating Range[6]

Parameters	Description	CY7C291-35 CY7C292-35		CY7C291-50 CY7C292-50		Units
		Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		35		50	ns
t_{HZCS}	Chip Select Inactive to High Z[7]		25		25	ns
t_{ACS}	Chip Select Active to Output Valid		25		25	ns

AC Test Loads and Waveforms

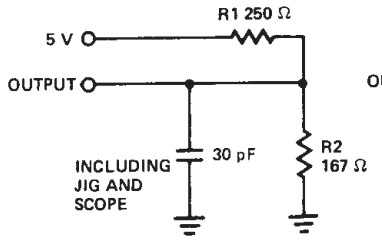


Figure 1a

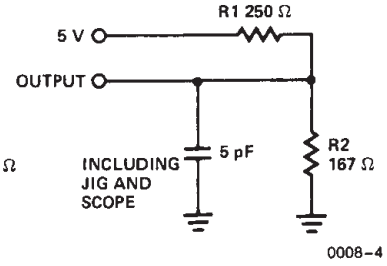


Figure 1b

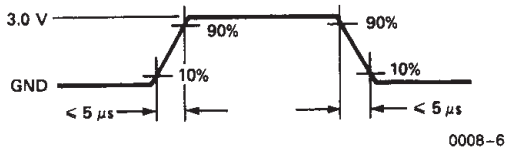
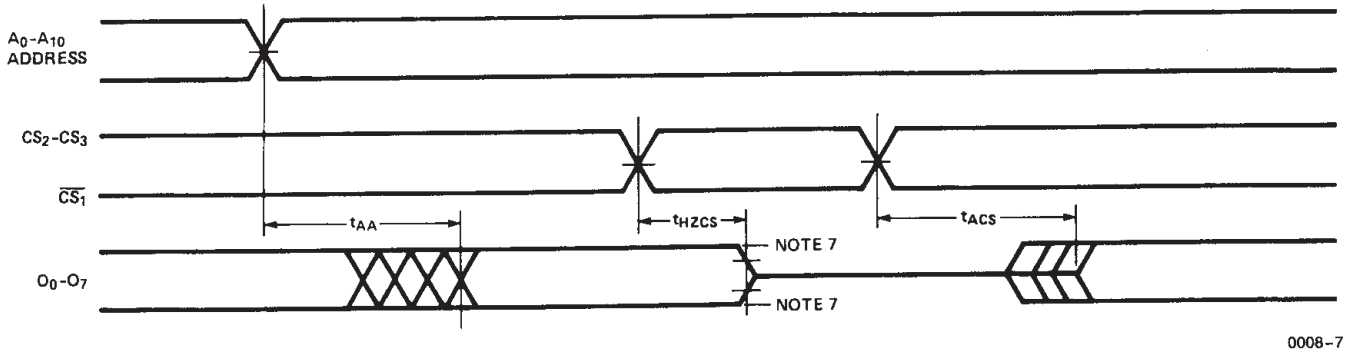


Figure 2. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT

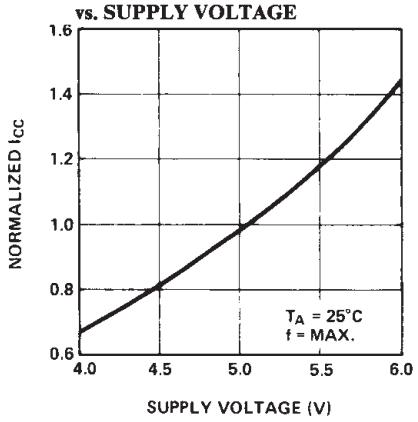


Notes:

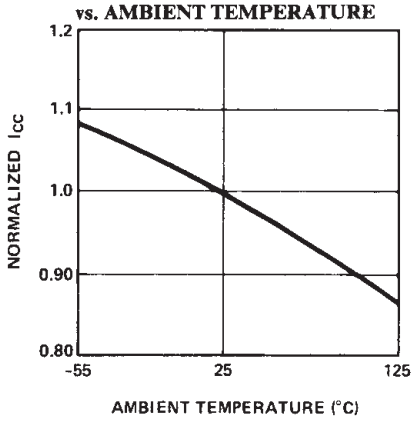
6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and loads shown in *Figures 1a, 1b.*
7. t_{HZCS} is tested with load shown in *Figure 1b.* Transition is measured at steady state High level −500 mV or steady state Low level +500 mV on the output from the 1.5V level on the input.

Typical DC and AC Characteristics

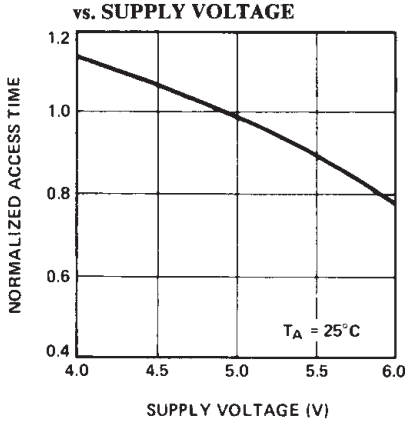
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



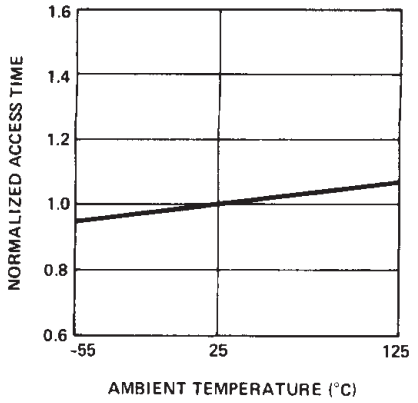
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



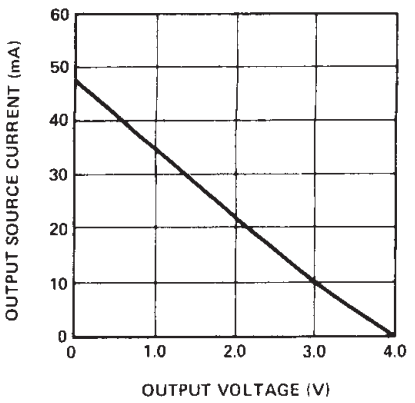
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



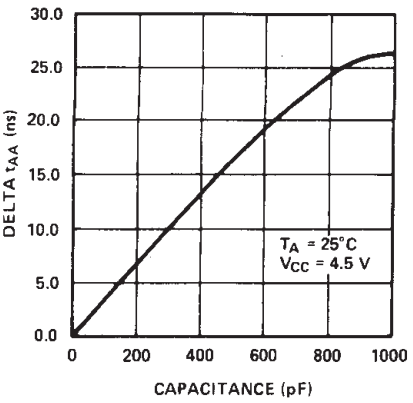
NORMALIZED ACCESS TIME vs. TEMPERATURE



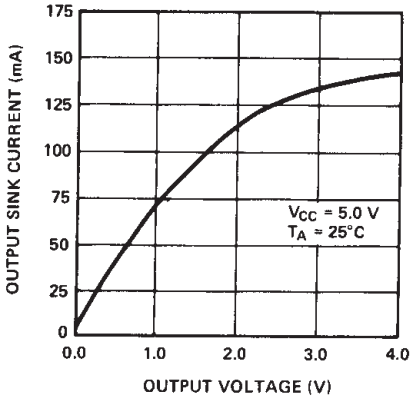
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



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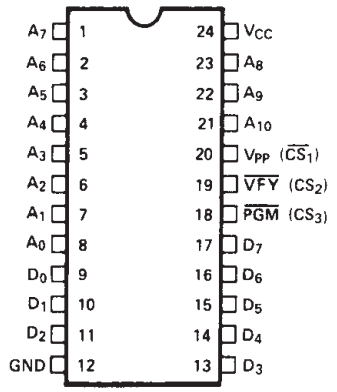

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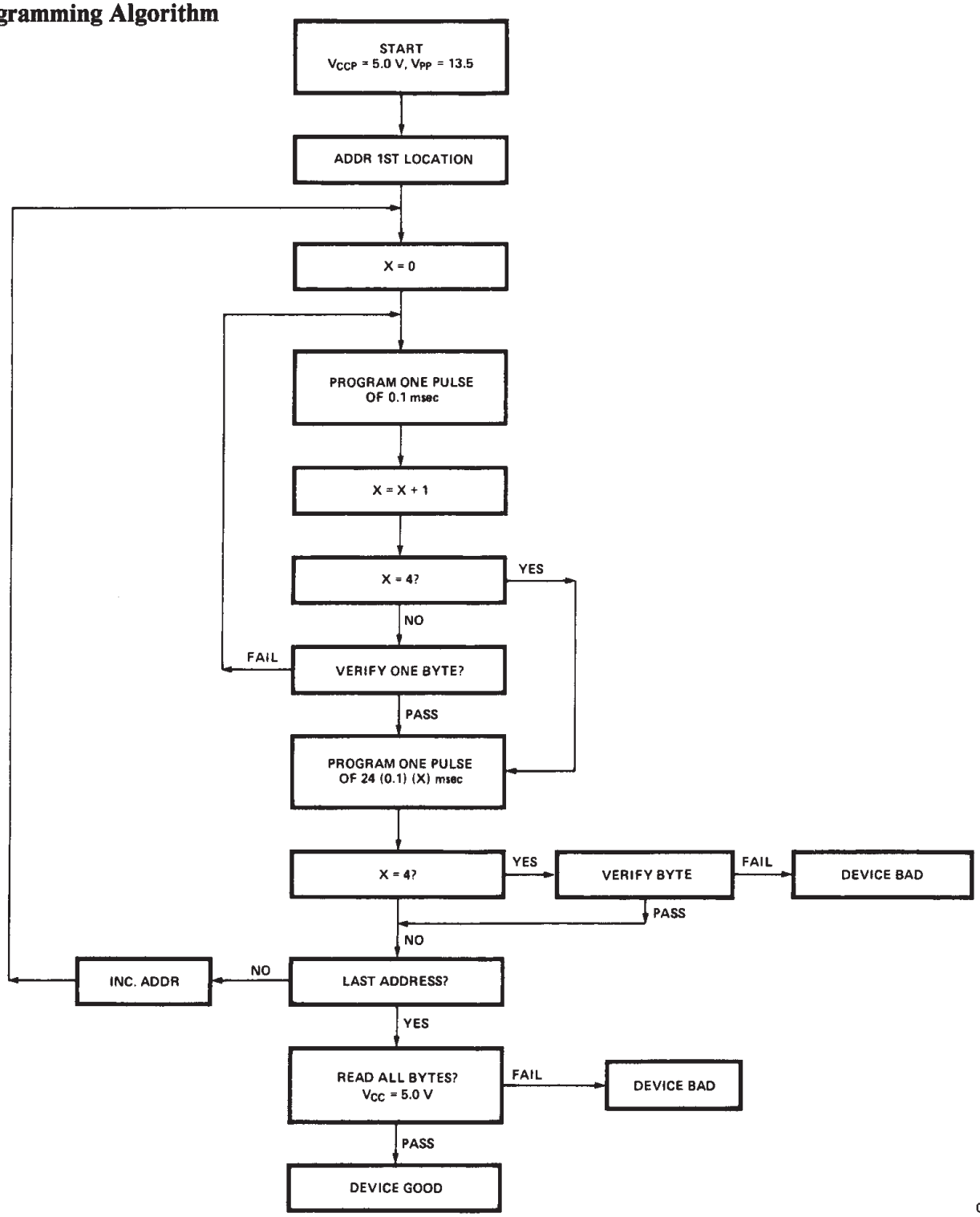
Figure 3. Programming Pinout

Programming Algorithm



The CY7C291 and CY7C292 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4*.

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the PGM pulse (t_{PP}) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verification is performed at V_{CCP} = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 5.0V.

Figure 4. Programming Flowchart

Programming Information

The 7C291 and 7C292 2K x 8 CMOS PROMs are implemented with a differential EPROM memory cell. The PROMs are delivered in an erased state, containing neither "1s" nor "0s". This erased condition of the array may be assessed using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see below.

Blank Check

A virgin device contains neither ones nor zeros because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 2047. A device is considered virgin if all locations are respectively "1s" and "0s" when addressed in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both ones and zeros. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

DC Programming Parameters T_A = 25°C

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage[1]	13.0	14.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input HIGH Voltage	3.0		V
V_{ILP}	Input LOW Voltage		0.4	V
V_{OH}	Output HIGH Voltage[2]	2.4		V
V_{OL}	Output LOW Voltage[2]		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters T_A = 25°C

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width[3]	100	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R, t_F	V_{PP} Rise and Fall Time[3]	1.0		μs
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify to High Z		1.0	μs

Notes:

1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

3

Mode Selection

Table 3

Mode		Pin Function			Outputs (9–11, 13–17)
	Read or Output Disable	CS_3	CS_2	$\overline{CS_1}$	
	Other	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	
	Pin Number	(18)	(19)	(20)	
Read		V_{IH}	V_{IH}	V_{IL}	Data Out
Output Disable[4]		X	X	V_{IH}	High Z
Output Disable[4]		X	V_{IL}	X	High Z
Output Disable[4]		V_{IL}	X	X	High Z
Program		V_{ILP}	V_{IHP}	V_{PP}	Data In
Program Verify		V_{IHP}	V_{ILP}	V_{PP}	Data Out
Program Inhibit		V_{IHP}	V_{IHP}	V_{PP}	High Z
Intelligent Program		V_{ILP}	V_{IHP}	V_{PP}	Data In
Blank Check Ones		V_{PP}	V_{ILP}	V_{ILP}	Ones
Blank Check Zeros		V_{PP}	V_{IHP}	V_{ILP}	Zeros

Notes:

4. X = Don't care but not to exceed V_{CC} + 5%.
5. During programming and verification, all unspecified pins to be at V_{ILP}.

Programming Sequence 2K x 8

Power the device for normal read mode operation with pin 18, 19 and 20 at V_{IH}. Per *Figure 5* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see Table 3. Again per *Figure 5* address, program, and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24 x the sum of the previous programming pulses before advancing to the next address to repeat the process.

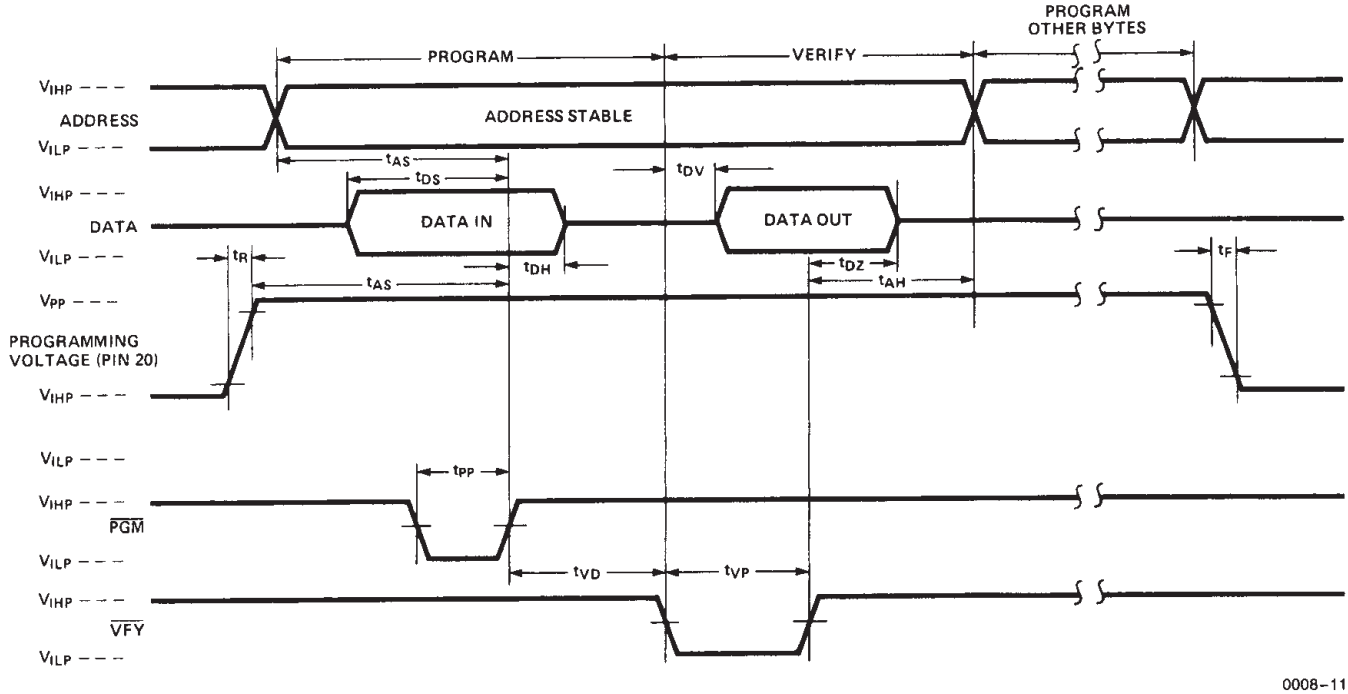


Figure 5. Programming Waveforms

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35 ns	CY7C291-35PC CY7C292-35PC CY7C291-35DC CY7C291-35LC CY7C292-35DC	P13 P11 D14 L64 D12	Commercial
50 ns	CY7C291-50PC CY7C292-50PC CY7C291-50DC CY7C291-50LC CY7C292-50DC	P13 P11 D14 L64 D12	Commercial
50 ns	CY7C291-50DMB CY7C291-50LMB CY7C292-50DMB	D14 L64 D12	Military

PROM Programming Information

Introduction

PROMs or Programmable Read Only Memories have existed since the early 1970's and continue to provide the highest speed non-volatile form of semiconductor memory available. Until the introduction of CMOS PROMs from Cypress, all PROMs were produced in bipolar technology, because bipolar technology provided the highest possible performance at an acceptable cost level. All bipolar PROMs use a fuse for the programming element. The fuses are in tact when the product is delivered to the user, and may be programmed or written once with a pattern and used or read infinitely. The fuses are literally blown using a high current supplied by a Programming System. Since the fuses may only be blown or programmed once, they may not be programmed during test. In addition, since they may not be programmed until the user determines the pattern, they may not be completely tested prior to shipment from the supplier. This inability to completely test, results in less than 100% yield during programming and use by the customer for two reasons. First, some percentage of the product fails to program. These devices fall out during the programming operation, and although a nuisance are easily identified. Additional yield is lost because the device fails to perform even though it programs correctly. This failure is normally due to the device being too slow. This is a more subtle failure, and can only be found by 100% post program AC testing, or even worse by trouble shooting an assembled board or system.

Cypress CMOS PROMs use an EPROM programming mechanism. This technology has been in use in MOS technologies since the early 1970s. However, as with most MOS technologies the emphasis has been on density, not performance. CMOS at Cypress is as fast as or faster than Bipolar and coupled with EPROM, becomes a viable alternative to bipolar PROMs from a performance point-of-view. In the arena of programming, EPROM has some significant advantages over fuse technology. EPROM cells are programmed by injecting charge on an isolated gate which permanently turns off the transistor. This mechanism can be reversed by irradiating the device with ultraviolet light. The fact that programming can be erased, totally changes the testing and programming situation and philosophy. All cells can be programmed during the manufacturing process and then erased prior to packaging and subsequent shipment. While these cells are programmed, the performance of each cell in the memory can be tested allowing the shipment of devices that program every time, and will perform as specified when programmed.

Programmable Technology

EPROM Process Technology

EPROM technology employs a floating or isolated gate between the normal control gate and the source/drain region of a transistor. This gate may be charged with electrons during the programming operation and when charged with electrons, the transistor is permanently turned off. When uncharged (the transistor is unprogrammed) the device may be turned on and off normally with the control gate. The state of the floating gate, charged or uncharged, is permanent because the gate is isolated in an extremely pure oxide. The charge may be removed if the device is irradiated with ultraviolet energy in the form of light. This ultraviolet light allows the electrons on the gate to recombine and discharge the gate. This process is repeatable and therefore can be used during the processing of the device repeatedly if necessary to assure programming function and performance.

Two Transistor Cells

In order to provide an EPROM cell that is as fast as the fuse technology employed in bipolar processes, Cypress uses a two transistor EPROM cell. One transistor is optimized for reliable programming, and one transistor is optimized for high speed. The floating gates are connected such that charge injected on the floating gate of the programming transistor is conducted to the read transistor, biasing it off.

Differential Memory Cells

A second area that high speed CMOS PROM design technology differs from conventional high density EPROM designs is in the area of differential cell/differential sensing versus single ended cell/differential sensing with a dummy cell.

In a conventional high density EPROM a single EPROM transistor is used to switch the input to one side of a differential sense amplifier. The other side of the sense amplifier is biased at an intermediate level with a dummy cell. An unprogrammed EPROM transistor will conduct and drive the sense amplifier to a logic "0". A programmed EPROM transistor will not conduct, and consequently drives the sense amplifier to a logic "1". A conventional EPROM cell therefore is delivered with a specific state "0" or "1" in it depending on the number of inversions after the sense amplifier and can always be programmed to the opposite state. Access time in this conventional approach is heavily dependent on the time the selected EPROM transistor takes to move the input of the sense amplifier from a quiescent condition to the threshold that the dummy cell is biasing the second input to the sense amplifier. This bias is several volts, and requires a significant delay before the sense amplifier begins to react.

Cypress PROMs employ a true differential cell approach, with EPROM cells attached to both inputs of the sense amplifier. As indicated above, the read transistor which is optimized for speed is actually the transistor attached to the sense amplifier. In the erased state, both EPROM transistors conduct when selected eccentrically biasing the input of the sense amplifier at the same level. If the inputs were at identical levels, the output of the sense amplifier would be in a mestastable condition or, neither a "1" nor "0". In actual practice the natural bias and high gain of the sense amplifier combine to cause the output to favor one or the other stable conditions. The difference between the two conditions is however only a few millivolts and the memory cell should be considered to contain neither a "1" nor a "0". As a result of this design approach, the memory cell must be programmed to either a "1" or a "0" depending on the desired condition and the conventional BLANK CHECK mechanism is invalid. The benefit of the approach however is that only a small differential signal from the cell begins the sense amplifier switching and the access time of the memory is extremely fast.

Programming Algorithim

Byte Addressing and Programming

All Cypress CMOS PROMs are addressed and programmed on a byte basis unlike the bipolar products that they replace. The address lines used to access the memory in a read mode are the same for programming, and the address map is identical. The information to be programmed into each byte is presented on the data out pins during the programming operation and the data is read from these same pins for verification that the byte has been programmed.

Blank Check

Since a differential cell contains neither a "1" nor a "0" before it is programmed, the conventional BLANK CHECK is not valid. For this reason, all Cypress CMOS PROMs contain a special BLANK CHECK mode of operation. Blank check is performed by separately examining the "0" and "1" sides of the differential memory cell to determine whether either side has been independently programmed. This is accomplished in two passes one comparing the "0" side of the differential cell against a reference voltage applied to the opposite side of the sense amplifier and then repeating this operation for the "1"s side of the cell. The modes are called BLANK CHECK ONES, and BLANK CHECK ZEROS. These modes are entered by the application of a supervoltage to the device.

Programming the Data Array

Programming is accomplished by applying a supervoltage to one pin of the device causing it to enter the programming mode of operation. This also provides the programming voltage for the cells to be programmed. In this mode of operation, the address lines of the device are used to address each location to be programmed, and the data is presented on the pins normally used for reading the contents of the device. Each device has a READ and a WRITE pin in the programming mode. These are active low signals and cause the data on the output pins to be written into the addressed memory location in the case of the WRITE signal or read out of the device in the case of the READ signal. When both the READ and WRITE signals are high, the outputs are disabled and in a high impedance state. Programming therefore is accomplished by placing data on the output pins, and writing it into the addressed location with the WRITE signal. Verification of data is accomplished by reading the information on the output pins while the READ signal is active.

The timing for actual programming is supplied in the unique programming specification for each device.

Special Features

Depending on the specific CMOS PROM in question, additional features that require programming may be available to the designer. Two of these features are a Programmable INITIAL BYTE and Programmable SYNCHRONOUS/ASYNCHRONOUS ENABLE available in some of the registered devices. Like programming the array, these features make use of EPROM cells and are programmed in a similar manner, using supervoltages. The specific timing and programming requirements are specified in the data sheet of the device employing the feature.

Programming Support

Programming support for Cypress CMOS PROMs is available from a number of programmer manufacturers some of which are listed below.

Data I/O
Programmer Model 29
Unipak II

Data I/O Corporation
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444

Stag
Programmer PPZ

Stag Microsystems
528-5 Weddell Dr.
Sunnyvale, CA 94089
(408) 745-1991

Sunrise Systems
Programmer Model Z-1000 B

Sunrise Systems
524 S. Vermont
Glendora, CA 91740
(818) 914-1926

Wavetek Digilec
Programmer Model 803

Wavetek Digilec
586 Weddell Dr.
Suite 1
Sunnyvale, CA 94089
(408) 745-0722