

MEMORY

**CMOS 256K × 16 BIT
FAST PAGE MODE DYNAMIC RAM****MB814260-60/-70****CMOS 262,144 × 16 BIT Fast Page Mode Dynamic RAM****DESCRIPTION**

The Fujitsu MB814260 is a fully decoded CMOS Dynamic RAM (DRAM) that contains 4,194,304 memory cells accessible in 16-bit increments. The MB814260 features a “fast page” mode of operation whereby high-speed access of up to 512 × 16-bits of data can be selected in the same row. The MB814260-60/-70 DRAMs are ideally suited for memory applications such as embedded control, buffer, portable computers, and video imaging equipment where very low power dissipation and high bandwidth are basic requirements of the design.

The MB814260 is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes.

ABSOLUTE MAXIMUM RATINGS (See NOTE.)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +7	V
Voltage of V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +7	V
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	—	50	mA
Storage Temperature	T_{STG}	-55 to +125	°C
Temperature under Bias	T_{BIAS}	0 to +70	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

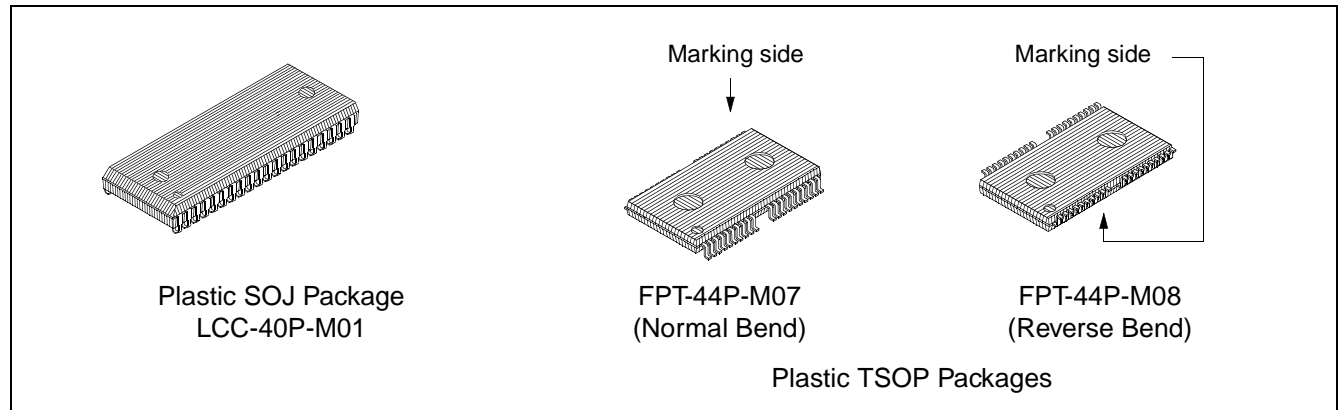
MB814260-60/MB814260-70

■ PRODUCT LINE & FEATURES

Parameter		MB814260-60	MB814260-70
RAS Access Time		60 ns max.	70 ns max.
CAS Access Time		20 ns max.	20 ns max.
Address Access Time		30 ns max.	35 ns max.
Random Cycle Time		110 ns max.	125 ns min.
Fast Page Mode Cycle Time		40 ns min.	45 ns min.
Low Power Dissipation	Operating current	523 mW max.	462 mW max.
	Standby current	11 mW max. (TTL level)/5.5 mW max. (CMOS level)	

- 262,144 words × 16 bit organization
- Silicon gate, CMOS, Advanced Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- 9 rows × 9 columns, addressing scheme
- $\overline{1WE} / \overline{2CAS}$
- Early Write or \overline{OE} controlled Write capability
- RAS only CAS-before-RAS, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

■ PACKAGE

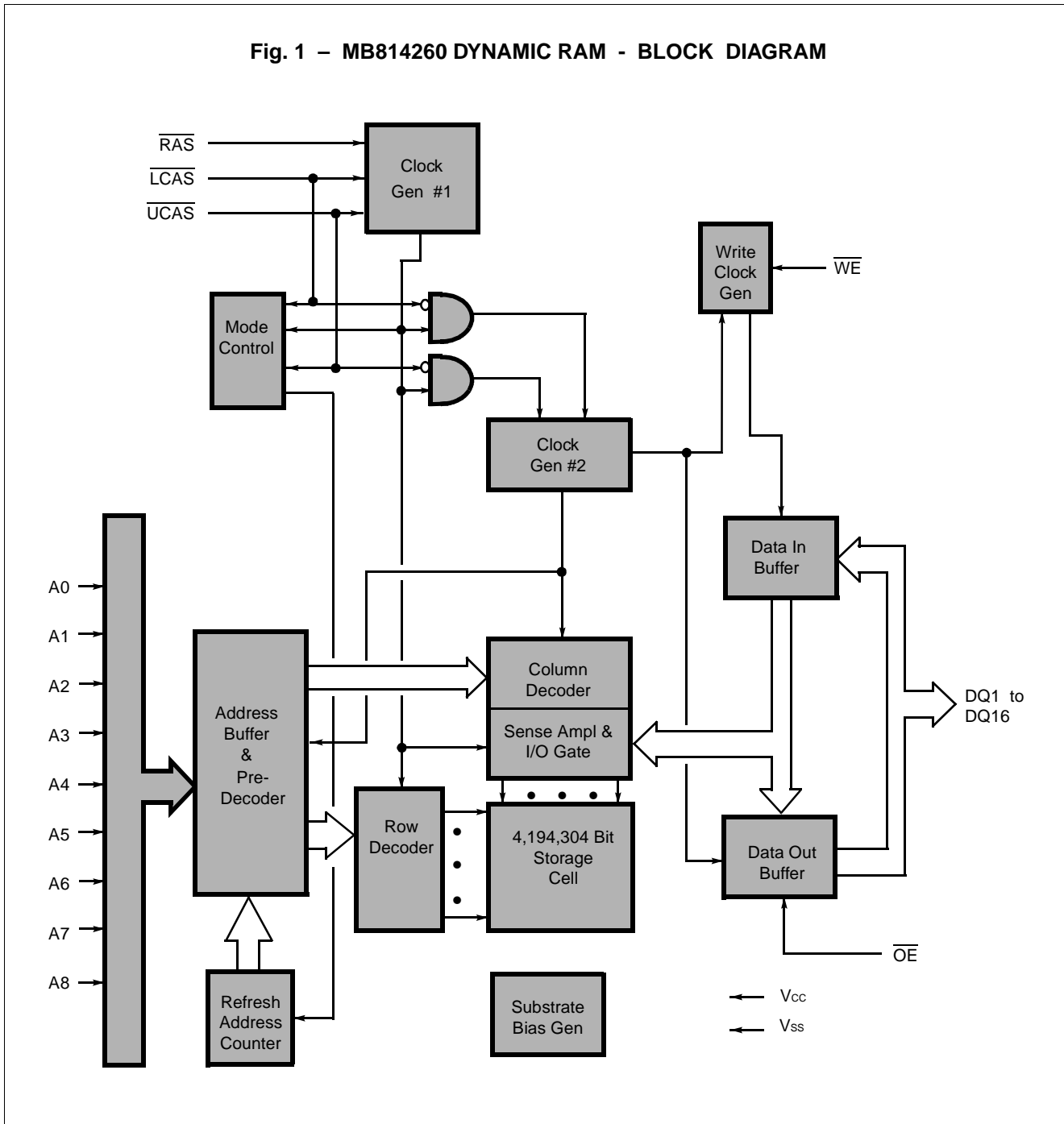


Package and Ordering Information

- 40-pin plastic (400 mil) SOJ, order as MB814260-xxPJ
- 44-pin plastic (400 mil) TSOP-II with normal bend leads, order as MB814260-xxPFTN
- 44-pin plastic (400 mil) TSOP-II with reverse bend leads, order as MB814260-xxPFTR

MB814260-60/MB814260-70

Fig. 1 – MB814260 DYNAMIC RAM - BLOCK DIAGRAM



■ CAPACITANCE

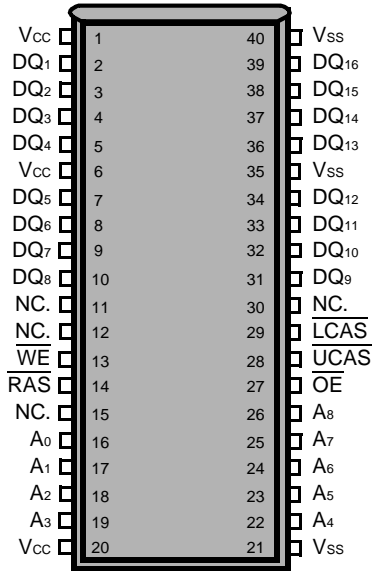
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A ₀ to A ₈	C _{IN1}	—	5	pF
Input Capacitance, RAS, LCAS, UCAS, WE, OE	C _{IN2}	—	7	pF
Input/Output Capacitance, DQ ₁ to DQ ₁₆	C _{DQ}	—	7	pF

MB814260-60/MB814260-70

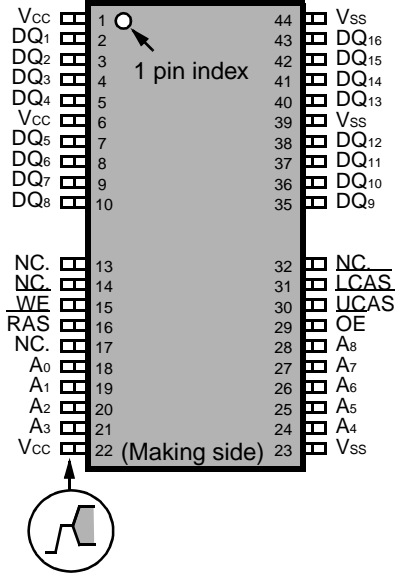
PIN ASSIGNMENTS AND DESCRIPTIONS

40-Pin SOJ:
(TOP VIEW)

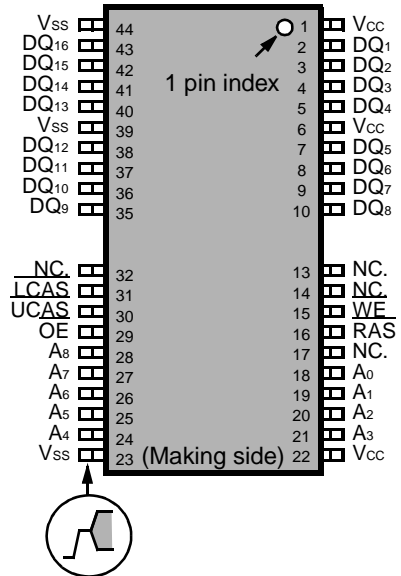


44-Pin FPT:
(TOP VIEW)

<Normal Bend : FPT-44P-M07>



<Reverse Bend : FPT-44P-M08>



Designator	Function
A ₀ to A ₈	Address inputs. row : A ₀ to A ₈ column : A ₀ to A ₈ refresh : A ₀ to A ₈
$\overline{\text{RAS}}$	Row address strobe.
$\overline{\text{LCAS}}$	Lower column address strobe
$\overline{\text{UCAS}}$	Upper column address strobe
$\overline{\text{WE}}$	Write enable
$\overline{\text{OE}}$	Output enable.
DQ ₁ to DQ ₁₆	Data Input/ Output
V _{cc}	+5 volt power supply.
V _{ss}	Circuit ground.

MB814260-60/MB814260-70

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit	Ambient Operating Temp
Supply Voltage	1	V _{CC}	4.5	5.0	5.5	V	0°C to +70°C
		V _{SS}	0	0	0		
Input High Voltage, all inputs	1	V _{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs(*)	1	V _{IL}	-0.3	—	0.8	V	
Input Low Voltage, DQ(*)	1	V _{ILD}	-0.3	—	0.8	V	

* : Undershoots of up to -2.0 volts with a pulse width not exceeding 20 ns are acceptable.

■ FUNCTIONAL OPERATION

ADDRESS INPUTS

Eighteen input bits are required to decode any sixteen of 4,194,304 cell addresses in the memory matrix. Since only nine address bits are available, the column and row inputs are separately strobed by $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ and $\overline{\text{RAS}}$ as shown in Figure 5. First, nine row address bits are input on pins A₀-through-A₈ and latched with the row address strobe ($\overline{\text{RAS}}$) then, nine column address bits are input and latched with the column address strobe ($\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$). Both row and column addresses must be stable on or before the falling edges of $\overline{\text{RAS}}$ and $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$, respectively. The address latches are the flow-through type; thus, address information appearing after t_{RAH} (min)+t_τ is automatically treated as the column address to start select operation of the column decode. Therefore, to have correct data within t_{RAC}, the column address should be input within t_{RAD}(max.). If t_{RAD} > t_{RAD} (max.), the access time is the later one of either t_{AA} or t_{CAS}.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{\text{WE}}$. When $\overline{\text{WE}}$ is active Low, a write cycle is initiated; when $\overline{\text{WE}}$ is High, a read cycle is selected. During the read mode, input data are ignored. When an early write cycle is executed, the output buffers stay in a high-impedance state during the cycle.

DATA INPUT

Input data are written into memory in either of three basic ways—the early write cycle, the $\overline{\text{OE}}$ (delayed) write cycle, and the read-modify-write cycle. The falling edge of $\overline{\text{WE}}$ or $\overline{\text{LCAS}}/\overline{\text{UCAS}}$, whichever is later, serves as the input data-latch strobe. In the early write cycle, the input data of DQ₁-DQ₈ are strobed by $\overline{\text{LCAS}}$ and DQ₉-DQ₁₆ are strobed by $\overline{\text{UCAS}}$ and the setup/hold times are referenced to each falling edge of $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ because $\overline{\text{WE}}$ goes Low before $\overline{\text{LCAS}}/\overline{\text{UCAS}}$. In the delayed write or read-modify-write cycle, $\overline{\text{WE}}$ goes Low after $\overline{\text{LCAS}}/\overline{\text{UCAS}}$; thus, input data is strobed by $\overline{\text{WE}}$ and all setup/hold times are referenced to the falling edge of $\overline{\text{WE}}$. Since this device is an I/O common type, when the delayed write or read-modified-write is executed, I/O data have to be controlled by $\overline{\text{OE}}$.

DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- t_{RAC} : from the falling edge of $\overline{\text{RAS}}$ when t_{RCD} (max) is satisfied.
- t_{CAC} : from the falling edge of $\overline{\text{LCAS}}$ (for DQ₁-DQ₈) $\overline{\text{UCAS}}$ (for DQ₉-DQ₁₆) when t_{RCD} is greater than t_{RCD} (max).
- t_{AA} : from column address input when t_{RAD} is greater than t_{RAD} (max).
- t_{OEA} : from the falling edge of $\overline{\text{OE}}$ when $\overline{\text{OE}}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}.

The data remains valid until either $\overline{\text{LCAS}}/\overline{\text{UCAS}}$ or $\overline{\text{OE}}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

MB814260-60/MB814260-70

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{\text{RAS}}$ is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 512×16-bits can be accessed. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or ready-modify-write cycles are permitted.

MB814260-60/MB814260-70

■ DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Notes 3

Parameter	Notes	Symbol	Conditions	Value		Unit
				Min.	Max.	
Output high voltage	1	V_{OH}	$I_{OH} = -5 \text{ mA}$	2.4	—	V
Output low voltage	1	V_{OL}	$I_{OL} = 4.2 \text{ mA}$	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	$0 \text{ V} \leq V_{IN} \leq 5.5 \text{ V};$ $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V};$ $V_{SS} = 0 \text{ V};$ All other pins not under test = 0 V	-10	10	μA
Output leakage current		$I_{DQ(L)}$	$0 \text{ V} \leq V_{OUT} \leq 5.5 \text{ V};$ Data out disabled	-10	10	
Operating current (Average power supply current) 2	MB814260-60	I_{CC1}	$\overline{\text{RAS}}$ & $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$ cycling; $t_{RC} = \text{min}$	—	95	mA
	MB814260-70				84	
Standby current (Power supply current)	TTL level	I_{CC2}	$\overline{\text{RAS}} = \overline{\text{LCAS}}$, $\overline{\text{UCAS}} = V_{IH}$	—	2.0	mA
	CMOS level		$\overline{\text{RAS}} = \overline{\text{LCAS}}$, $\overline{\text{UCAS}} \geq V_{CC} - 0.2 \text{ V}$		1.0	
Refresh current #1 (Average power supply current) 2	MB814260-60	I_{CC3}	$\overline{\text{LCAS}}$, $\overline{\text{UCAS}} = V_{IH}$, $\overline{\text{RAS}}$ cycling; $t_{RC} = \text{min}$	—	95	mA
	MB814260-70				84	
Fast Page Mode current 2	MB814260-60	I_{CC4}	$\overline{\text{RAS}} = V_{IL}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$ cycling; $t_{PC} = \text{min}$	—	95	mA
	MB814260-70				84	
Refresh current #2 (Average power supply current) 2	MB814260-60	I_{CC5}	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$; $t_{RC} = \text{min}$	—	95	mA
	MB814260-70				84	

MB814260-60/MB814260-70

■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814260-60		MB814260-70		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh		t_{REF}	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		t_{RC}	110	—	125	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	150	—	170	—	ns
4	Access Time from \overline{RAS}	6, 9	t_{RAC}	—	60	—	70	ns
5	Access Time from \overline{CAS}	7, 9	t_{CAC}	—	20	—	20	ns
6	Column Address Access Time	8, 9	t_{AA}	—	30	—	35	ns
7	Output Hold Time		t_{OH}	0	—	0	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	ns
9	Output Buffer Turn Off Delay Time	10	t_{OFF}	—	15	—	15	ns
10	Transition Time		t_t	2	50	2	50	ns
11	\overline{RAS} Precharge Time		t_{RP}	40	—	45	—	ns
12	\overline{RAS} Pulse Width		t_{RAS}	60	100000	70	100000	ns
13	\overline{RAS} Hold Time		t_{RSH}	20	—	20	—	ns
14	\overline{CAS} to \overline{RAS} Precharge Time		t_{CRP}	0	—	0	—	ns
15	\overline{RAS} to \overline{CAS} Delay Time	11, 12	t_{RCD}	20	40	20	50	ns
16	\overline{CAS} Pulse Width		t_{CAS}	20	10000	20	10000	ns
17	\overline{CAS} Hold Time		t_{CSH}	60	—	70	—	ns
18	\overline{CAS} Precharge Time (Normal)	19	t_{CPN}	10	—	10	—	ns
19	Row Address Setup Time		t_{ASR}	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	10	—	ns
21	Column Address Setup Time		t_{ASC}	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	12	—	12	—	ns
23	\overline{RAS} to Column Address Delay Time	13	t_{RAD}	15	30	15	35	ns
24	Column Address to \overline{RAS} Lead Time		t_{RAL}	30	—	35	—	ns
25	Column Address to \overline{CAS} Lead Time		t_{CAL}	30	—	35	—	ns
26	Read Command Setup Time		t_{RCS}	0	—	0	—	ns
27	Read Command Hold Time Referenced to \overline{RAS}	14	t_{RRH}	0	—	0	—	ns
28	Read Command Hold Time Referenced to \overline{CAS}	14	t_{RCH}	0	—	0	—	ns
29	Write Command Setup Time	15	t_{WCS}	0	—	0	—	ns
30	Write Command Hold Time		t_{WCH}	10	—	10	—	ns
31	\overline{WE} Pulse Width		t_{WP}	10	—	10	—	ns
32	Write Command to \overline{RAS} Lead Time		t_{RWL}	15	—	20	—	ns

(Continued)

MB814260-60/MB814260-70

■ AC CHARACTERISTICS (Continued)

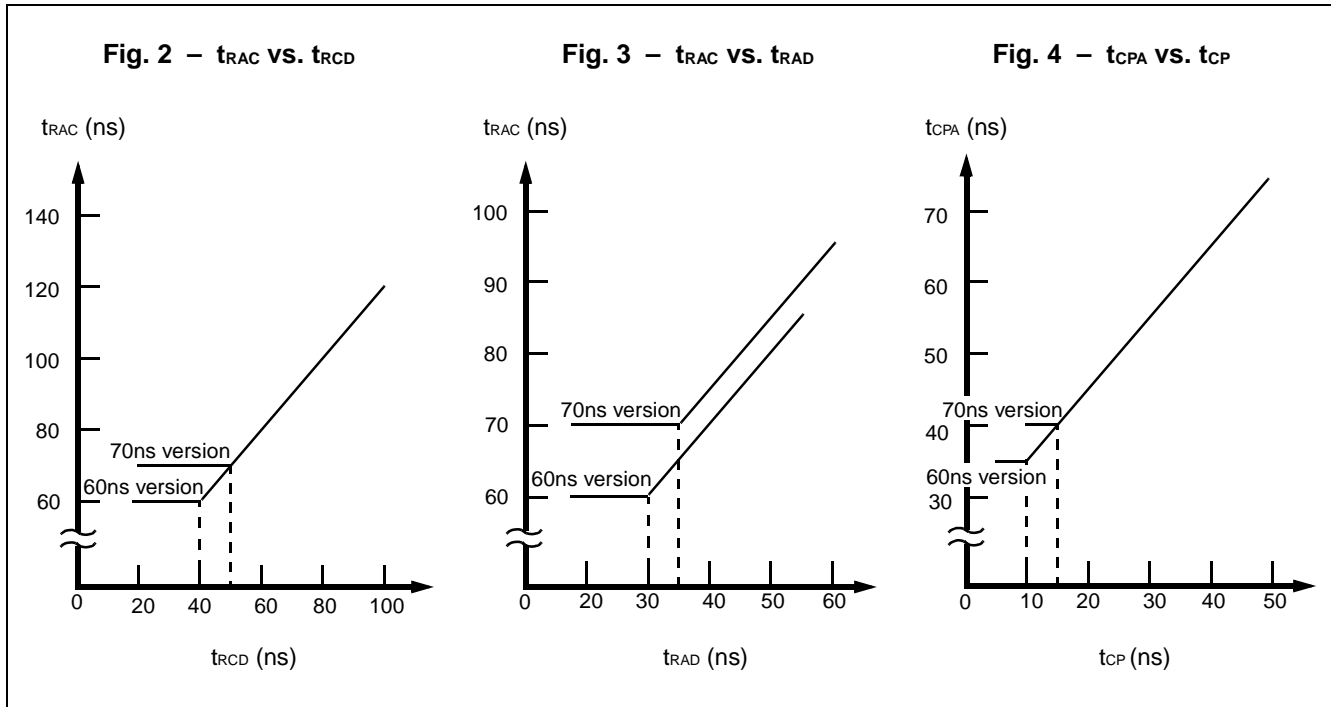
(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814260-60		MB814260-70		Unit
				Min.	Max.	Min.	Max.	
33	Write Command to CAS Lead Time		t _{CWL}	15	—	18	—	ns
34	DIN Setup Time		t _{DS}	0	—	0	—	ns
35	DIN Hold Time		t _{DH}	10	—	10	—	ns
36	RAS to WE Delay Time		t _{RWD}	85	—	95	—	ns
37	CAS to WE Delay Time		t _{CWD}	40	—	40	—	ns
38	Column Address to WE Delay Time		t _{AWD}	55	—	60	—	ns
39	RAS Precharge Time to CAS Active Time (Refresh cycles)		t _{RPC}	10	—	10	—	ns
40	CAS Set Up Time for CAS-before-RAS Refresh		t _{CSR}	0	—	0	—	ns
41	CAS Hold Time for CAS-before-RAS Refresh		t _{CHR}	10	—	10	—	ns
42	Access Time from OE	[9]	t _{OEA}	—	20	—	20	ns
43	Output Buffer Turn Off Delay from OE	[10]	t _{OEZ}	—	15	—	15	ns
44	OE to RAS Lead Time for Valid Data		t _{OEL}	10	—	10	—	ns
45	OE Hold Time Referenced to WE	[16]	t _{OEH}	0	—	0	—	ns
46	OE to Data in Delay Time		t _{OED}	15	—	15	—	ns
47	DIN to CAS Delay Time	[17]	t _{DZC}	0	—	0	—	ns
48	DIN to OE Delay Time	[17]	t _{DZO}	0	—	0	—	ns
50	Column Address Hold Time from RAS		t _{AR}	32	—	32	—	ns
51	Write Command Hold Time from RAS		t _{WCR}	30	—	30	—	ns
52	DIN Hold Time Referenced to RAS		t _{DHR}	30	—	30	—	ns
53	CAS to Data in Delay Time		t _{CDD}	15	—	15	—	ns
60	Fast Page Mode RAS Pulse Width		t _{RASP}	60	200000	70	200000	ns
61	Fast Page Mode Read/Write Cycle Time		t _{PC}	40	—	45	—	ns
62	Fast Page Mode Read-Modify-Write Cycle Time		t _{PRWC}	80	—	90	—	ns
63	Access Time from CAS Precharge	[9, 18]	t _{CPA}	—	35	—	40	ns
64	Fast Page Mode CAS Pulse width		t _{CP}	10	—	10	—	ns
65	Fast Page Mode RAS Hold Time from CAS Precharge		t _{RHCP}	35	—	40	—	ns
66	Fast Page Mode CAS Precharge to WE Delay Time		t _{CPWD}	55	—	60	—	ns

MB814260-60/MB814260-70

- Notes: 1. Referenced to V_{SS} . To all V_{CC} (V_{SS}) pins, the same supply voltage should be applied.
2. I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
 I_{CC} depends on the number of address change as $\overline{RAS} = V_{IL}$ and $\overline{UCAS} = V_{IH}$, $\overline{LCAS} = V_{IH}$, $V_{IL} > -0.3V$.
 I_{CC1} , I_{CC3} and I_{CC5} are specified at one time of address change during $\overline{RAS} = V_{IL}$ and $\overline{UCAS} = V_{IH}$, $\overline{LCAS} = V_{IH}$.
 I_{CC4} is specified at one time of address change during one Page cycle.
3. An Initial pause ($\overline{RAS} = \overline{CAS} = V_{IH}$) of 200 μs is required after power-up followed by any eight \overline{RAS} -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight \overline{CAS} -before- \overline{RAS} initialization cycles instead of 8 \overline{RAS} cycles are required.
4. AC characteristics assume $t_T = 5$ ns.
5. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min.) and V_{IL} (max.).
6. Assumes that $t_{RCD} \leq t_{RCD}(\text{max.})$, $t_{RAD} \leq t_{RAD}(\text{max.})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}(\text{max.})$, $t_{RAD} \geq t_{RAD}(\text{max.})$, and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC} .
8. If $t_{RAD} \geq t_{RAD}(\text{max.})$ and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA} .
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the $t_{RCD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
12. $t_{RCD}(\text{min.}) = t_{RAH}(\text{min.}) + 2t_T + t_{ASC}(\text{min.})$.
13. Operation within the $t_{RAD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}(\text{min.})$ the data output pin will remain High-Z state through entire cycle.
16. Assumes that $t_{WCS} < t_{WCS}(\text{min.})$.
17. Either t_{DZC} or t_{DZO} must be satisfied.
18. t_{CPA} is access time from the selection of a new column address (that is caused by changing both \overline{UCAS} and \overline{LCAS} from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than $t_{CPA}(\text{max.})$.
19. Assumes that \overline{CAS} -before- \overline{RAS} refresh.

MB814260-60/MB814260-70



FUNCTIONAL TRUTH TABLE

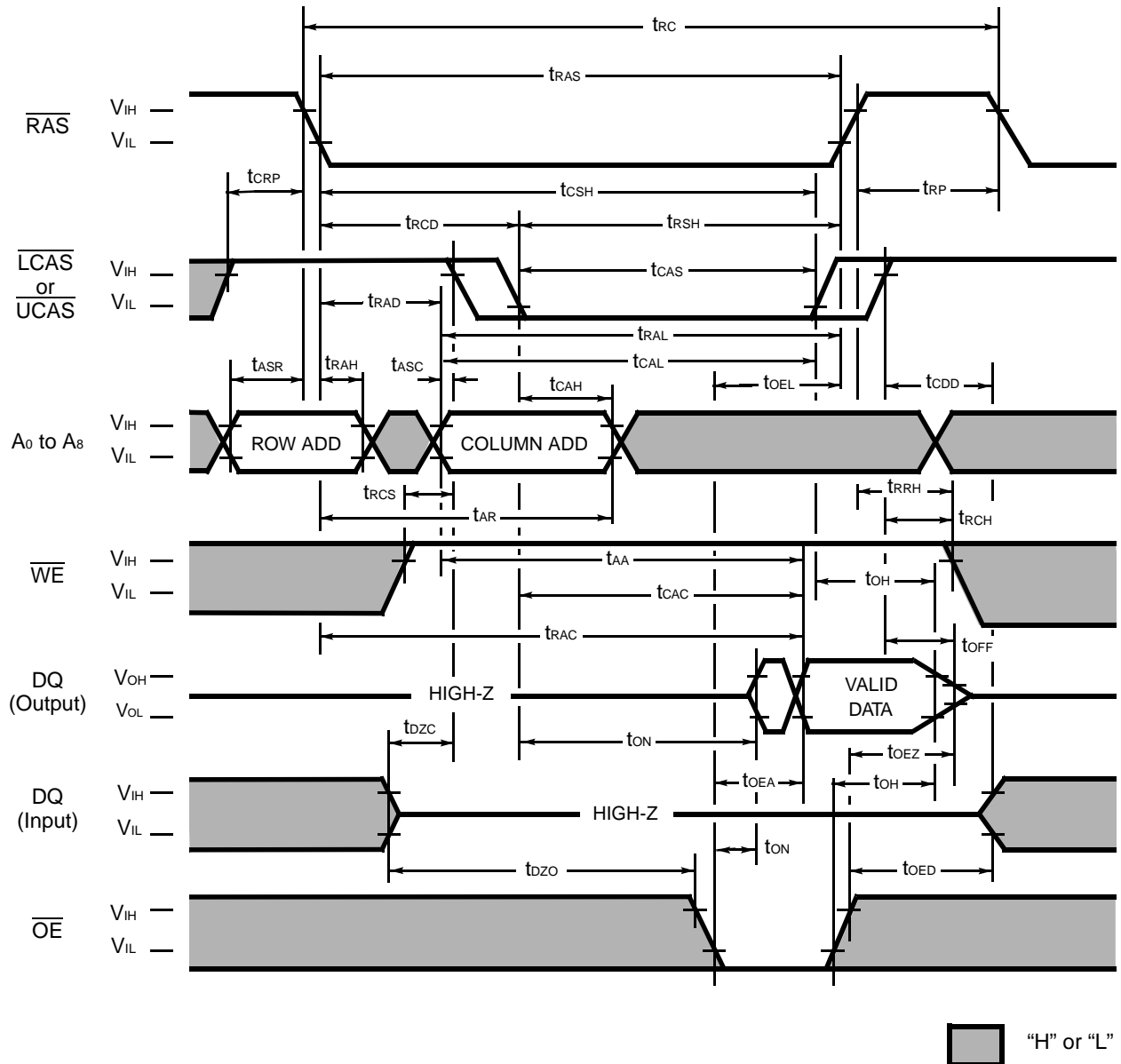
Operation Mode	Clock Input					Address		Input/Output Data				Refresh	Note
	\overline{RAS}	\overline{LCA}_S	\overline{UCA}_S	\overline{WE}	\overline{OE}	Row	Column	DQ ₁ to DQ ₈		DQ ₉ to DQ ₁₆			
								Input	Output	Input	Output		
Standby	H	H	H	X	X	—	—	—	High-Z	—	High-Z	—	
Read Cycle	L	L H L	H L L	H	L	Valid	Valid	—	Valid High-Z Valid	—	High-Z Valid Valid	Yes*	$t_{RCS} \geq t_{RCS}(\text{min.})$
Write Cycle (Early Write)	L	L H L	H L L	L	X	Valid	Valid	Valid — Valid	High-Z	— Valid Valid	High-Z	Yes*	$t_{WCS} \geq t_{WCS}(\text{min.})$
Read-Modify-Write Cycle	L	L H L	H L L	H→L	L→H	Valid	Valid	Valid — Valid	Valid High-Z Valid	— Valid Valid	High-Z Valid Valid	Yes*	
\overline{RAS} -only Refresh Cycle	L	H	H	X	X	Valid	—	—	High-Z	—	High-Z	Yes	
\overline{CAS} -before- \overline{RAS} Refresh Cycle	L	L	L	X	X	—	—	—	High-Z	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}(\text{min.})$
Hidden Refresh Cycle	H→L	L H L	H L L	H	L	—	—	—	Valid High-Z Valid	—	High-Z Valid Valid	Yes	Previous data is kept.

X; "H" or "L"

*; It is impossible in Fast Page Mode.

MB814260-60/MB814260-70

Fig. 5 – READ CYCLE



DESCRIPTION

To implement a read operation, a valid address is latched in by the \overline{RAS} and \overline{LCAS} or \overline{UCAS} address strobes and with \overline{WE} set to a High level and \overline{OE} set to a low level, the output is valid once the memory access time has elapsed. \overline{LCAS} controls the input/output data on DQ₁-DQ₈ pins, \overline{UCAS} controls one on DQ₈-DQ₁₆ pins. The access time is determined by RAS (t_{RC}), $\overline{LCAS}/\overline{UCAS}$ (t_{CAC}), \overline{OE} (t_{OE}) or column addresses (t_{AA}) under the following conditions:

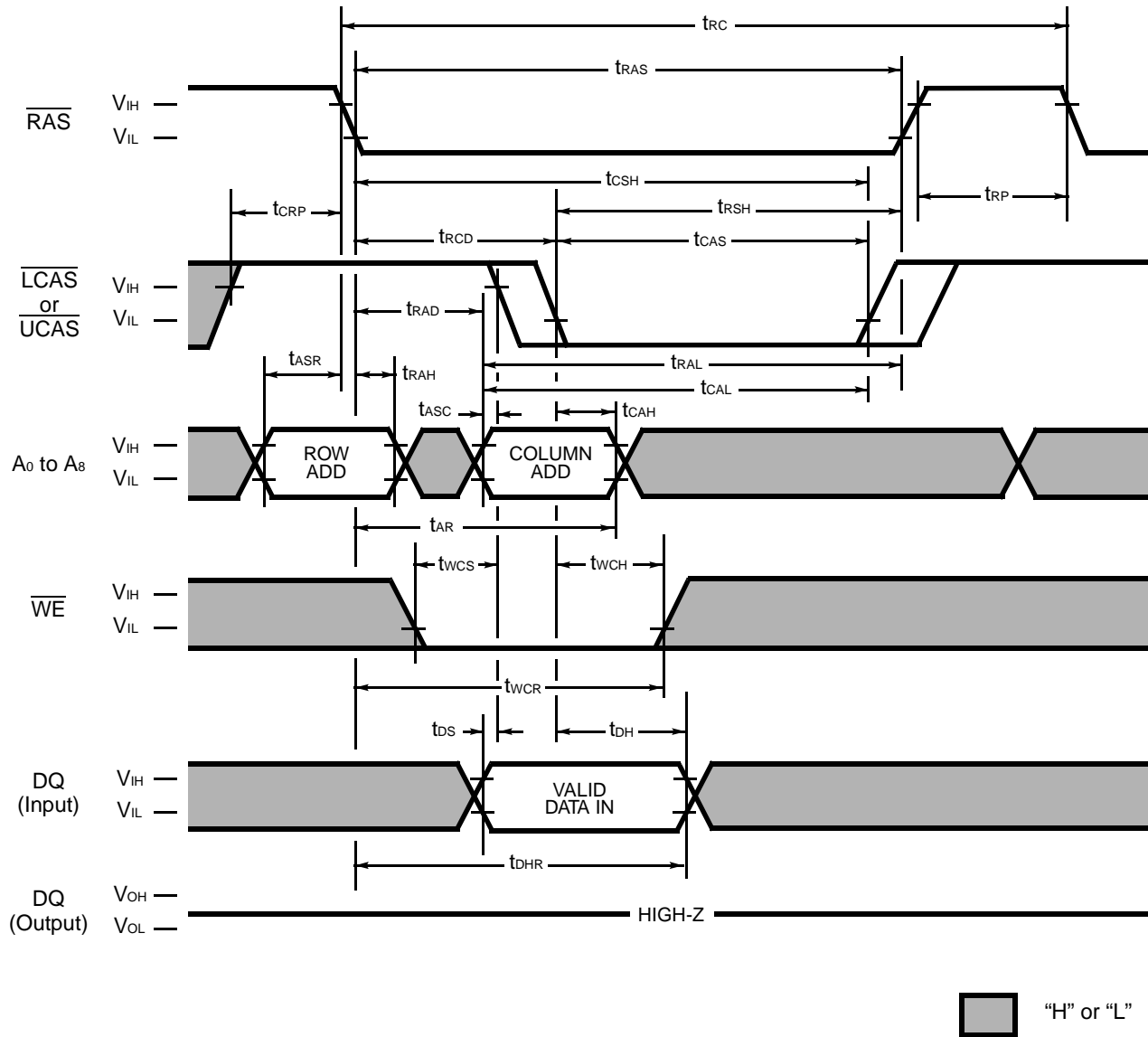
If $t_{RCD} > t_{RCD}(\max.)$, access time = t_{CAC} .

If $t_{RAD} > t_{RAD}(\max.)$, access time = t_{AA} .

If \overline{OE} is brought Low after t_{RC} , t_{CAC} , or t_{AA} (whichever occurs later), access time = t_{OE} .

However, if either $\overline{LCAS}/\overline{UCAS}$ or \overline{OE} goes High, the output returns to a high-impedance state after t_{OH} is satisfied.

MB814260-60/MB814260-70

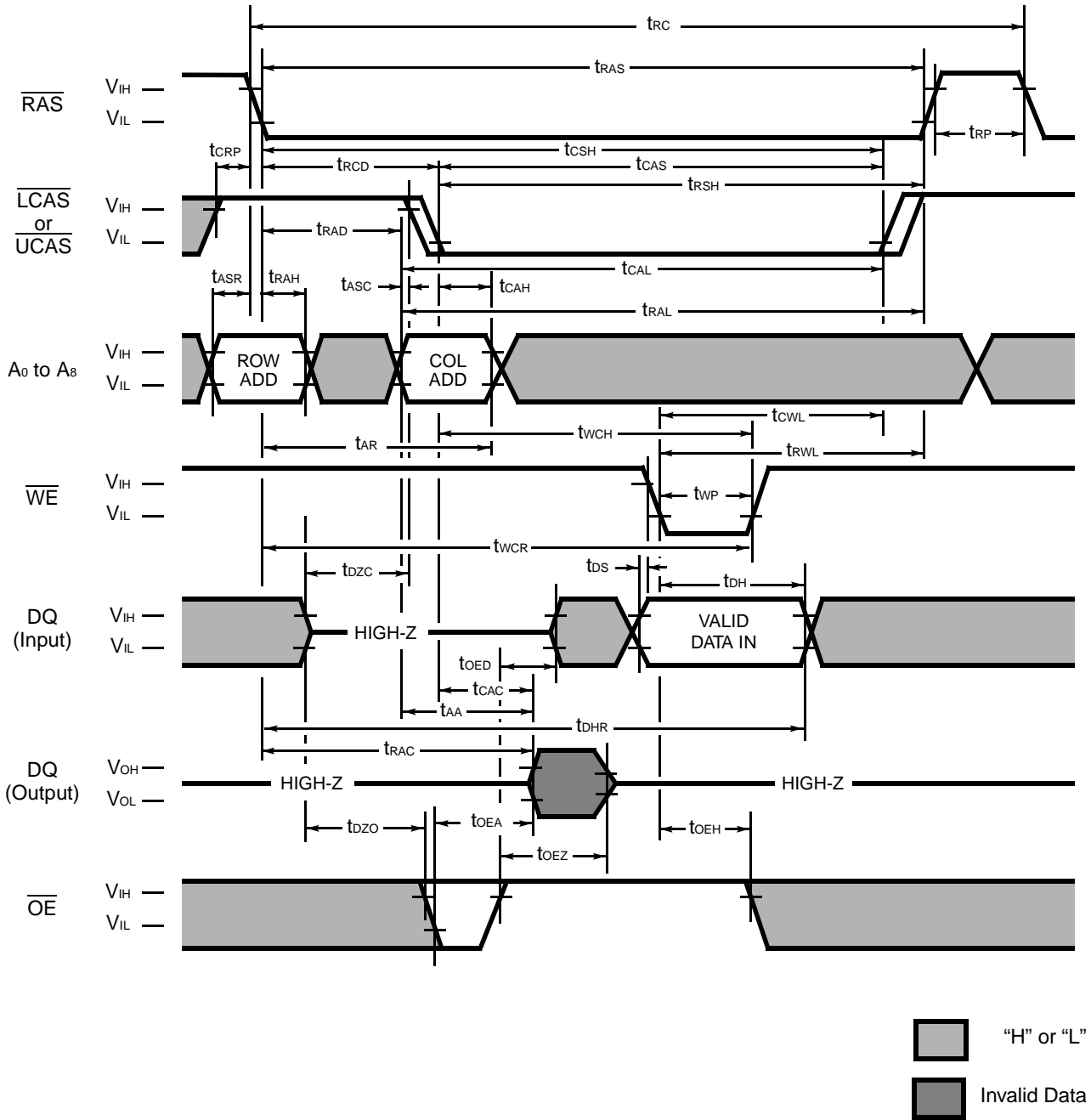
Fig. 6 - EARLY WRITE CYCLE ($\overline{OE} = \text{"H" or "L"}$)

DESCRIPTION

A write cycle is similar to a read cycle except \overline{WE} is set to a Low state and \overline{OE} is an "H" or "L" signal. A write cycle can be implemented in either of three ways – early write, \overline{OE} write (delayed write), or read-modify-write. During all write cycles, timing parameters t_{RWL} , t_{CWL} , t_{RAL} and t_{CAL} must be satisfied. In the early write cycle shown above t_{WCS} satisfied, data on the DQ pins are latched with the falling edge of LCAS or UCAS and written into memory.

MB814260-60/MB814260-70

Fig. 7 - \overline{OE} (DELAYED WRITE) CYCLE

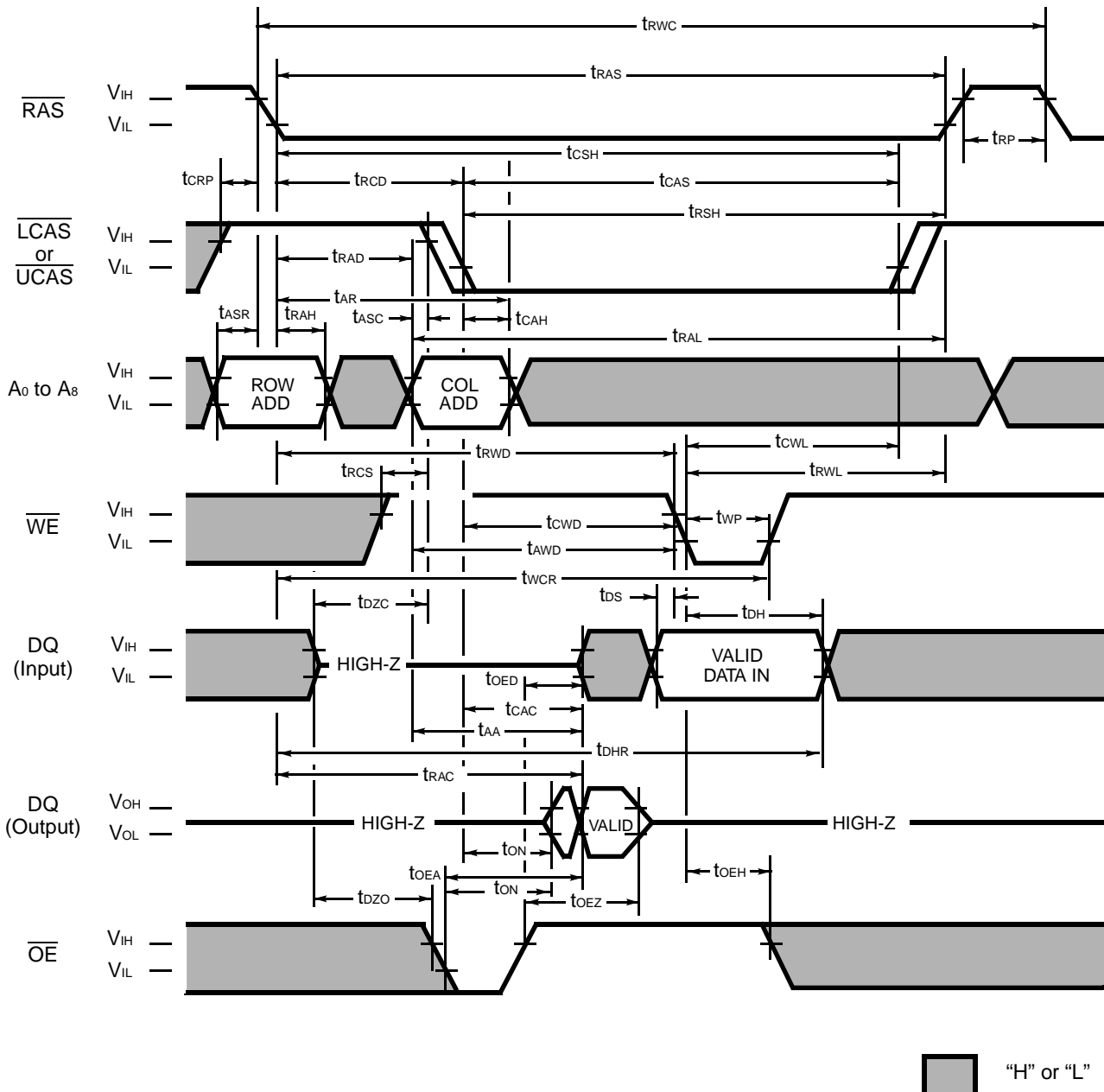


DESCRIPTION

In the \overline{OE} (delayed write) cycle, t_{WCS} is not satisfied; thus, the data on the DQ pins is latched with the falling edge of \overline{WE} and written into memory. The Output Enable (\overline{OE}) signal must be changed from Low to High before \overline{WE} goes Low ($t_{OED} + t_r + t_{DS}$).

MB814260-60/MB814260-70

Fig. 8 - READ-MODIFY-WRITE CYCLE

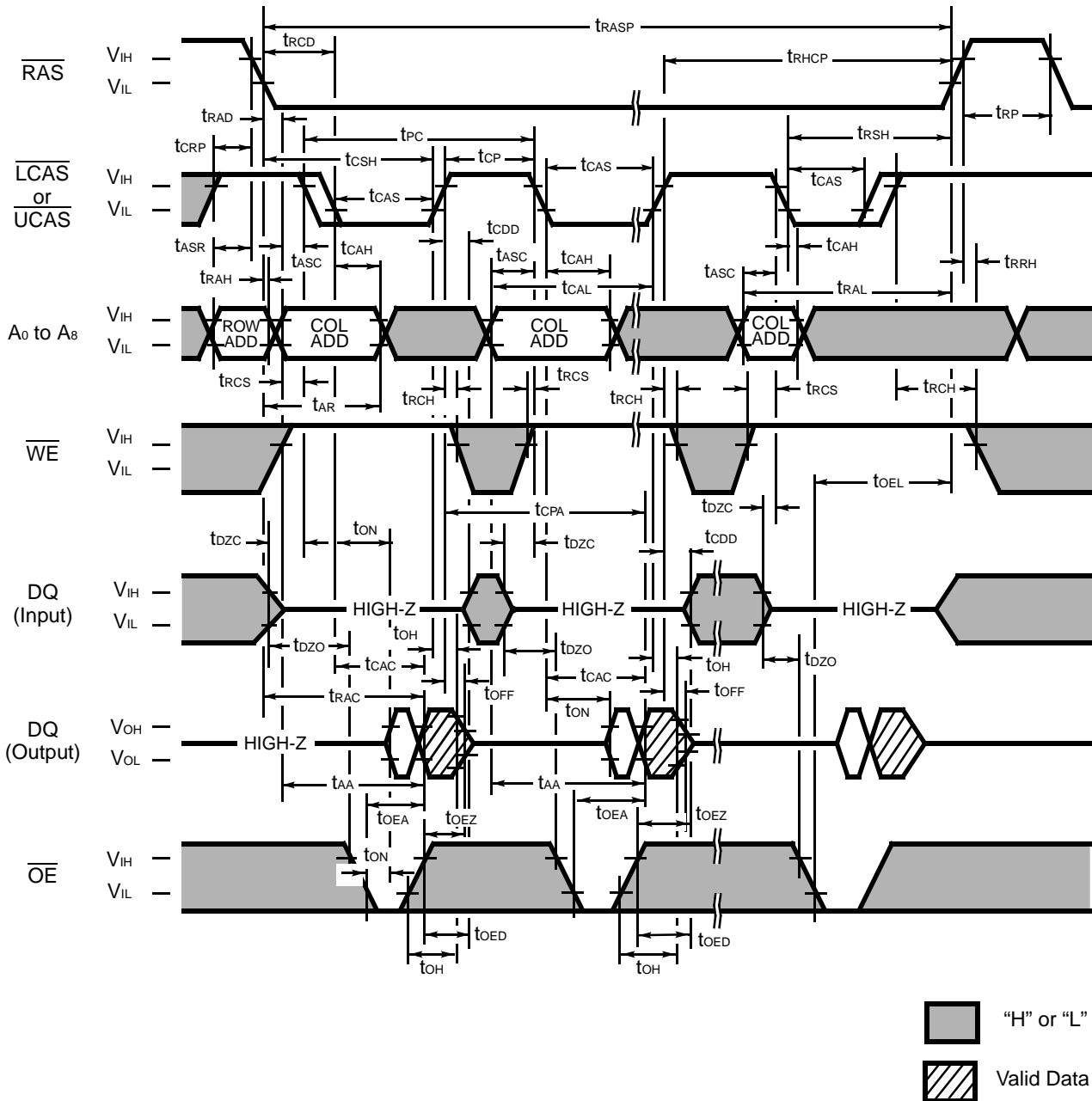


DESCRIPTION

The read-modify-write cycle is executed by changing \overline{WE} from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, \overline{OE} must be changed from Low to High after the memory access time.

MB814260-60/MB814260-70

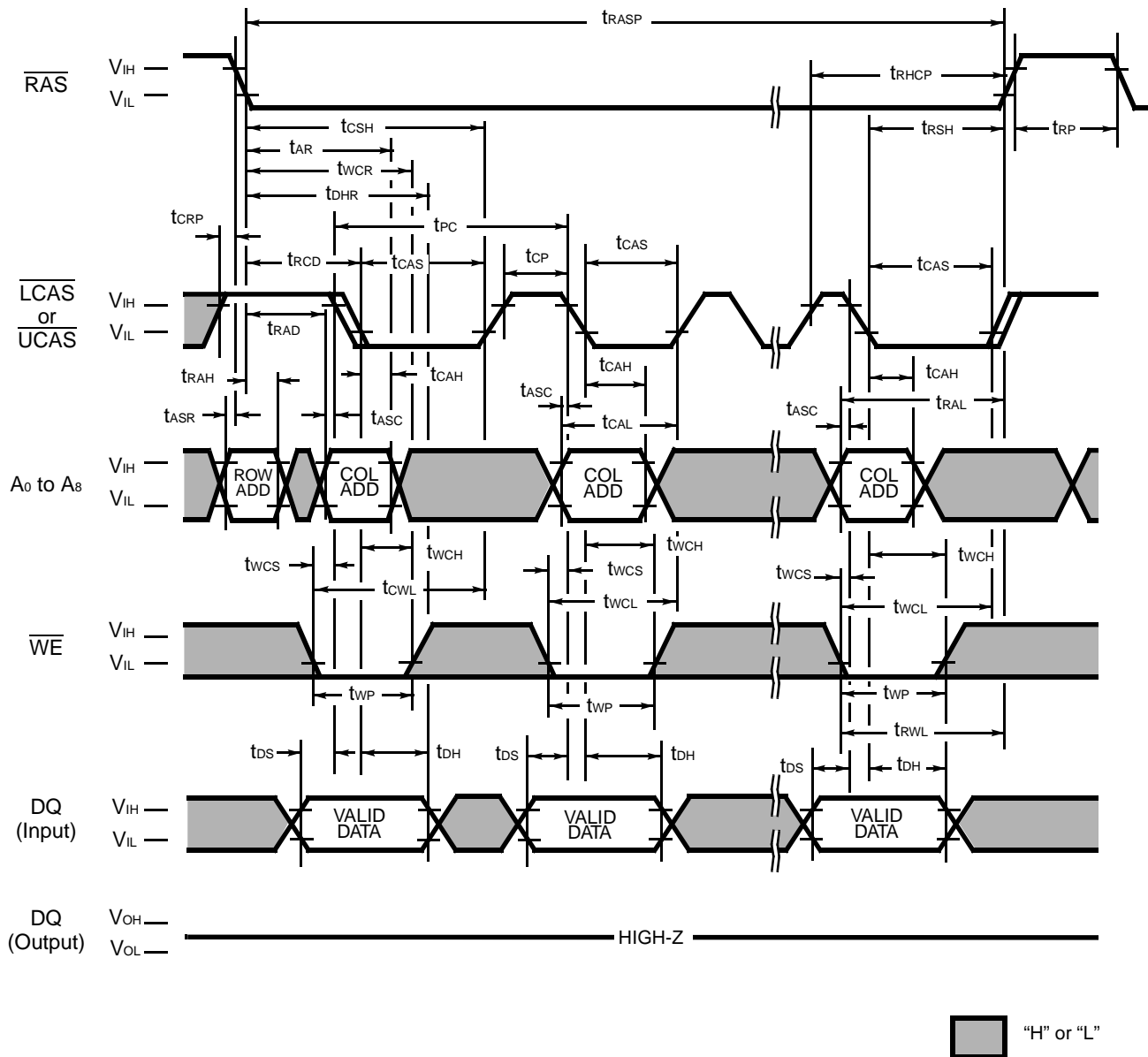
Fig. 9 – FAST PAGE MODE READ CYCLE



DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining \overline{RAS} at a Low level and \overline{WE} at a High level during all successive memory cycles in which the row address is latched. The access time is determined by t_{CAC} , t_{AA} , t_{CPA} , or t_{OEA} , whichever one is the latest in occurring.

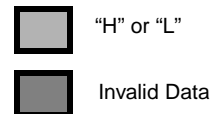
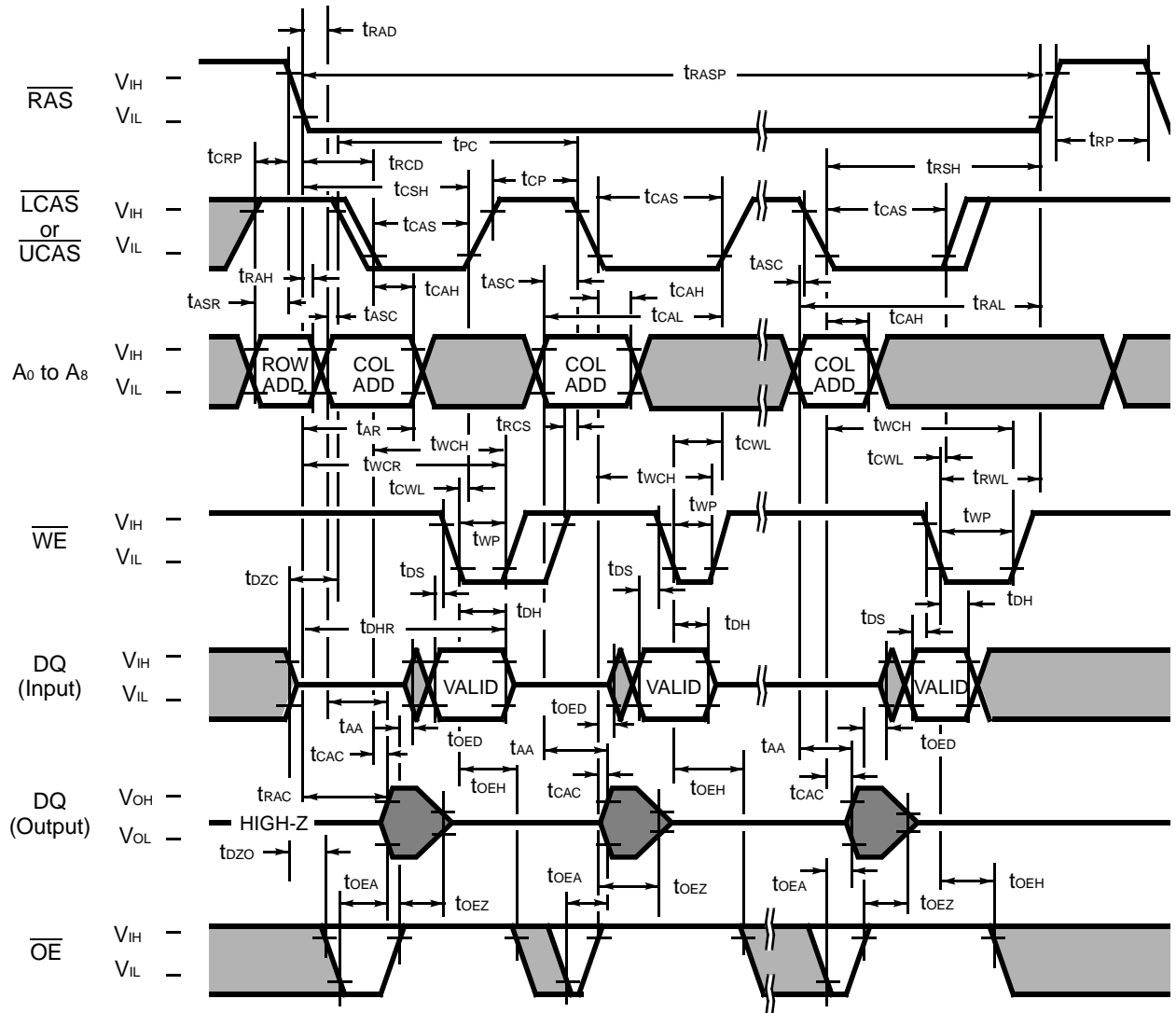
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Fig. 10 - FAST PAGE MODE WRITE CYCLE (\overline{OE} = "H" or "L")

DESCRIPTION

The fast page mode write cycle is executed in the same manner as the fast page mode read cycle except the states of \overline{WE} and \overline{OE} are reversed. Data appearing on the DQ₁ to DQ₈ is latched on the falling edge of LCAS and one appearing on the DQ₉ to DQ₁₆ is latched on the falling edge of UCAS and the data is written into the memory. During the fast page mode write cycle, including the delayed (\overline{OE}) write and read-modify-write cycles, t_{WCL} must be satisfied.

MB814260-60/MB814260-70

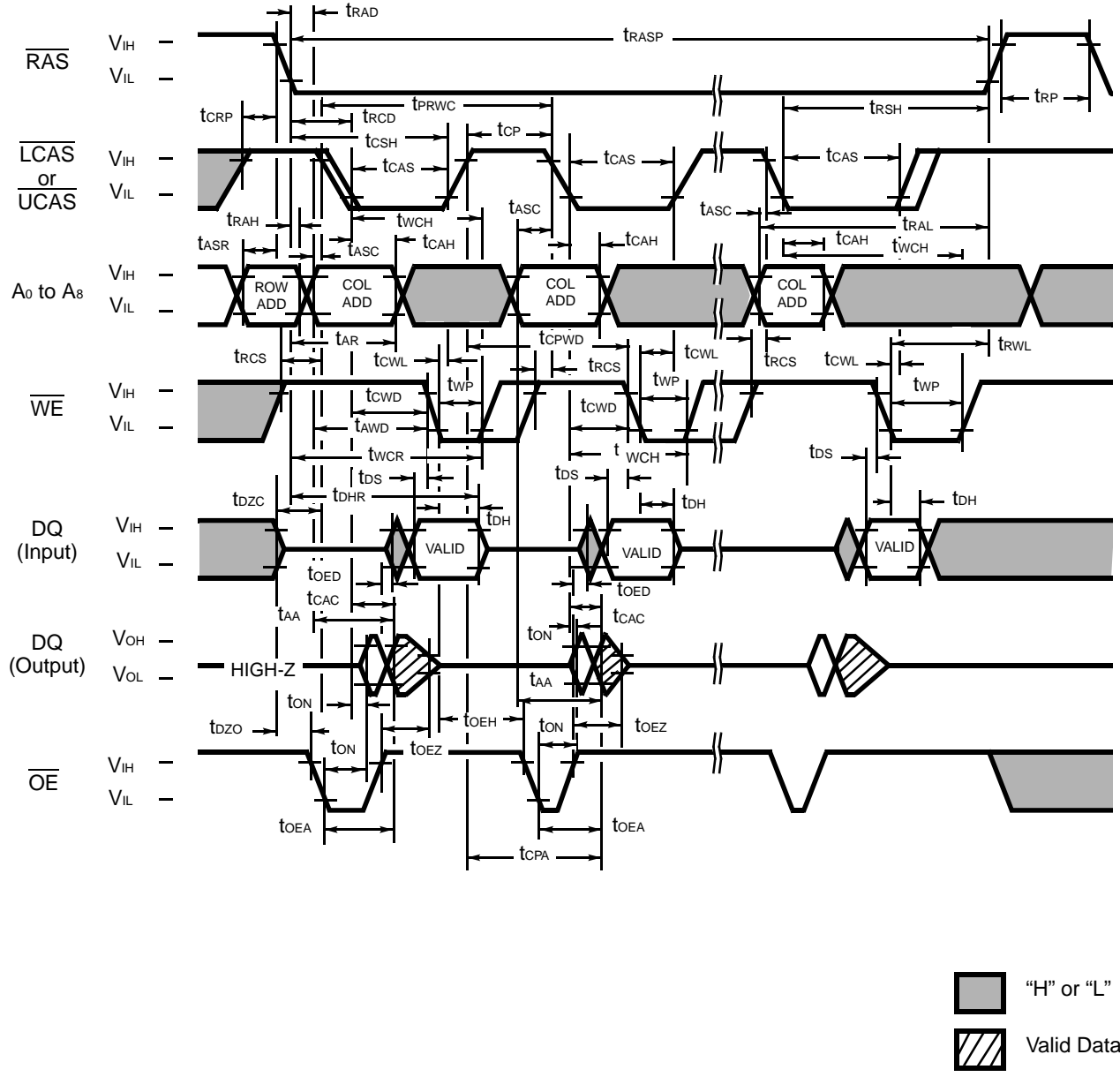
Fig. 11 - FAST PAGE MODE $\overline{\text{OE}}$ WRITE CYCLE

DESCRIPTION

The fast page mode $\overline{\text{OE}}$ (delayed) write cycle is executed in the same manner as the fast page mode write cycle except for the states of $\overline{\text{WE}}$ and $\overline{\text{OE}}$. Input data on the DQ pins are latched on the falling edge of $\overline{\text{WE}}$ and written into memory. In the fast page mode delayed write cycle, $\overline{\text{OE}}$ must be changed from Low to High before $\overline{\text{WE}}$ goes Low ($t_{\text{OED}} + t_r + t_{\text{DS}}$).

MB814260-60/MB814260-70

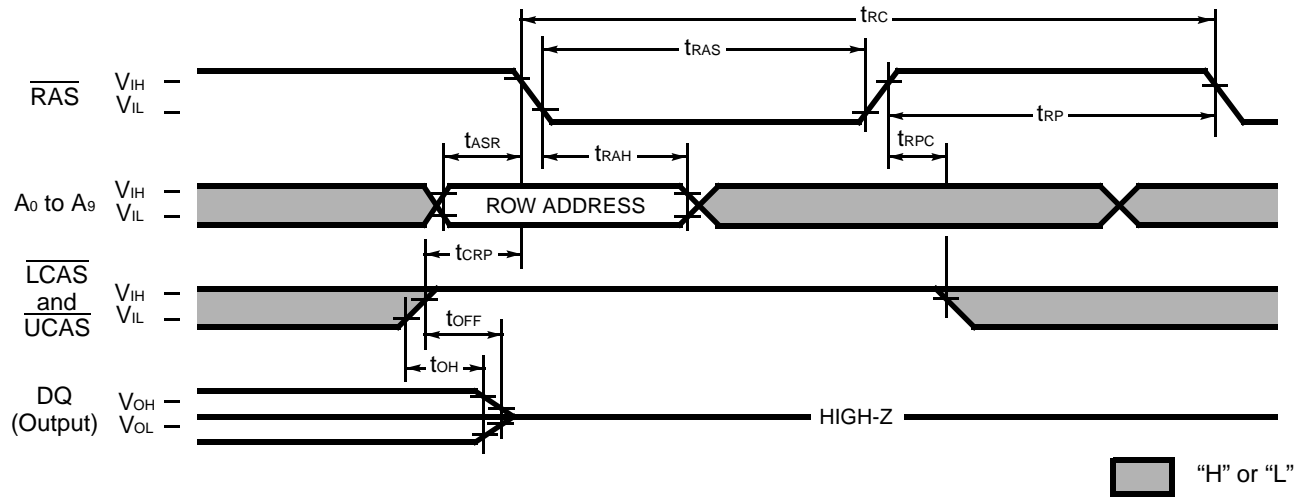
Fig. 12 – FAST PAGE MODE READ-MODIFY-WRITE CYCLE



DESCRIPTION

During fast page mode of operation, the read-modify-write cycle can be executed by switching $\overline{\text{WE}}$ from High to Low after input date appears at the DQ pins during a normal cycle.

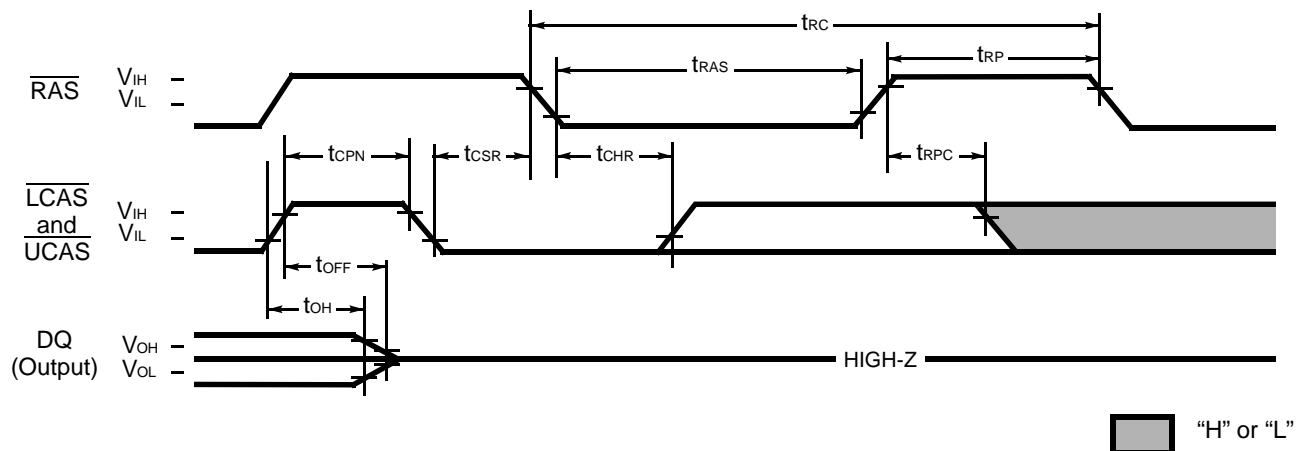
MB814260-60/MB814260-70

Fig. 13 - $\overline{\text{RAS}}$ -ONLY REFRESH ($\overline{\text{WE}} = \overline{\text{OE}} = \text{"H" or "L"}$)

DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2-milliseconds. Three refresh modes are available: $\overline{\text{RAS}}$ -only refresh, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, and hidden refresh.

$\overline{\text{RAS}}$ -only refresh is performed by keeping $\overline{\text{RAS}}$ Low and $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{\text{RAS}}$. During $\overline{\text{RAS}}$ -only refresh, DQ pins are kept in a high-impedance state.

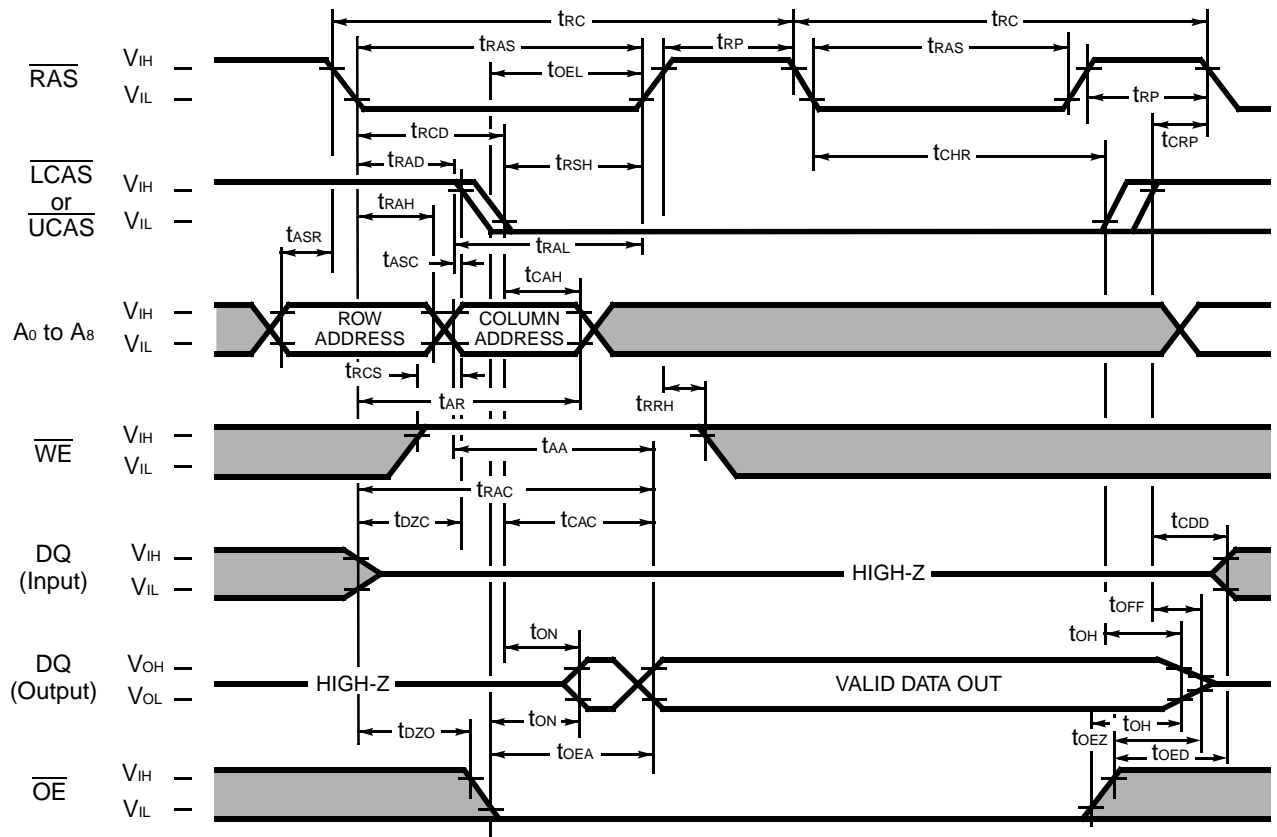
Fig. 14 - $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ REFRESH (ADDRESSES = $\overline{\text{WE}} = \overline{\text{OE}} = \text{"H" or "L"}$)

DESCRIPTION

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ is held Low for the specified setup time (t_{CSR}) before $\overline{\text{RAS}}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh operation.

MB814260-60/MB814260-70

Fig. 15 - HIDDEN REFRESH CYCLE



■ "H" or "L"

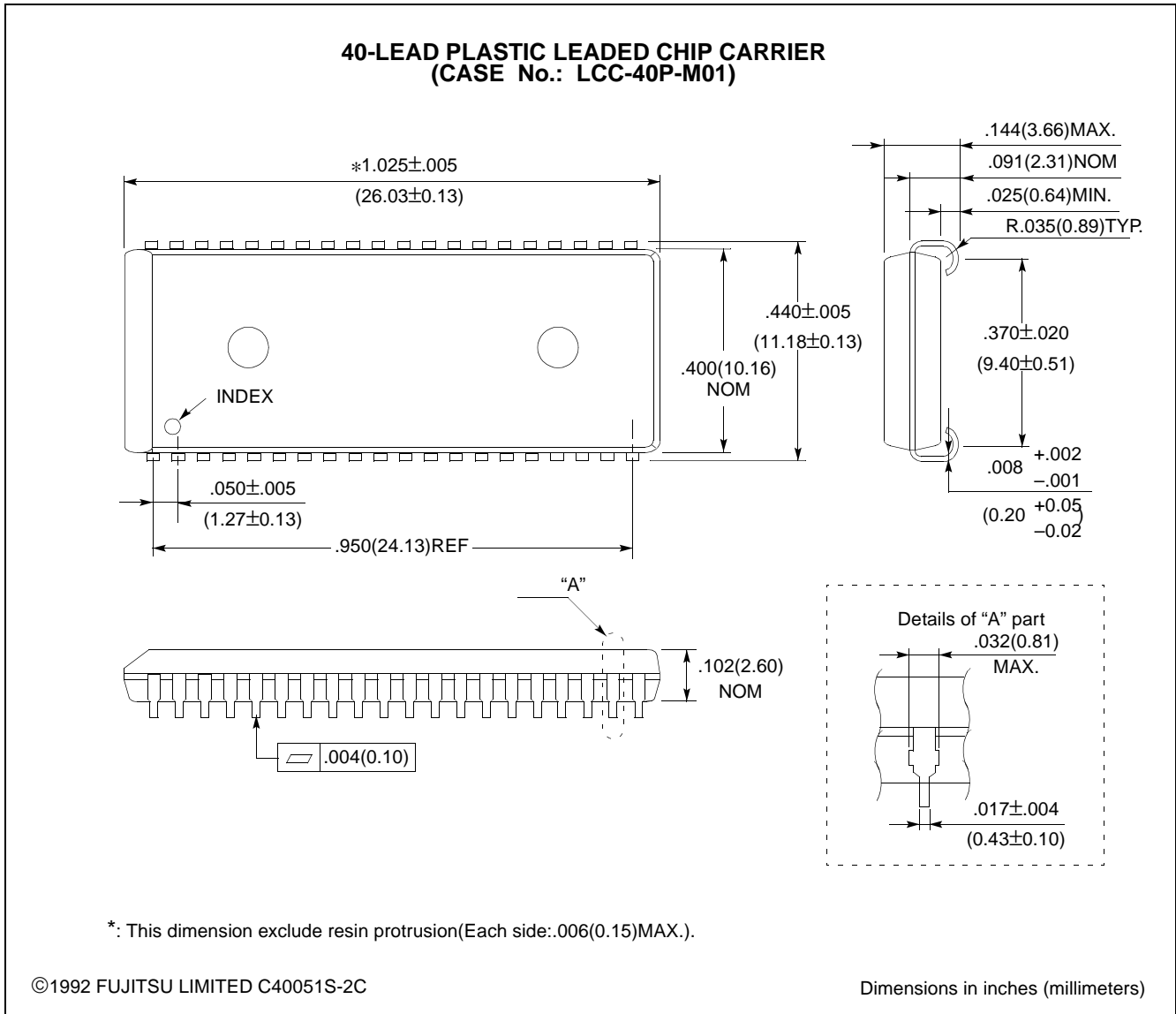
DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of \overline{LCAS} or \overline{UCAS} and cycling RAS. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have \overline{CAS} -before- \overline{RAS} refresh capability.

MB814260-60/MB814260-70

■ PACKAGE DIMENSIONS

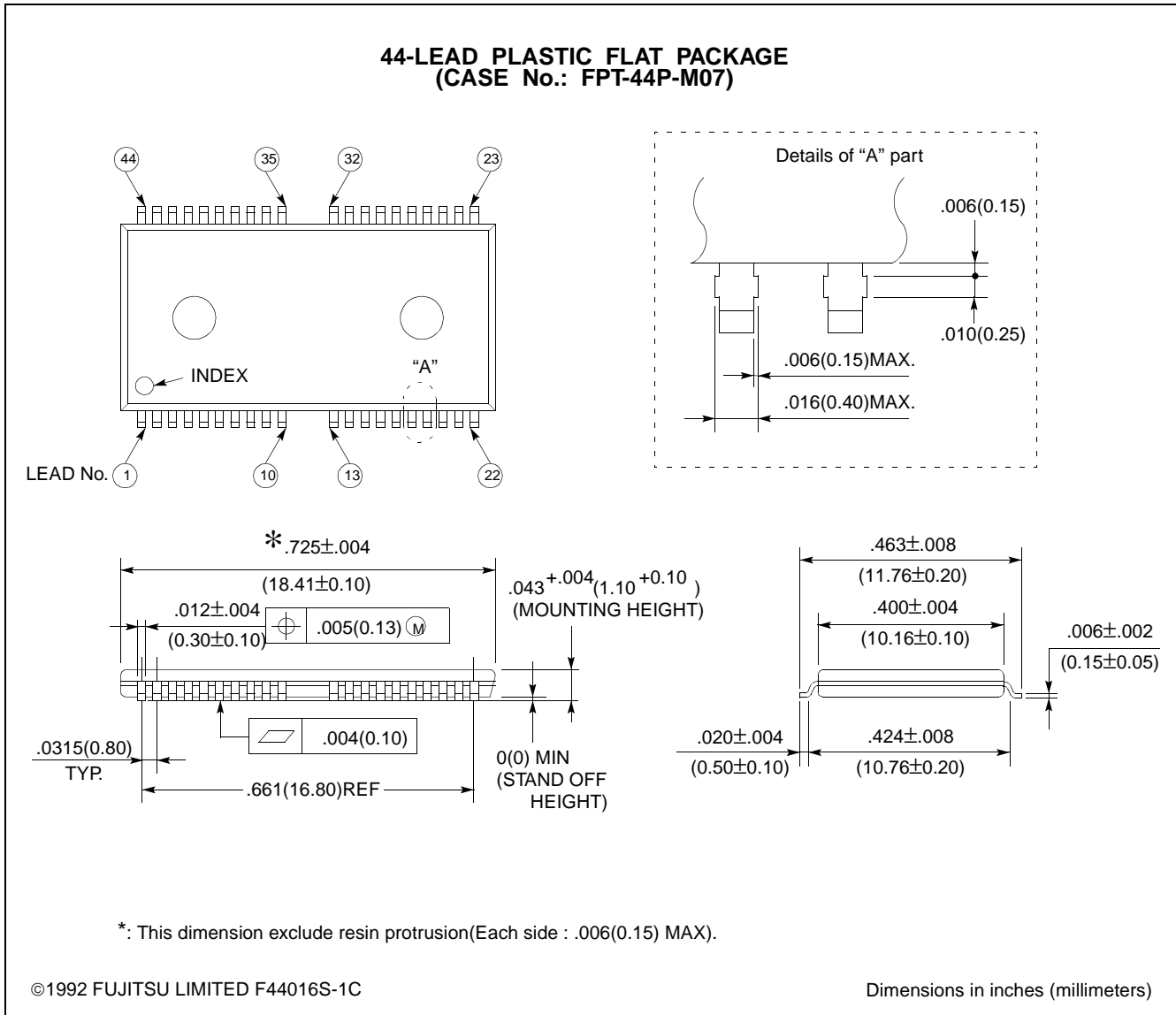
(Suffix: -PJ)



MB814260-60/MB814260-70

■ PACKAGE DIMENSIONS (Continued)

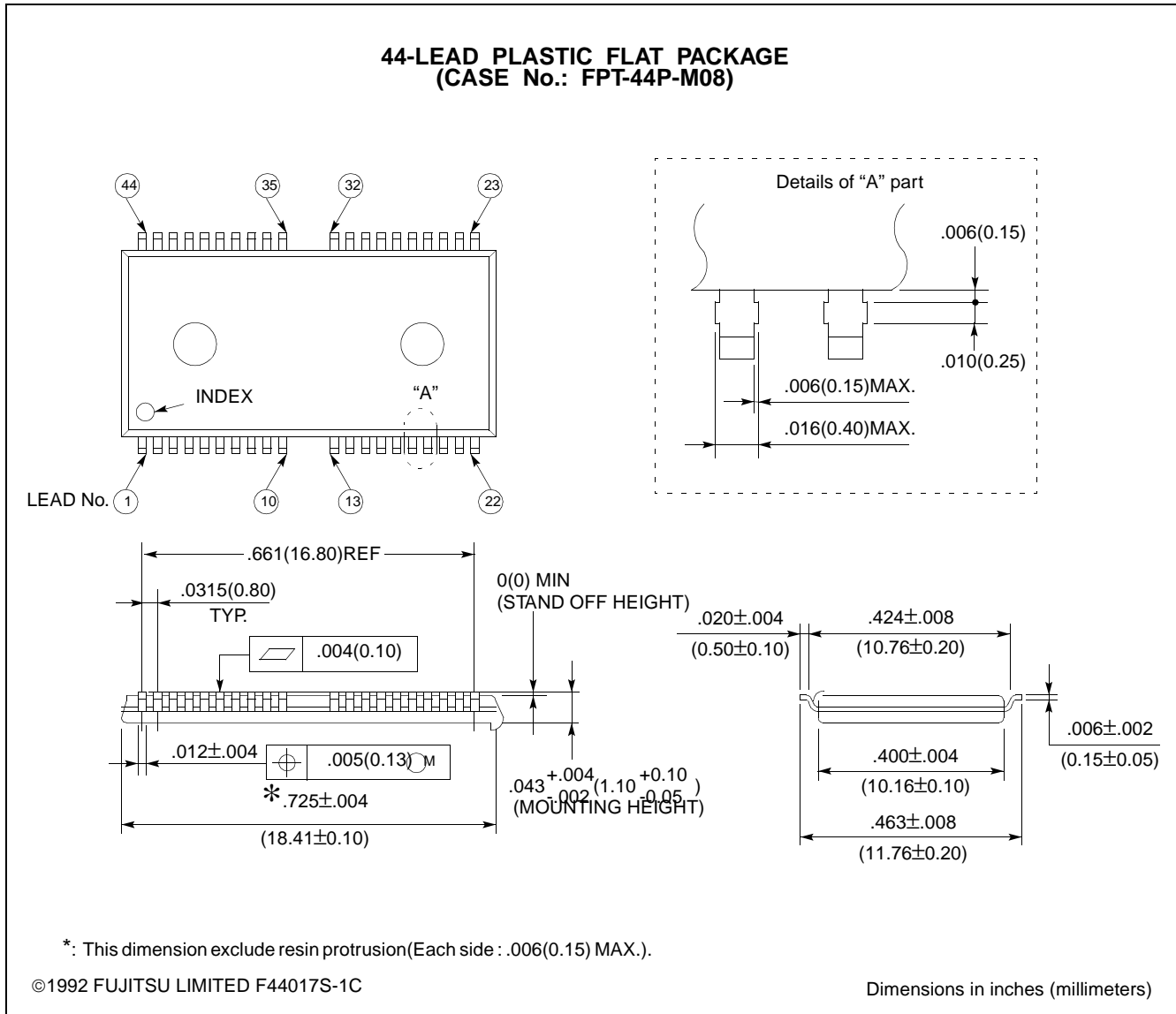
(Suffix: -PFTN)



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■ PACKAGE DIMENSIONS (Continued)

(Suffix: -PFTR)



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