



CMOS Static RAM 16K (2K x 8-Bit)

IDT6116SA
IDT6116LA

Features

- ◆ High-speed access and chip select times
 - Military: 20/25/35/45/55/70/90/120/150ns (max.)
 - Industrial: 20/25/35/45ns (max.)
 - Commercial: 15/20/25/35/45ns (max.)
- ◆ Low-power consumption
- ◆ Battery backup operation
 - 2V data retention voltage (LA version only)
- ◆ Produced with advanced CMOS high-performance technology
- ◆ CMOS process virtually eliminates alpha particle soft-error rates
- ◆ Input and output directly TTL-compatible
- ◆ Static operation: no clocks or refresh required
- ◆ Available in ceramic and plastic 24-pin DIP, 24-pin Thin Dip, 24-pin SOIC and 24-pin SOJ
- ◆ Military product compliant to MIL-STD-883, Class B

Description

The IDT6116SA/LA is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

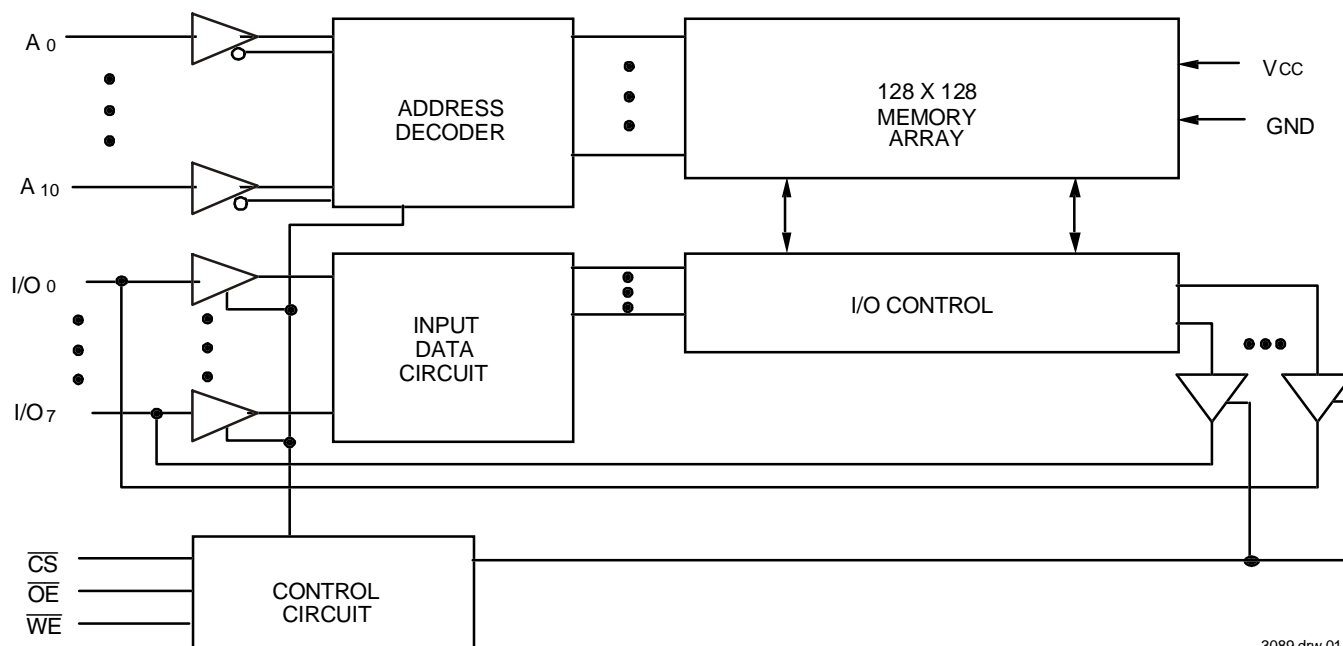
Access times as fast as 15ns are available. The circuit also offers a reduced power standby mode. When \overline{CS} goes HIGH, the circuit will automatically go to, and remain in, a standby power mode, as long as \overline{CS} remains HIGH. This capability provides significant system level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1 μ W to 4 μ W operating off a 2V battery.

All inputs and outputs of the IDT6116SA/LA are TTL-compatible. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT6116SA/LA is packaged in 24-pin 600 and 300 mil plastic or ceramic DIP, 24-lead gull-wing SOIC, and 24-lead J-bend SOJ providing high board-level packing densities.

Military grade product is manufactured in compliance to the latest version of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

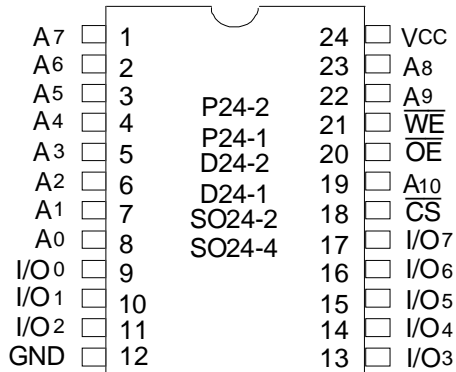
Functional Block Diagram



3089 drw 01

FEBRUARY 2001

Pin Configurations



3089 drw 02

DIP/SOIC/SOJ Top View

Pin Description

| Name | Description |
|-------------------------------------|-------------------|
| A ₀ - A ₁₀ | Address Inputs |
| I/O ₀ - I/O ₇ | Data Input/Output |
| \overline{CS} | Chip Select |
| \overline{WE} | Write Enable |
| \overline{OE} | Output Enable |
| V _{CC} | Power |
| GND | Ground |

3089 tbl 01

Truth Table⁽¹⁾

| Mode | \overline{CS} | \overline{OE} | \overline{WE} | I/O |
|---------|-----------------|-----------------|-----------------|---------------------|
| Standby | H | X | X | High-Z |
| Read | L | L | H | DATA _{OUT} |
| Read | L | H | H | High-Z |
| Write | L | X | L | DATA _{IN} |

3089 tbl 02

NOTE:

1. H = V_{IH}, L = V_{IL}, X = Don't Care.

Capacitance (T_A = +25°C, f = 1.0 MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|-----------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 8 | pF |
| C _{VO} | I/O Capacitance | V _{OUT} = 0V | 8 | pF |

3089 tbl 03

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

Absolute Maximum Ratings⁽¹⁾

| Symbol | Rating | Com'l. | Mil. | Unit |
|----------------------------------|--------------------------------------|--------------|--------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +7.0 | -0.5 to +7.0 | V |
| T _A | Operating Temperature | 0 to +70 | -55 to +125 | °C |
| T _{BIAS} | Temperature Under Bias | -55 to +125 | -65 to +135 | °C |
| T _{STG} | Storage Temperature | -55 to +125 | -65 to +150 | °C |
| P _T | Power Dissipation | 1.0 | 1.0 | W |
| I _{OUT} | DC Output Current | 50 | 50 | mA |

3089 tbl 04

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} +0.5V.

Recommended Operating Temperature and Supply Voltage

| Grade | Ambient Temperature | GND | V _{CC} |
|------------|---------------------|-----|-----------------|
| Military | -55°C to +125°C | 0V | 5.0V ± 10% |
| Industrial | -45°C to +85°C | 0V | 5.0V ± 10% |
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |

3089 tbl 05

Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------|--------------------|---------------------|------|-----------------------|------|
| V _{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 ⁽²⁾ | V |
| GND | Ground | 0 | 0 | 0 | V |
| V _{IH} | Input High Voltage | 2.2 | 3.5 | V _{CC} + 0.5 | V |
| V _{IL} | Input Low Voltage | -0.5 ⁽¹⁾ | — | 0.8 | V |

3089 tbl 06

NOTES:

- V_{IL} (min.) = -3.0V for pulse width less than 20ns, once per cycle.
- V_{IH} must not exceed V_{CC} + 0.5V.

DC Electrical Characteristics

(V_{CC} = 5.0V ± 10%)

| Symbol | Parameter | Test Conditions | IDT6116SA | | IDT6116LA | | Unit | |
|-----------------|------------------------|--|----------------|------|-----------|------|------|----|
| | | | Min. | Max. | Min. | Max. | | |
| I _I | Input Leakage Current | V _{CC} = Max., V _{IN} = GND to V _{CC} | MIL. COM'L. | — | 10 | — | 5 | μA |
| | | | | — | 5 | — | 2 | |
| I _O | Output Leakage Current | V _{CC} = Max., \overline{CS} = V _{IH} , V _{OUT} = GND to V _{CC} | MIL. COM'L. | — | 10 | — | 5 | μA |
| | | | | — | 5 | — | 2 | |
| V _{OL} | Output Low Voltage | I _{OL} = 8mA, V _{CC} = Min. | — | 0.4 | — | 0.4 | V | |
| V _{OH} | Output High Voltage | I _{OH} = -4mA, V _{CC} = Min. | 2.4 | — | 2.4 | — | V | |

3089 tbl 07

DC Electrical Characteristics⁽¹⁾

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

| Symbol | Parameter | Power | 6116SA15 | 6116SA20 6116LA20 | | 6116SA25 6116LA25 | | 6116SA35 6116LA35 | | Unit |
|------------------|---|-------|---------------|----------------------|-----|----------------------|-----|----------------------|-----|------|
| | | | Com'l Only | Com'l & Ind | Mil | Com'l & Ind | Mil | Com'l. & Ind. | Mil | |
| I _{CC1} | Operating Power Supply Current CS ≤ V _{IL} , Outputs Open V _{CC} = Max., f = 0 | SA | 105 | 105 | 130 | 80 | 90 | 80 | 90 | mA |
| | | LA | 95 | 95 | 120 | 75 | 85 | 75 | 85 | |
| I _{CC2} | Dynamic Operating Current CS ≤ V _{IL} , Outputs Open V _{CC} = Max., f = f _{MAX} ⁽²⁾ | SA | 150 | 130 | 150 | 120 | 135 | 100 | 115 | mA |
| | | LA | 140 | 120 | 140 | 110 | 125 | 95 | 105 | |
| I _{SB} | Standby Power Supply Current (TTL Level) CS ≥ V _{IH} , Outputs Open V _{CC} = Max., f = f _{MAX} ⁽²⁾ | SA | 40 | 40 | 50 | 40 | 45 | 25 | 35 | mA |
| | | LA | 35 | 35 | 45 | 35 | 40 | 25 | 30 | |
| I _{SB1} | Full Standby Power Supply Current (CMOS Level) CS ≥ V _{HC} , V _{CC} = Max., V _{IN} ≤ V _{LC} or V _{IN} ≥ V _{HC} , f = 0 | SA | 2 | 2 | 10 | 2 | 10 | 2 | 10 | mA |
| | | LA | 0.1 | 0.1 | 0.9 | 0.1 | 0.9 | 0.1 | 0.9 | |

3089 tbl 08

NOTES:

- All values are maximum guaranteed values.
- f_{MAX} = 1/TRC, only address inputs are cycling at f_{MAX}, f = 0 means address inputs are not changing.

DC Electrical Characteristics⁽¹⁾ (continued)
(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

| Symbol | Parameter | Power | 6116SA45 6116LA45 | | 6116SA55 6116LA55 | 6116SA70 6116LA70 | 6116SA90 6116LA90 | 6116SA120 6116LA120 | 6116SA150 6116LA150 | Unit |
|------------------|---|-------|----------------------|-----|----------------------|----------------------|----------------------|------------------------|------------------------|------|
| | | | Com'l & Ind | Mil | Mil Only | Mil Only | Mil Only | Mil Only | Mil Only | |
| I _{CC1} | Operating Power Supply Current, $\overline{CS} \leq V_{IL}$, Outputs Open V _{CC} = Max., f = 0 | SA | 80 | 90 | 90 | 90 | 90 | 90 | 90 | mA |
| | | LA | 75 | 85 | 85 | 85 | 85 | 85 | 85 | |
| I _{CC2} | Dynamic Operating Current, $\overline{CS} \leq V_{IL}$, Outputs Open V _{CC} = Max., f = f _{MAX} ⁽²⁾ | SA | 100 | 100 | 100 | 100 | 100 | 100 | 90 | mA |
| | | LA | 90 | 95 | 90 | 90 | 85 | 85 | 85 | |
| I _{SB} | Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open V _{CC} = Max., f = f _{MAX} ⁽²⁾ | SA | 25 | 25 | 25 | 25 | 25 | 25 | 25 | mA |
| | | LA | 20 | 20 | 20 | 20 | 25 | 15 | 15 | |
| I _{SB1} | Full Standby Power Supply Current (CMOS Level), $\overline{CS} \geq V_{HC}$, V _{CC} = Max., V _{IN} ≤ V _{LC} or V _{IN} ≥ V _{HC} , f = 0 | SA | 2 | 10 | 10 | 10 | 10 | 10 | 10 | mA |
| | | LA | 0.1 | 0.9 | 0.9 | 0.9 | 0.9 | 0.9 | 0.9 | |

3089 tbl 09

NOTES:

- All values are maximum guaranteed values.
- f_{MAX} = 1/trc, only address inputs are toggling at f_{MAX}, f = 0 means address inputs are not changing.

Data Retention Characteristics Over All Temperature Ranges
(LA Version Only) (V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

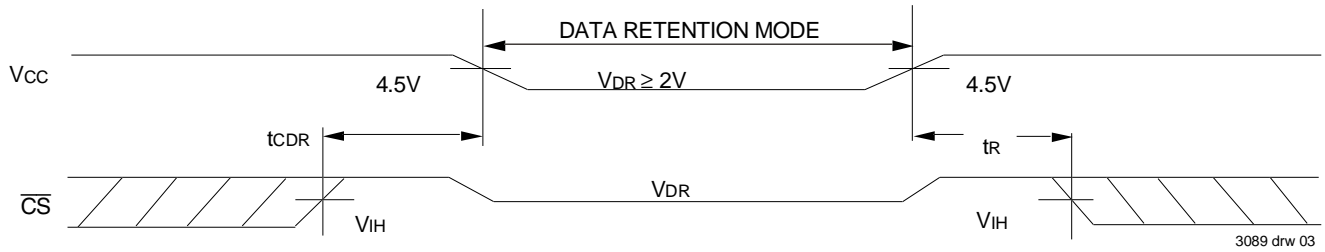
| Symbol | Parameter | Test Condition | Min. | Typ. ⁽¹⁾ V _{CC} @ | | Max. V _{CC} @ | | Unit |
|---------------------------------|--------------------------------------|---|--------------------------------|--|------|---------------------------|------|------|
| | | | | 2.0V | 3.0V | 2.0V | 3.0V | |
| V _{DR} | V _{CC} for Data Retention | — | 2.0 | — | — | — | — | V |
| I _{CCDR} | Data Retention Current | MIL. COM'L. | — | 0.5 | 1.5 | 200 | 300 | μA |
| | | | — | 0.5 | 1.5 | 20 | 30 | |
| t _{CDR} ⁽³⁾ | Chip Deselect to Data Retention Time | $\overline{CS} \geq V_{HC}$ V _{IN} ≥ V _{HC} or ≤ V _{LC} | — | 0 | — | — | — | ns |
| t _R ⁽³⁾ | Operation Recovery Time | | t _{RC} ⁽²⁾ | — | — | — | — | ns |
| I _{LIL} | Input Leakage Current | | — | — | — | 2 | 2 | μA |

3089 tbl 10

NOTES:

- T_A = + 25°C
- t_{RC} = Read Cycle Time.
- This parameter is guaranteed by device characterization, but is not production tested.

Low Vcc Data Retention Waveform



AC Test Conditions

| | |
|-------------------------------|---------------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 5ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| AC Test Load | See Figures 1 and 2 |

3089 tbl 11

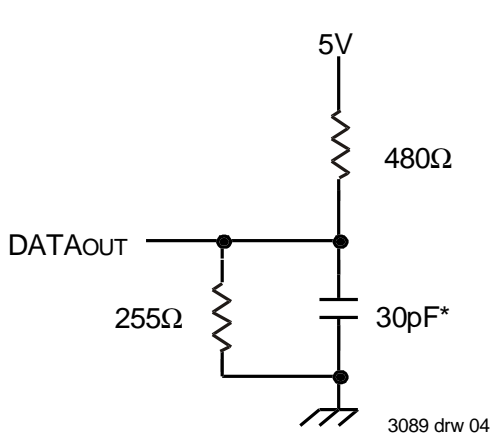


Figure 1. AC Test Load

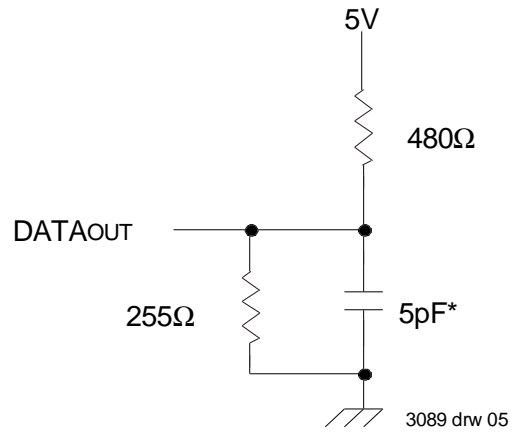


Figure 2. AC Test Load
(for tOLZ, tCLZ, tOHZ, tWHZ, tCHZ & tOW)

*Including scope and jig.

AC Electrical Characteristics (Vcc = 5V ± 10%, All Temperature Ranges)

| Symbol | Parameter | 6116SA15 ⁽¹⁾ | | 6116SA20 6116LA20 | | 6116SA25 6116LA25 | | 6116SA35 6116LA35 | | Unit |
|---------------------------------|------------------------------------|-------------------------|------|----------------------|------|----------------------|------|----------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | | | | | |
| t _{RC} | Read Cycle Time | 15 | — | 20 | — | 25 | — | 35 | — | ns |
| t _{AA} | Address Access Time | — | 15 | — | 19 | — | 25 | — | 35 | ns |
| t _{ACS} | Chip Select Access Time | — | 15 | — | 20 | — | 25 | — | 35 | ns |
| t _{CLZ} ⁽³⁾ | Chip Select to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{OE} | Output Enable to Output Valid | — | 10 | — | 10 | — | 13 | — | 20 | ns |
| t _{OLZ} ⁽³⁾ | Output Enable to Output in Low-Z | 0 | — | 0 | — | 5 | — | 5 | — | ns |
| t _{CHZ} ⁽³⁾ | Chip Deselect to Output in High-Z | — | 10 | — | 11 | — | 12 | — | 15 | ns |
| t _{OHZ} ⁽³⁾ | Output Disable to Output in High-Z | — | 8 | — | 8 | — | 10 | — | 13 | ns |
| t _{OH} | Output Hold from Address Change | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{PU} ⁽³⁾ | Chip Select to Power Up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{PD} ⁽³⁾ | Chip Deselect to Power Down Time | — | 15 | — | 20 | — | 25 | — | 35 | ns |

3089 tbl 12

AC Electrical Characteristics (Vcc = 5V ± 10%, All Temperature Ranges) (continued)

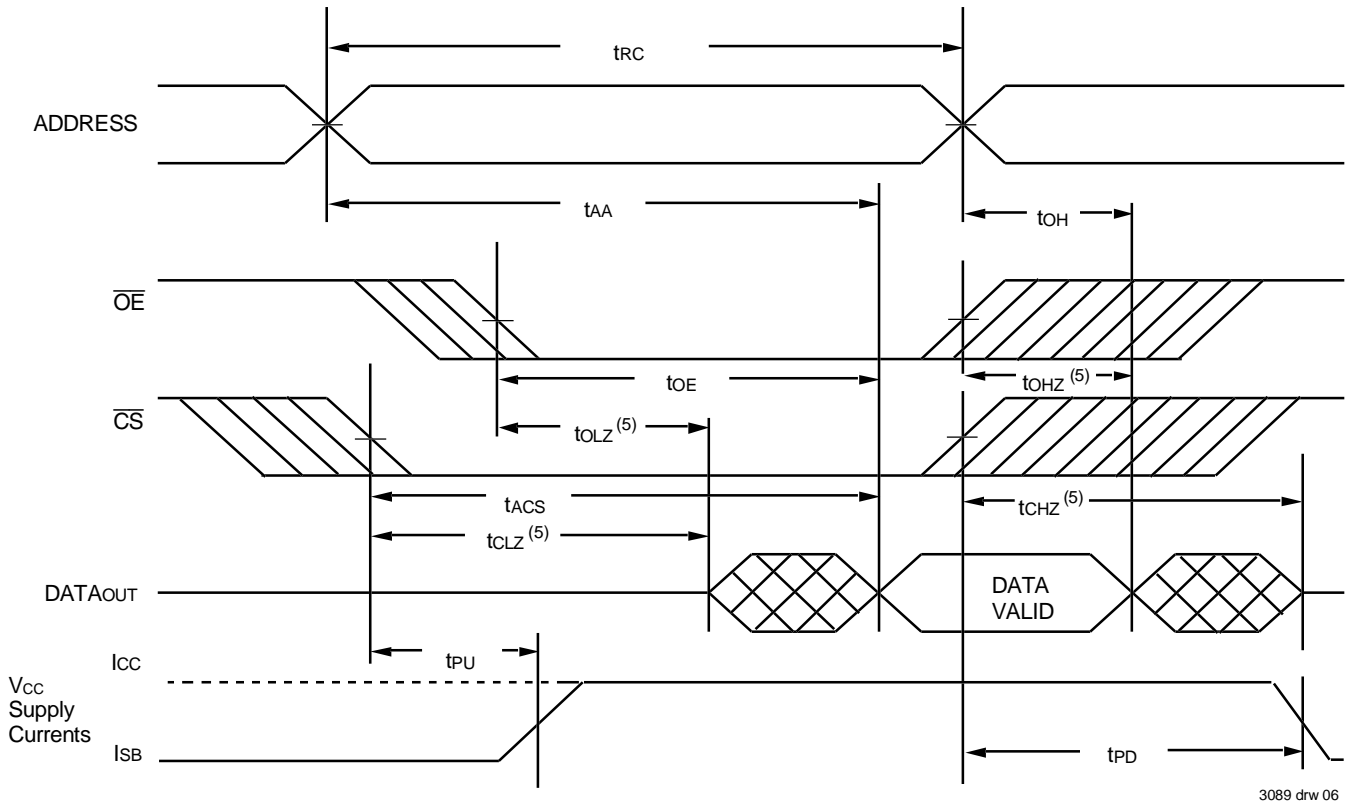
| Symbol | Parameter | 6116SA45 6116LA45 | | 6116SA55 ⁽²⁾ 6116LA55 ⁽²⁾ | | 6116SA70 ⁽²⁾ 6116LA70 ⁽²⁾ | | 6116SA90 ⁽²⁾ 6116LA90 ⁽²⁾ | | 6116SA120 ⁽²⁾ 6116LA120 ⁽²⁾ | | 6116SA150 ⁽²⁾ 6116LA150 ⁽²⁾ | | Unit |
|---------------------------------|------------------------------------|----------------------|------|--|------|--|------|--|------|--|------|--|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | | | | | | | | | |
| t _{RC} | Read Cycle Time | 45 | — | 55 | — | 70 | — | 90 | — | 120 | — | 150 | — | ns |
| t _{AA} | Address Access Time | — | 45 | — | 55 | — | 70 | — | 90 | — | 120 | — | 150 | ns |
| t _{ACS} | Chip Select Access Time | — | 45 | — | 50 | — | 65 | — | 90 | — | 120 | — | 150 | ns |
| t _{CLZ} ⁽³⁾ | Chip Select to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{OE} | Output Enable to Output Valid | — | 25 | — | 40 | — | 50 | — | 60 | — | 80 | — | 100 | ns |
| t _{OLZ} ⁽³⁾ | Output Enable to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{CHZ} ⁽³⁾ | Chip Deselect to Output in High-Z | — | 20 | — | 30 | — | 35 | — | 40 | — | 40 | — | 40 | ns |
| t _{OHZ} ⁽³⁾ | Output Disable to Output in High-Z | — | 15 | — | 30 | — | 35 | — | 40 | — | 40 | — | 40 | ns |
| t _{OH} | Output Hold from Address Change | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |

3089 tbl 13

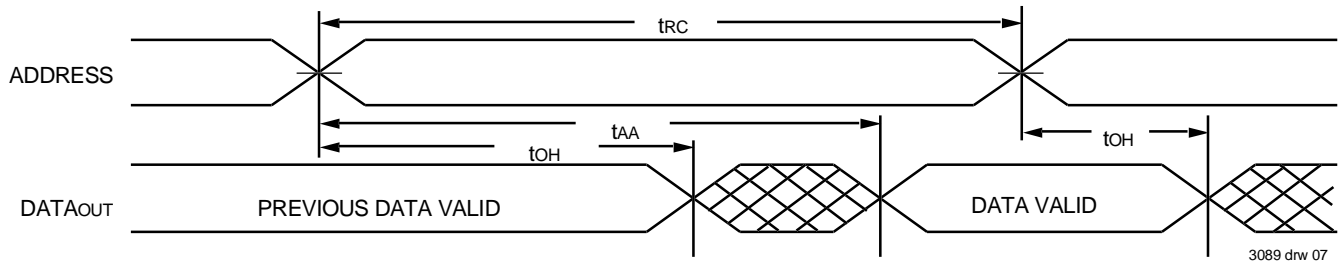
NOTES:

- 0°C to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- This parameter guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

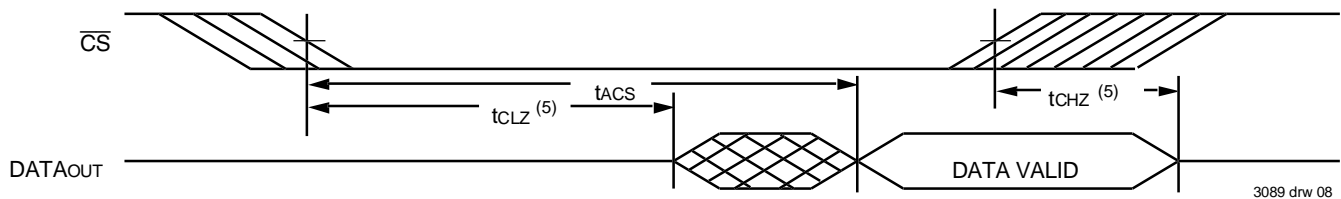
Timing Waveform of Read Cycle No. 1^(1,3)



Timing Waveform of Read Cycle No. 2^(1,2,4)



Timing Waveform of Read Cycle No. 3^(1,3,4)



NOTES:

1. \overline{WE} is HIGH for Read cycle.
2. Device is continuously selected, \overline{CS} is LOW.
3. Address valid prior to or coincident with \overline{CS} transition LOW.
4. \overline{OE} is LOW.
5. Transition is measured $\pm 500\text{mV}$ from steady state.

AC Electrical Characteristics (Vcc = 5V ± 10%, All Temperature Ranges)

| Symbol | Parameter | 6116SA15 ⁽¹⁾ | | 6116SA20 6116LA20 | | 6116SA25 6116LA25 | | 6116SA35 6116LA35 | | Unit |
|----------------------------------|---------------------------------|-------------------------|------|----------------------|------|----------------------|------|----------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Write Cycle | | | | | | | | | | |
| t _{WC} | Write Cycle Time | 15 | — | 20 | — | 25 | — | 35 | — | ns |
| t _{CW} | Chip Select to End-of-Write | 13 | — | 15 | — | 17 | — | 25 | — | ns |
| t _{AW} | Address Valid to End-of-Write | 14 | — | 15 | — | 17 | — | 25 | — | ns |
| t _{AS} | Address Set-up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{WP} | Write Pulse Width | 12 | — | 12 | — | 15 | — | 20 | — | ns |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{WHZ} ⁽³⁾ | Write to Output in High-Z | — | 7 | — | 8 | — | 16 | — | 20 | ns |
| t _{DW} | Data to Write Time Overlap | 12 | — | 12 | — | 13 | — | 15 | — | ns |
| t _{DH} ⁽⁴⁾ | Data Hold from Write Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{OW} ^(3,4) | Output Active from End-of-Write | 0 | — | 0 | — | 0 | — | 0 | — | ns |

3089 tbl 14

AC Electrical Characteristics (Vcc = 5V ± 10%, All Temperature Ranges) (continued)

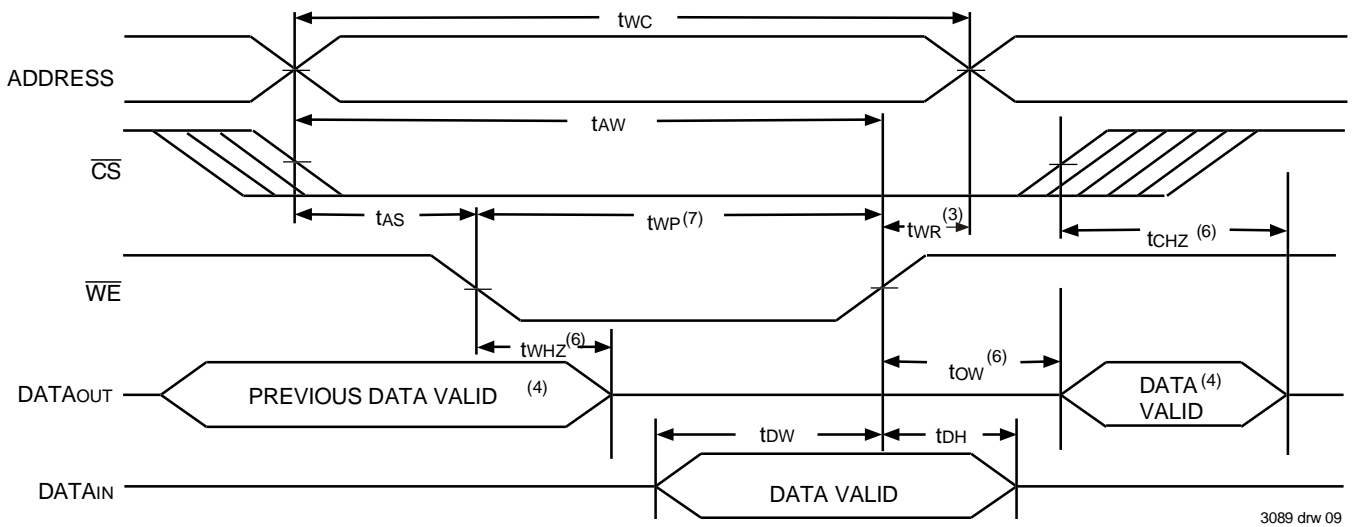
| Symbol | Parameter | 6116SA45 6116LA45 | | 6116SA55 ⁽²⁾ 6116LA55 ⁽²⁾ | | 6116SA70 ⁽²⁾ 6116LA70 ⁽²⁾ | | 6116SA90 ⁽²⁾ 6116LA90 ⁽²⁾ | | 6116SA120 ⁽²⁾ 6116LA120 ⁽²⁾ | | 6116SA150 ⁽²⁾ 6116LA150 ⁽²⁾ | | Unit |
|----------------------------------|---------------------------------|----------------------|------|--|------|--|------|--|------|--|------|--|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Write Cycle | | | | | | | | | | | | | | |
| t _{WC} | Write Cycle Time | 45 | — | 55 | — | 70 | — | 90 | — | 120 | — | 150 | — | ns |
| t _{CW} | Chip Select to End-of-Write | 30 | — | 40 | — | 40 | — | 55 | — | 70 | — | 90 | — | ns |
| t _{AW} | Address Valid to End-of-Write | 30 | — | 45 | — | 65 | — | 80 | — | 105 | — | 120 | — | ns |
| t _{AS} | Address Set-up Time | 0 | — | 5 | — | 15 | — | 15 | — | 20 | — | 20 | — | ns |
| t _{WP} | Write Pulse Width | 25 | — | 40 | — | 40 | — | 55 | — | 70 | — | 90 | — | ns |
| t _{WR} | Write Recovery Time | 0 | — | 5 | — | 5 | — | 5 | — | 5 | — | 10 | — | ns |
| t _{WHZ} ⁽³⁾ | Write to Output in High-Z | — | 25 | — | 30 | — | 35 | — | 40 | — | 40 | — | 40 | ns |
| t _{DW} | Data to Write Time Overlap | 20 | — | 25 | — | 30 | — | 30 | — | 35 | — | 40 | — | ns |
| t _{DH} ⁽⁴⁾ | Data Hold from Write Time | 0 | — | 5 | — | 5 | — | 5 | — | 5 | — | 10 | — | ns |
| t _{OW} ^(3,4) | Output Active from End-of-Write | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |

3089 tbl 15

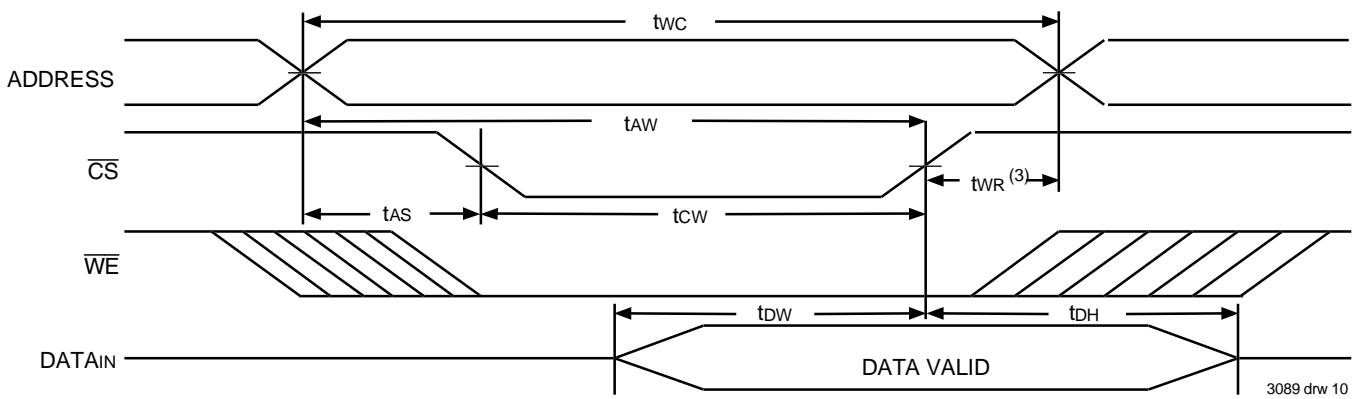
NOTES:

- 0°C to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- This parameter guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.
- The specification for t_{DH} must be met by the device supplying write data to the RAM under all operation conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.

Timing Waveform of Write Cycle No. 1 (\overline{WE} Controlled Timing)^(1,2,5,7)



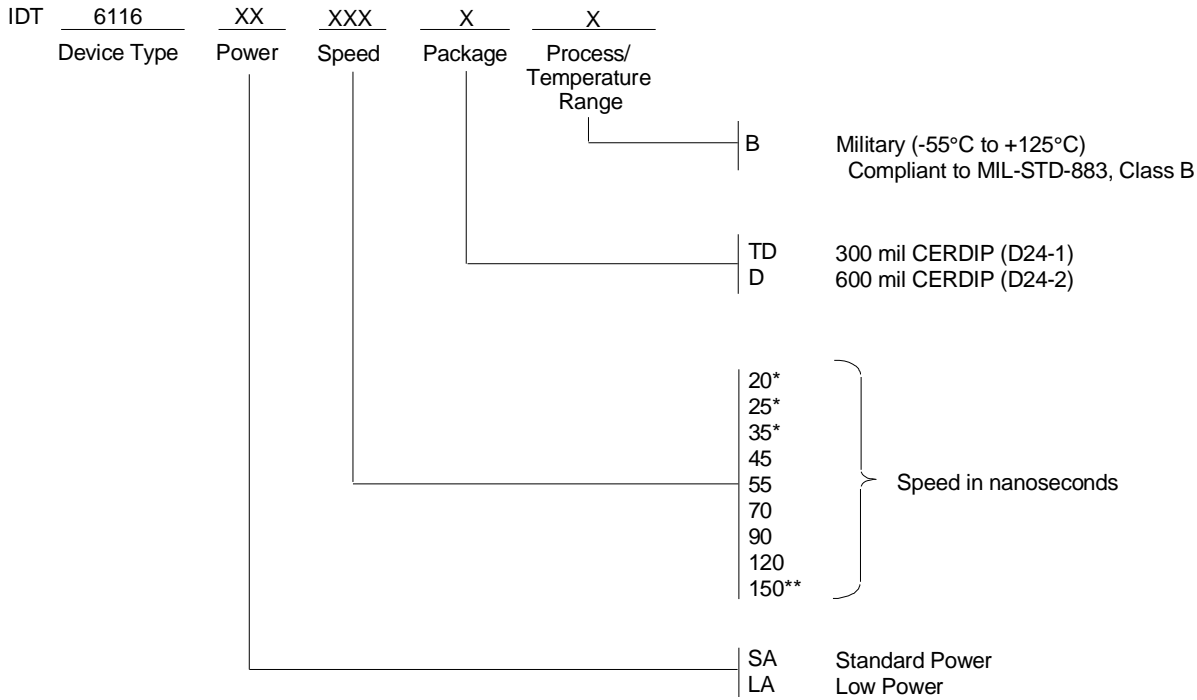
Timing Waveform of Write Cycle No. 2 (\overline{CS} Controlled Timing)^(1,2,3,5,7)



NOTES:

1. \overline{WE} or \overline{CS} must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW \overline{CS} and a LOW \overline{WE} .
3. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and the input signals must not be applied.
5. If the \overline{CS} LOW transition occurs simultaneously with or after the \overline{WE} LOW transition, the outputs remain in the high-impedance state.
6. Transition is measured $\pm 500\text{mV}$ from steady state.
7. \overline{OE} is continuously HIGH. If \overline{OE} is LOW during a \overline{WE} controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WHZ} + t_{DW})$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the write pulse is the specified t_{WP} . For a \overline{CS} controlled write cycle, \overline{OE} may be LOW with no degradation to t_{CW} .

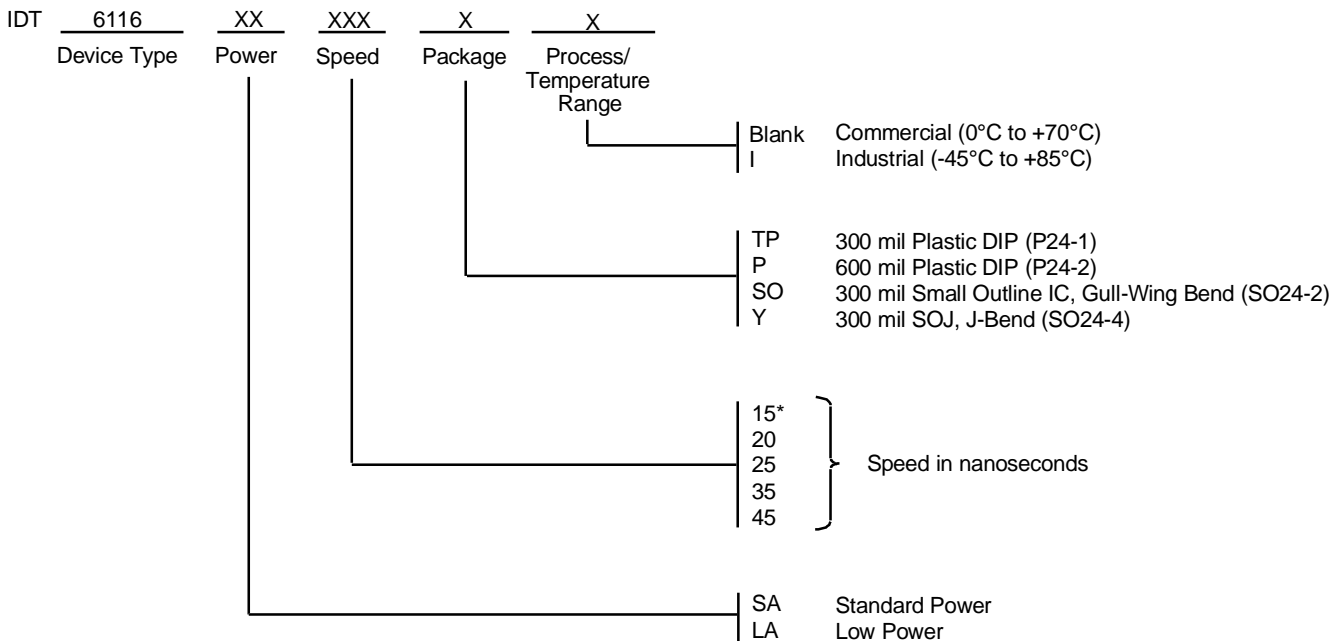
Ordering Information — Military



*Available in 300 mil packaging only.
**Available in 600 mil packaging only.

3089 drw 11

Ordering Information — Commercial & Industrial



*Available in commercial temperature range and standard power only.

3089 drw 12

Datasheet Document History

| | | |
|----------|-----------------|--|
| 1/7/00 | | Updated to new format |
| | Pg. 1, 3, 4, 10 | Added Industrial Temperature range offerings |
| | Pg. 9, 10 | Separated ordering information into military, commercial, and industrial temperature range offerings |
| | Pg. 11 | Added Datasheet Document History |
| 08/09/00 | | Not recommended for new designs |
| 02/01/01 | | Removed "Not recommended for new designs" |



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