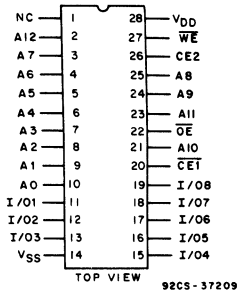


CDM6264



TOP VIEW
92CS-37209
TERMINAL ASSIGNMENT

CMOS 8192-Word by 8-Bit LSI Static RAM

Features:

- Fully static operation
- Single power supply: 4.5 V to 5.5 V
- All inputs and outputs directly TTL compatible
- Industry standard 28-pin configuration
- Input address buffers gated off with chip disable
- 3-state outputs

The RCA-CDM6264 is a 8192-word by 8-bit static random-access memory. It is designed for use in memory systems where high-speed, low power and simplicity in use are desirable. This device has common data input and data output and utilizes a single power supply of 4.5 V to 5.5 V.

Either chip enable ($\overline{CE1}$ or $\overline{CE2}$), when not valid, will gate off the address and output buffers and power down the chip to

minimum standby power with inputs toggling. The output enable (\overline{OE}) controls the output buffers to eliminate bus contention.

The CDM6264 is supplied in a 28-lead dual-in-line plastic (E suffix) package.

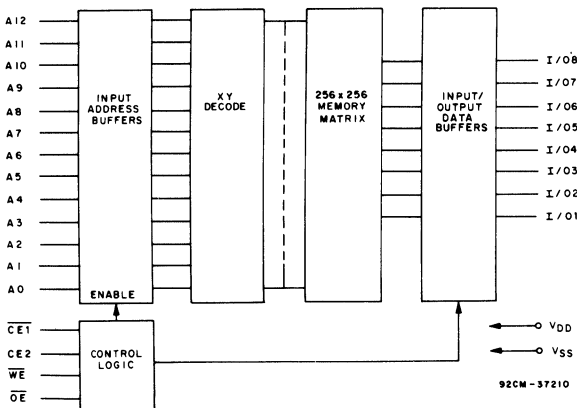


Fig. 1 - Functional block diagram.

	CDM6264-3	CDM6264-2T
Access Time (max)	150 ns	200 ns
Output Enable Time (max.)	70 ns	70 ns
Operating Current (max.)	45 mA	45 mA
Standby Current I_{DDS1} (max.)	100 μ A	200 μ A
Operating Temp. Range:	0°C to +70°C	-40°C to +85°C
Data Retention Voltage:		
0°C $\leq T_A \leq +70^\circ$ C	2 V min	—
0°C $\leq T_A \leq +85^\circ$ C	—	2 V min
-40°C $\leq T_A < 0^\circ$ C	—	4 V min.

TRUTH TABLE

$\overline{CE1}$	$\overline{CE2}$	\overline{OE}	\overline{WE}	A0 TO A12	MODE	DATA I/O	DEVICE CURRENT
H	X	X	X	X	NOT SELECTED	HIGH Z	STANDBY
X	L	X	X	X	NOT SELECTED	HIGH Z	STANDBY
L	H	L	H	STABLE	READ	DATA OUT	ACTIVE
L	H	X	L	STABLE	WRITE	DATA IN	ACTIVE
L	H	H	H	STABLE	OUTPUT DISABLE	HIGH Z	ACTIVE

L = LOW H = HIGH X = H OR L

CDM6264

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
 (Voltage referenced to V_{SS} terminal) -0.3 to +7 V
 INPUT VOLTAGE RANGE, ALL INPUTS -0.3 to +7 V
 POWER DISSIPATION PER PACKAGE (P_D):
 For T_A = -40° to +60° C 500 mW
 For T_A = +60° to +85° C Derate linearly at 8 mW/°C to 300 mW
 DEVICE DISSIPATION PER OUTPUT TRANSISTOR
 For T_A = FULL PACKAGE-TEMPERATURE RANGE 100 mW
 OPERATING-TEMPERATURE RANGE (T_A):
 CDM6264-3 0° to +70° C
 CDM6264-2L -40° to +85° C
 STORAGE TEMPERATURE RANGE (T_{stg}) -55 to +125° C
 LEAD TEMPERATURE (DURING SOLDERING):
 At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. +265° C

OPERATING CONDITIONS at T_A = 0° to +70° C (CDM6264-3); T_A = -40° to +85° C (CDM6264-2L)

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS			UNITS
	ALL TYPES			
	MIN.		MAX.	
DC Operating Voltage Range		4.5	5.5	V
Input Voltage Range	V _{IH}	2.2	V _{DD} + 0.3	
	V _{IL}	-0.3	0.8	
Input Signal Rise or Fall Time ^Δ	t _r , t _f	—	5	μs

^ΔInput signal rise and fall times with a duration greater than the maximum value can cause loss of stored data in the selected mode.

STATIC ELECTRICAL CHARACTERISTICS at T_A = 0° to +70° C (CDM6264-3); T_A = -40° to +85° C (CDM6264-2L), V_{DD} = 5 V ± 10%, Except as noted

CHARACTERISTIC	CONDITIONS	LIMITS						UNITS	
		CDM6264-3			CDM6264-2L				
		Min.	Typ.*	Max.	Min.	Typ.*	Max.		
Standby Device Current	I _{DDS}	CE1=V _{IH} or CE2=V _{IL}	—	1.5	3	—	2	4	mA
	I _{DDS1}	CE1=CE2 ≥ V _{DD} -0.2 V or CE2 ≤ 0.2 V	—	5	100	—	10	200	μA
Output Voltage Low Level	V _{OL} Max.	I _{OL} =2.1 mA	—	—	0.4	—	—	0.4	V
		I _{OL} =1 μA	—	0.1	—	—	0.1	—	
Output Voltage High Level	V _{OH} Min.	I _{OH} =-1 mA	2.4	—	—	2.4	—	—	V
		I _{OH} =-1 μA	—	V _{DD} -0.1	—	—	V _{DD} -0.1	—	
Input Leakage Current	I _{IN} Max.	V _{IN} =0 V to V _{DD}	—	±0.1	±2	—	±0.1	±2	μA
3-State Output Leakage Current	I _{OUT}	V _{I,O} =0 V to V _{DD}	—	±0.5	±2	—	±0.5	±2	μA
Operating Device Current	I _{OPER1} [#]	V _{IN} =V _{IL} , V _{IH} t _{cyc} =1 μs	—	4.5	9	—	7.5	15	mA
		t _{cyc} =min. cycle time	—	22.5	45	—	22.5	45	
	I _{OPER2} [#]	V _{IN} =0.2 V, t _{cyc} =1 μs	—	2	4	—	5	10	
		V _{DD} -0.2 V t _{cyc} =min. cycle time	—	20	40	—	20	40	
Input Capacitance	C _{IN}	V _{IN} =0 V, f=1 MHz, T _A =25° C	—	4	6	—	4	6	pF
Output Capacitance	C _{I,O}	V _{I,O} =0 V, f=1 MHz, T _A =25° C	—	6	8	—	6	8	pF

*Typical values are for T_A=25° C and nominal V_{DD}.

#Outputs open circuited.



CDM6264

SIGNAL DESCRIPTIONS

A0-A12 (Address Inputs): These inputs must be stable prior to a write operation, but may change asynchronously during read functions.

I/O1-I/O8: 8-bit tristate data bus.

CE1, CE2 (Chip Enable): Either chip enable, when not true, powers down the chip, disables Read and Write functions, and gates off address and output buffers.

OE (Output Enable): Enables tristate outputs if CE1 and CE2 are valid and OE is high.

WE (Write Enable): Enables Write function, if CE1 and CE2 are valid. WE will dominate if both WE and OE are low (i.e., the bus will be tristated and a Write will occur).

V_{DD}, V_{SS}: Power supply connections.

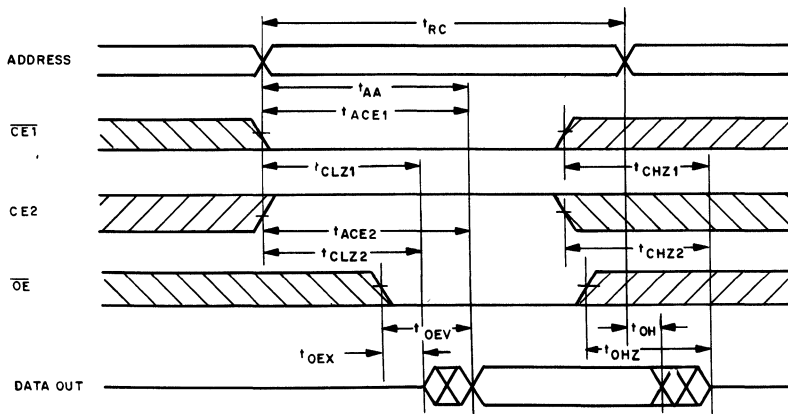
DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0° to +70° C (CDM6264-3);

T_A = -40° to +85° C (CDM6264-2I), V_{DD} = 5 V ± 10%,

Input t_r, t_f = 10 ns; C_L = 100 pF and 1 TTL Load, Input Pulse Levels: 0.8 V to 2.4 V

CHARACTERISTIC		LIMITS				UNITS
		CDM6264-3		CDM6264-2I		
		MIN. [†]	MAX.	MIN. [†]	MAX.	
Read Cycle Times, See Fig. 2						
Read Cycle Time	t _{RC}	150	—	200	—	ns
Address Access Time	t _{AA}	—	150	—	200	
Chip Enable Access Time	t _{ACE1} , t _{ACE2}	—	150	—	200	
Chip Enable to Output Active	t _{CLZ1} , t _{CLZ2}	10	—	10	—	
Output Enable to Output Valid	t _{OEV}	—	70	—	70	
Output Enable to Output Active	t _{OEX}	5	—	5	—	
Chip Disable to Output "High Z"	t _{CHZ1} , t _{CHZ2}	0	70	0	70	
Output Disable to Output "High Z"	t _{OHZ}	0	60	0	60	
Output Hold from Address Change	t _{OH}	30	—	30	—	

[†] Time required by a limit device to allow for the indicated function.



WE IS HIGH DURING READ CYCLE. TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.

92CM-37205

Fig. 2 - Read-cycle timing waveforms.

CDM6264

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 0^\circ$ to $+70^\circ\text{C}$ (CDM6264-3);

$T_A = -40^\circ$ to $+85^\circ\text{C}$ (CDM6264-2I), $V_{DD} = 5\text{ V} \pm 10\%$,

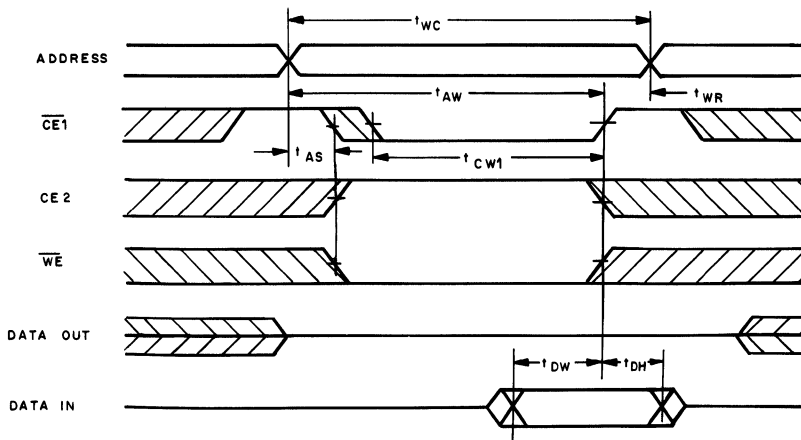
Input $t_r, t_f = 10\text{ ns}$; $C_L = 100\text{ pF}$ and 1 TTL Load, Input Pulse Levels: 0.8 V to 2.4 V

CHARACTERISTIC		LIMITS				UNITS
		CDM6264-3		CDM6264-2I		
		MIN.†	MAX.	MIN.†	MAX.	
Write Cycle Times, See Fig. 3						
Write Cycle Time	t_{wc}	150	—	200	—	ns
Chip Enable to End of WRITE	t_{cw1}, t_{cw2}	120	—	170	—	
Address Valid to End of WRITE	t_{aw}	120	—	170	—	
Address Setup Time	t_{as}	0	—	0	—	
Write Enable Width	t_{ww}	100	—	120	—	
Write Recovery Time	t_{wr}	0	—	0	—	
Write to Output "High Z"	t_{whz}	—	70	—	80	
Input Data Setup Time	t_{dw}	60	—	80	—	
Input Data Hold Time	t_{dh}	0	—	0	—	
Output Active from End of Write	t_{ow}	10	—	10	—	

†Time required by a limit device to allow for the indicated function.

WRITE CYCLE 1 (CE1 CONTROL)

5



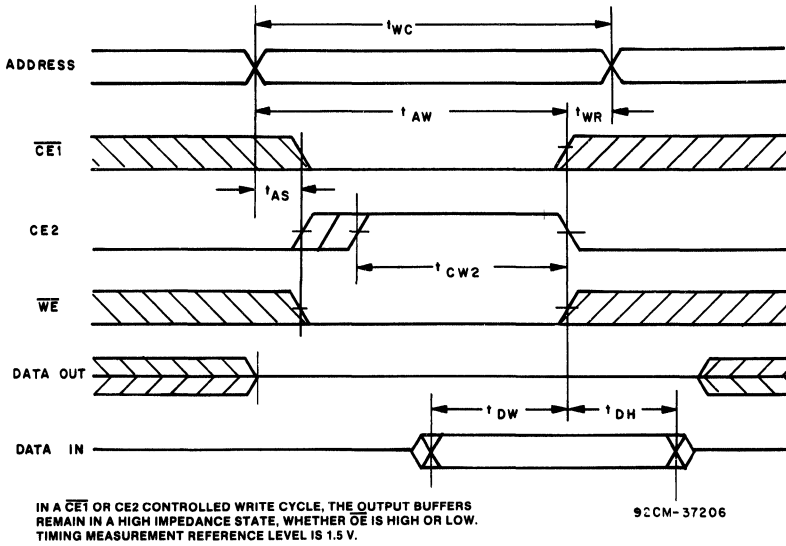
IN A CE1 OR CE2 CONTROLLED WRITE CYCLE, THE OUTPUT BUFFERS REMAIN IN A HIGH IMPEDANCE STATE, WHETHER CE IS HIGH OR LOW. TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.

92CM-37204

Fig. 3 - Write-cycle timing waveforms.

CDM6264

WRITE CYCLE 2 (CE2 CONTROL)



WRITE CYCLE 3 (\overline{WE} CONTROL)

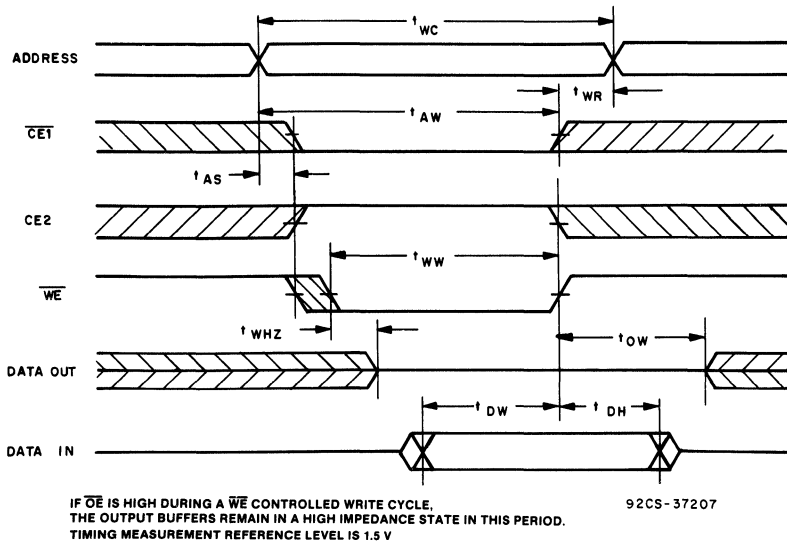


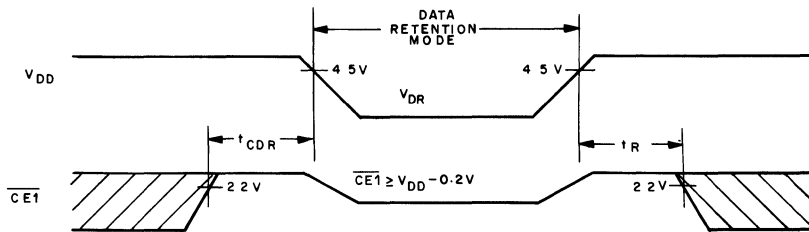
Fig. 3 - Write-cycle timing waveforms (cont'd).

DATA RETENTION CHARACTERISTICS, See Fig. 4.

CHARACTERISTIC	TEST CONDITIONS	LIMITS				UNITS
		CDM6264-3		CDM6264-2I		
		Min.	Max.	Min.	Max.	
Minimum Data Retention Voltage V_{DR}	$CE1 \geq V_{DD}-0.2 V$, or $CE2 \leq 0.2 V$:	2	—	—	—	V
	$0^{\circ}C \leq T_A \leq +70^{\circ}C$	—	—	2	—	
	$0^{\circ}C \leq T_A \leq +85^{\circ}C$	—	—	—	4	
Data Retention Quiescent Current I_{DDDR}	$CE1, CE2 \geq V_{DD}-0.2 V$, or $CE2 \leq 0.2 V$:	—	50	—	—	μA
	$V_{DD} = 3 V, 0^{\circ}C \leq T_A \leq +70^{\circ}C$	—	—	—	100	
	$V_{DD} = 3 V, 0^{\circ}C \leq T_A \leq +85^{\circ}C$	—	—	—	100	
	$V_{DD} = 4 V, -40^{\circ}C \leq T_A < 0^{\circ}C$	—	—	—	100	
Chip Disable to Data Retention Time t_{CDR}	See Fig. 4	0	—	0	—	ns
Recovery to Normal Operation Time t_R	See Fig. 4	* t_{RC}	—	* t_{RC}	—	

* t_{RC} = Read Cycle Time

DATA RETENTION WAVEFORM 1 (CE1 CONTROL)



DATA RETENTION WAVEFORM 2 (CE2 CONTROL)

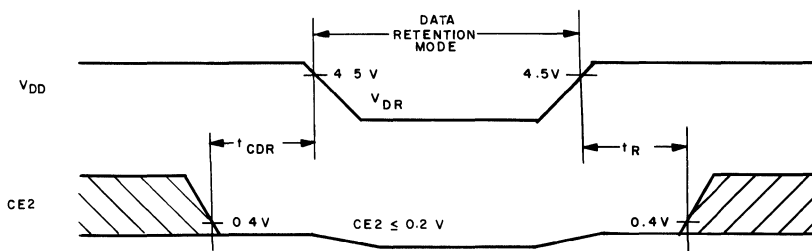


Fig 4 - Low V_{DD} data-retention timing waveforms. 92CM -37208