3258

64 × 7 × 5 CHARACTER GENERATOR

GENERAL DESCRIPTION – The 3258 is a Character Generator designed to display 64 characters in a 5 x 7 dot matrix. An on-chip row select counter sequences through the seven rows of each character. The five output buffers will each drive one TTL/DTL load directly at a 1.6 MHz input address rate making the 3258 an ideal device for CRT displays. Special input amplifiers on the Clock, Master Reset, and Address lines have eliminated the need for pull up resistors and allow direct operation at TTL/DTL logic levels.

- **PROGRAMMABLE WITH A CUSTOM CHARACTER FONT**
- **STANDARD PRODUCT: ASCII FONT**
- **16-PIN DUAL IN-LINE PACKAGE**
- **DIRECT TTL/DTL INTERFACE AT INPUTS AND OUTPUTS**
- **ON-CHIP ROW SELECT COUNTER**

PIN NAMES

A_n	Character Address Inputs
$\overline{O_n}$	Character Outputs
$\overline{CP}$	Clock Pulse Input
$\overline{MR}$	Master Reset Input
V_{GG}	–12 V Power Supply
V_{DD}	0 V Power Supply
V_{SS}	+5.0 V Power Supply

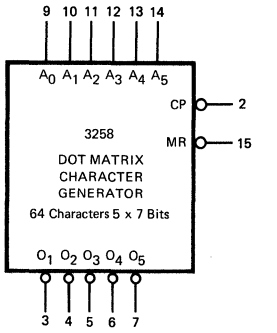
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65° to +150°C
Operating Temperature	0°C to +70°C
Voltage on any Pin Relative to V_{SS}	–20 V to +0.3 V

APPLICATIONS:

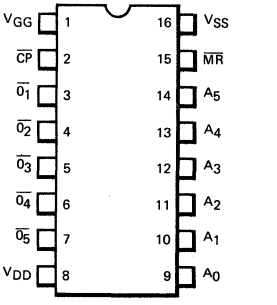
CRT Displays
Billboard Displays
LED Matrix Displays

LOGIC SYMBOL

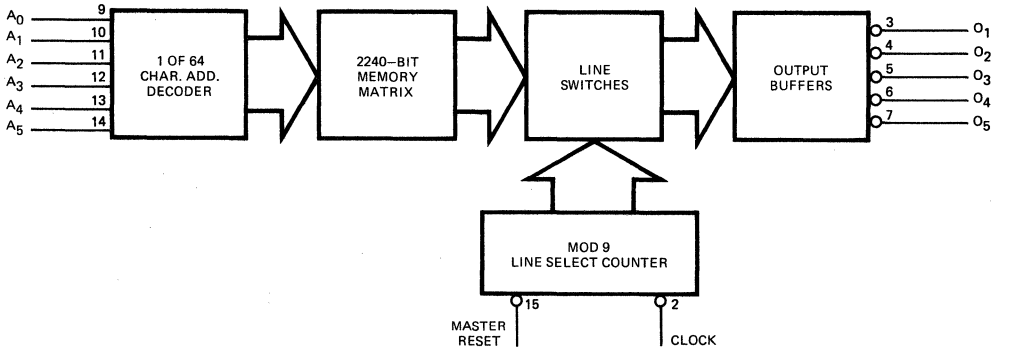


V_{SS} = PIN 16
V_{DD} = PIN 8
V_{GG} = PIN 1

CONNECTION DIAGRAM
DIP (TOP VIEW)



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION — A Master Reset pulse (≅ GND) is required to set the Modulo 9 counter to the first state. A 6-bit binary word present at the address inputs is decoded to select 1 of 64 characters in the memory. Information, representing the first row of the character, will be available at the five outputs the next clock time after the Master Reset goes HIGH (≅ V_{SS}). The next six rows of the character are sequentially selected by the counter. The last state of the counter, like the first state, clamps the outputs HIGH (≅ V_{SS}) which provides 2-space blanking between lines. The counter dead ends at the last state and the outputs will remain HIGH (≅ V_{SS}) providing blanking, until another Master Reset pulse is provided.

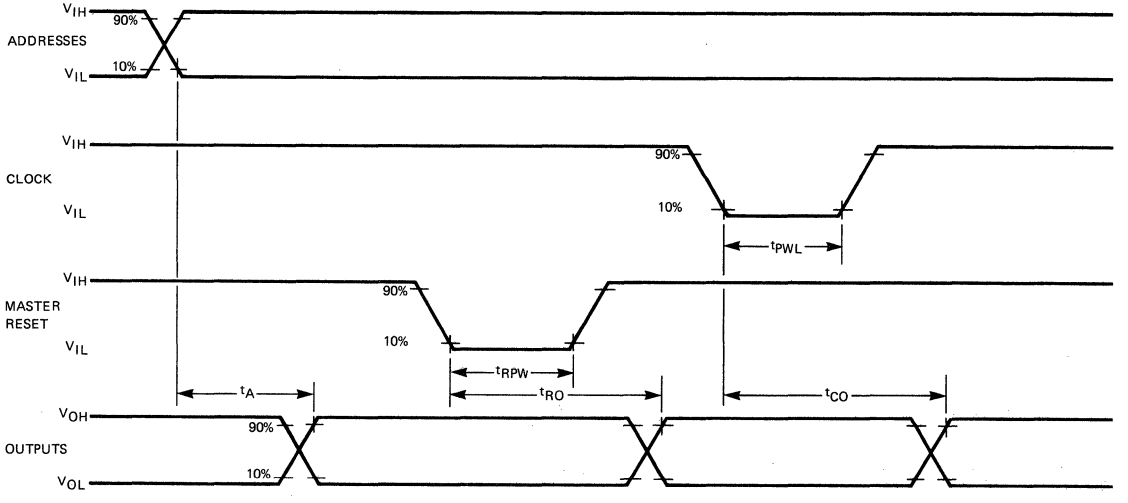
DC CHARACTERISTICS: V_{SS} = +5 V ±5%, V_{GG} = −12 V ±5%, V_{DD} = 0 V, T_A = 0°C to 70°C.

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	V_{SS} −2.35	V_{SS}	V	All Inputs
V_{IL}	Input LOW Voltage	V_{GG}	0.55	V	All Inputs
V_{OH}	Output HIGH Voltage	2.4	V_{SS}	V	I_{OH} = −0.5 mA
V_{OL}	Output LOW Voltage	0	0.4	V	I_{OL} = 2.4 mA
I_{IN}	Input Leakage Current		1.0	μA	V_{IN} = −13 V (Note 1)
I_{SS}	V_{SS} Current		28	mA	V_{SS} = +5.25 V, V_{GG} = −12.6 V Outputs Open
I_{GG}	V_{GG} Current		−28	mA	V_{SS} = +5.25 V, V_{GG} = −12.6 V Outputs Open
P_D	Power Dissipation		500	mW	

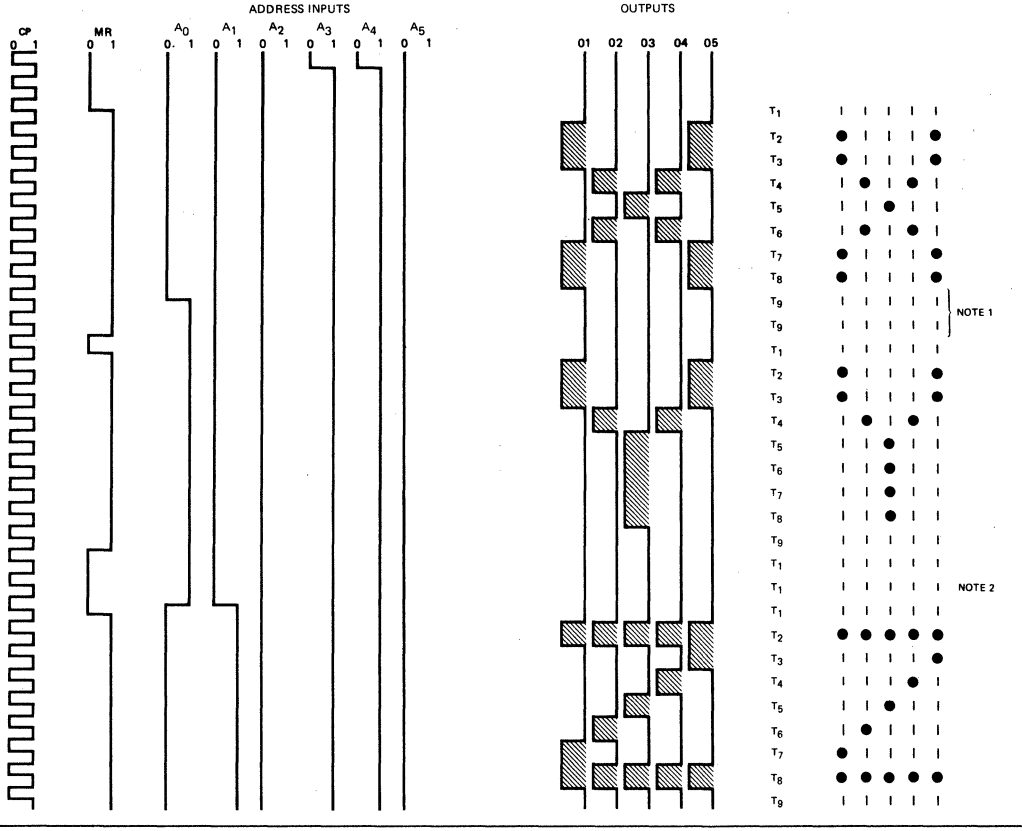
AC CHARACTERISTICS: V_{SS} = +5 V ±5%, V_{GG} = −12 V ±5%, V_{DD} = 0 V, C_L = 10 pF, T_A = 0°C to +70°C.

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	CONDITIONS
f	Clock Frequency		0	500	kHz	
t_{PWL}	Clock Pulse Width		1.0		μs	
t_r, t_f	Clock Rise and Fall Time			2.0	μs	
t_{RPW}	Reset Pulse Width		500		ns	
t_{RS}	Reset to Clock Set-up		200		ns	
t_A	Character Address to Output Time Delay	3258-1		550	ns	
		3258-2		625	ns	
		3258		800	ns	
t_{CO}	Clock to Output Time Delay			2.0	μs	
t_{RO}	Reset to Output Time Delay			2.0	μs	

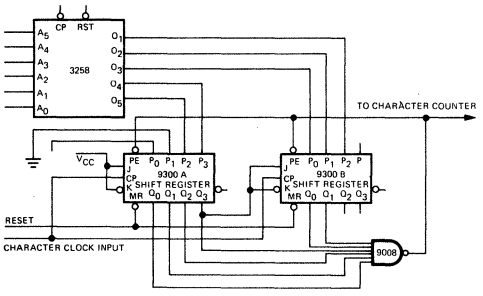
TIMING DIAGRAM

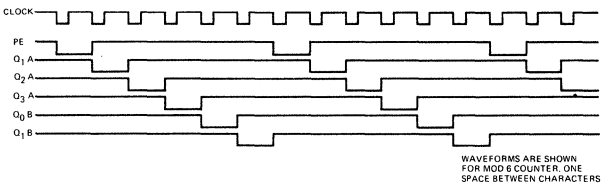


FUNCTIONAL TIMING DIAGRAM



APPLICATIONS





OPERATION:

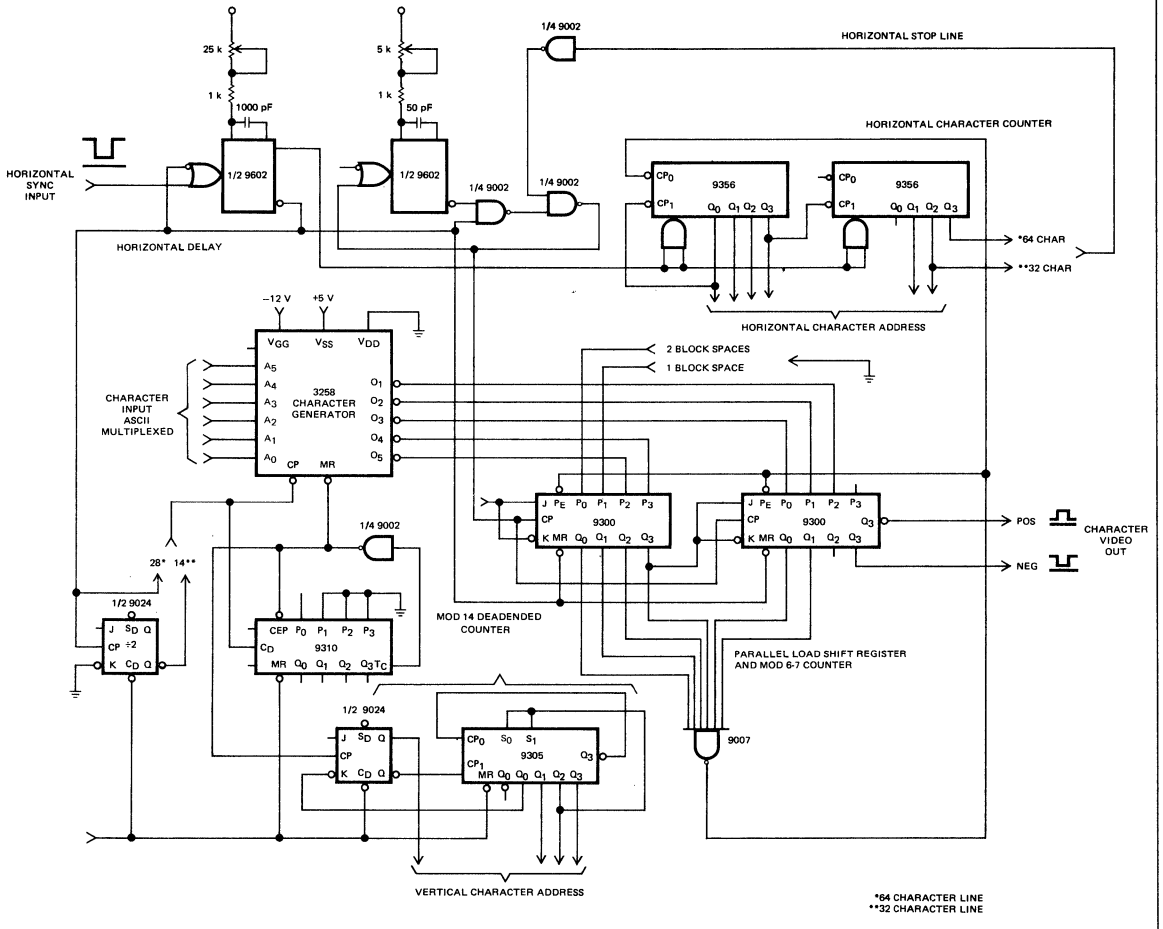
The two 9300 registers and the 9008, eight-input gate combine to form the character clock counter and the parallel to serial converter required for the outputs of the 3258 character generator.

When all the gate inputs are HIGH, the gate output is LOW which enables the parallel load (PE) of the shift registers. On the next clock pulse, positive edge after PE goes LOW, the contents of the 3258 character generator and the LOW on P_0 (A) are transferred into the registers. This LOW is shifted down the registers followed by all HIGH's from the JK input. On reaching Q_2 (B) all the outputs to the gates are once again HIGH, therefore reloading the shift registers again. The modulo count of the system can easily be changed to Modulo 7 by loading in a zero on P_0 (A).

The shift counter is reset at the beginning of each horizontal raster line to ensure that it has the correct time phase.

APPLICATIONS (cont'd)

HORIZONTAL RASTER SCAN CHARACTER GENERATOR



CUSTOM FONT ORDERING INFORMATION

Additional character fonts are available on request. The 3258 is programmed on IBM cards or IBM coding forms in the coding format shown below:

A logic "1" = A more positive voltage nominally +5 V
A logic "0" = A more negative voltage nominally 0 V

The character must be defined by a logic "0". The background by a logic "1". Each character is programmed on one IBM card or a single line on the coding form.

COLUMN NUMBER	DESCRIPTION
6,7,8,9,10,11	Character address input code. The most significant bit (A32) is in Column 11.
22,23,24,25,26	The top line of the character addressed. The most significant bit (05) is in Column 26.
28,29,30,31,32	The next line of the character addressed. The most significant bit (05) is in Column 32.
34,35,36,37,38	The next line of the character addressed. The most significant bit (05) is in Column 38.
40,41,42,43,44	The next line of the character addressed. The most significant bit (05) is in Column 44.
46,47,48,49,50	The next line of the character addressed. The most significant bit (05) is in Column 50.
52,53,54,55,56	The next line of the character addressed. The most significant bit (05) is in Column 56.
58,59,60,61,62	The bottom line of the character addressed. The most significant bit (05) is in Column 62.
73,74,75,76,77,78,79,80	Coding these columns is not essential and may be used for card identification purpose.

STANDARD ASCII CHARACTER FONT