Am9060

4096-Bit Dynamic R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- High density 4096 x 1 organization
- High output drive – two full TTL loads
- TTL compatible interface (except CE)
- Low power dissipation –
  - 400mW typ., 750mW max. operating
  - 5.0mW typ., 13mW max. refresh only
  - 0.1mW typ., 3.0mW max. standby
- Low I_{DD} current surges – easier decoupling
- Low V_{CC} current drain – 10μA
- Simplified timing requirements –
  - Zero data hold with respect to CE
  - Optional data hold with respect to R/W
  - Optional data set-up with respect to R/W
- Low clock capacitance –20pF max.
- Unique fully capacitive input circuits – eliminate extraneous current surges
- Direct plug-in replacement for TMS4060
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

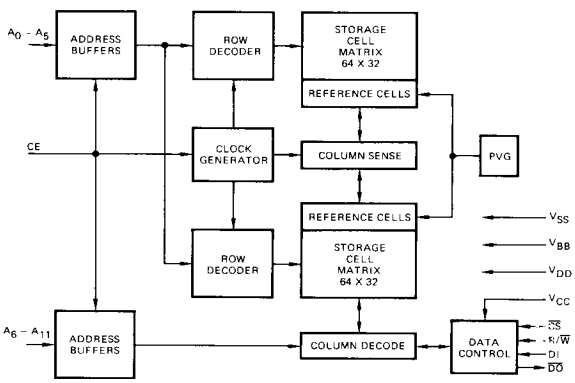
FUNCTIONAL DESCRIPTION

The Am9060 devices are high performance, 4k-bit, dynamic, read/write, random access memories. They are organized as 4096 words by 1-bit per word. The basic memory element is a one-transistor cell that stores charge on a small internal capacitor. The memory mechanism is dynamic and the chip should be periodically refreshed in order to maintain stored data integrity.

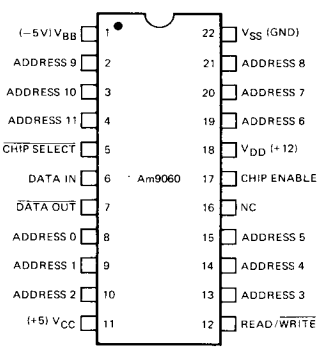
All input signals are fully TTL compatible, except the single high-level clock signal called Chip Enable. When CE goes low the memory is internally precharged and then assumes its low power standby mode. All operating cycles are initiated when CE goes high. Read-out is nondestructive so simple read or write operations are normally performed. Successive operations at the same location can be designed to improve performance since readdressing is not required. The most useful double operation combination is specified as a Read/Modify/Write cycle.

The output buffer will drive two standard TTL loads. The buffer is a three-state totem-pole configuration and exhibits a high output impedance when CE is low or when the chip is unselected. Output data polarity is inverted relative to the input data.

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Ambient Temperature Specification	Package Type	Access Time		
		300ns	250ns	200ns
$0°C \leq T_A \leq +70°C$	Molded DIP	AM9060CPC	AM9060DPC	AM9060EPC
	Hermetic DIP	AM9060CDC	AM9060DDC	AM9060EDC

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	0°C to +70°C
All Supply Voltages with Respect to V_{BB}	−0.3V to +20V
All Input Signal Voltages with Respect to V_{BB}	−0.3V to +20V
Output Voltage with Respect to V_{SS}, Operating	−2.0V to +7.0V
Power Dissipation	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Ambient Temperature	V_{DD}	V_{CC}	V_{SS}	V_{BB}
0°C to +70°C	+12V ± 5%	+5.0V ± 5%	0	−5.0V ± 10%

No signal or supply voltage should ever be more than 0.3V more negative than V_{BB}.

ELECTRICAL CHARACTERISTICS over operating range (note 1)

Parameters	Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0mA		2.4		V_{CC}	Volts
V_{OL}	Output LOW Voltage	I_{OL} = 3.2mA		V_{SS}		0.4	Volts
V_{IH}	Input HIGH Voltage (Except CE)			2.4		V_{CC}	Volts
V_{IL}	Input LOW Voltage (Except CE)			−0.6		0.8	Volts
$V_{IH(CE)}$	Chip Enable Input HIGH Voltage			V_{DD} −0.6		V_{DD} +1.0	Volts
$V_{IL(CE)}$	Chip Enable Input LOW Voltage			−1.0		0.8	Volts
I_I	Input Load Current (Except CE)	$V_{SS} \leq V_I \leq V_{CC}$				10	μA
$I_{I(CE)}$	Input Load Current, CE	$-1.0V \leq V_{I(CE)} \leq 13.2V$				2.0	μA
I_{OZ}	Output Leakage Current	$-0.6V \leq V_O \leq V_{CC}$ $CE = V_{IL(CE)}$ or $\overline{CS} = V_{IH}$				10	μA
I_{CC}	V_{CC} Supply Current (Note 7)	$CE = V_{IL(CE)}$ or $\overline{CS} = V_{IH}$				10	μA
I_{DD}	V_{DD} Supply Current	$V_{IH(CE)}$ = 12.6V			32	60	mA
		$V_{IL(CE)}$ = 0.6V			10	200	μA
$I_{DD(AV)}$	Average V_{DD} Supply Current	Read or Write cycle minimum cycle time	Am9060C		29	60	mA
			Am9060D		31	60	
			Am9060E		32	60	
		Read/Modify/Write cycle minimum cycle time	Am9060C		29	60	
			Am9060D		31	60	
			Am9060E		32	60	
I_{BB}	V_{BB} Supply Current	V_{BB} = −5.5V, V_{DD} = 12.6V V_{CC} = 5.25V, V_{SS} = 0V			−5.0	−100	μA

CAPACITANCE

Parameters	Description	Test Conditions		Typ. (Note 1)	Max.	Units
$C_{i(AW)}$	Input Capacitance (Address and Write)	V_{DD} = 12V, V_{SS} = 0V V_{BB} = −5.0V, V_{CC} = 5.0V All inputs = 0V f = 1MHz		5.0	7.0	pF
$C_{i(CD)}$	Input Capacitance (Chip Select and Data)			3.0	5.0	pF
$C_{i(CE)}$	Input Capacitance (Chip Enable)		$V_{I(CE)}$ = −1.0, 10.8	15	20	pF
C_O	Output Capacitance			3.0	5.0	pF

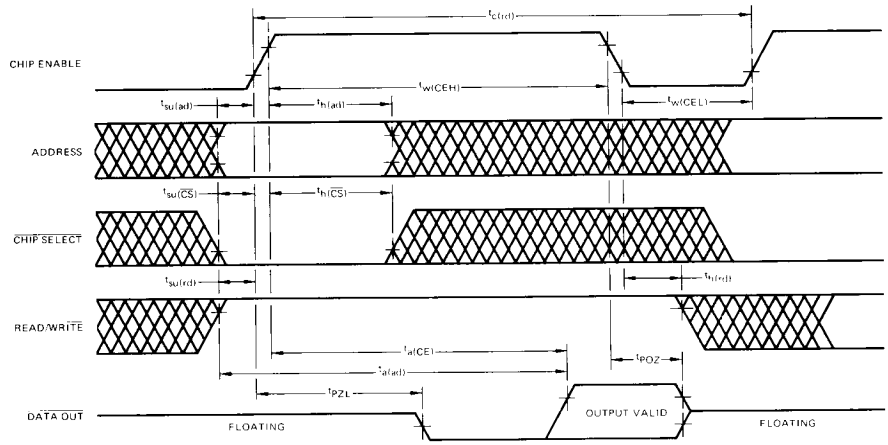
SWITCHING CHARACTERISTICS over operating range

Parameters	Description	Test Conditions		Am9060C Min.	Am9060C Max.	Am9060D Min.	Am9060D Max.	Am9060E Min.	Am9060E Max.	Units
t_R	Column Refresh Interval				2.0		2.0		2.0	ms
Read Cycle										
$t_{c(rd)}$	Read Cycle Time	CE transition time ≤ 20ns		470		430		400		ns
$t_{w(CEH)}$	Chip Enable HIGH Pulse Width	Chip Enable transition times ≤40ns		300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Chip Enable LOW Pulse Width			130		130		130		ns
$t_{su(ad)}$	Address Set-up Time			0		0		0		ns
$t_{su(CS)}$	Chip Select Set-up Time			0		0		0		ns
$t_{su(rd)}$	Read Set-up Time			0		0		0		ns
$t_{h(ad)}$	Address Hold Time			125		100		100		ns
$t_{h(CS)}$	Chip Select Hold Time			125		100		100		ns
$t_{h(rd)}$	Read Hold Time			0		0		0		ns
t_{PZL}	Chip Enable to Output ON Delay	Output load: one standard TTL gate plus 50pF			175		150		125	ns
t_{POZ}	Chip Enable to Output OFF Delay			30		30		30		ns
$t_{a(CE)}$	Chip Enable Access Time (Note 6)		Chip enable rise time ≤20ns		280		230		180	ns
$t_{a(ad)}$	Address Access Time (Note 6)				300		250		200	ns
Write Cycle										
$t_{c(wr)}$	Write Cycle Time	CE transition time ≤ 20ns		470		430		400		ns
$t_{w(CEH)}$	Chip Enable HIGH Pulse Width	Chip Enable transition times ≤40ns		300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Chip Enable LOW Pulse Width			130		130		130		ns
$t_{w(wr)}$	Write Pulse Width			200		190		180		ns
$t_{su(ad)}$	Address Set-up Time			0		0		0		ns
$t_{su(CS)}$	Chip Select Set-up Time			0		0		0		ns
$t_{su(da)}$	Data In Set-up Time			180		170		160		ns
$t_{su(wr)}$	Write Pulse Set-up Time			240		220		210		ns
$t_{h(ad)}$	Address Hold Time			125		100		100		ns
$t_{h(CS)}$	Chip Select Hold Time			125		100		100		ns
$t_{h(da)}$	Data In Hold Time (Note 2)			0 (30)		0 (20)		0 (10)		ns
Read/Modify/Write Cycle										
$t_{c(RMW)}$	Read/Modify/Write Cycle Time	CE transition time and Read/Write fall time ≤ 20ns		710		640		580		ns
$t_{w(CEH)}$	Chip Enable HIGH Pulse Width			540	4000	470	4000	410	4000	ns
$t_{w(CEL)}$	Chip Enable LOW Pulse Width	Chip Enable transition times ≤40ns		130		130		130		ns
$t_{w(wr)}$	Write Pulse Width			200		190		180		ns
$t_{su(ad)}$	Address Set-up Time			0		0		0		ns
$t_{su(CS)}$	Chip Select Set-up Time			0		0		0		ns
$t_{su(da)}$	Data In Set-up Time			180		170		160		ns
$t_{su(rd)}$	Read Set-up Time			0		0		0		ns
$t_{su(wr)}$	Write Pulse Set-up Time			240		220		210		ns
$t_{h(ad)}$	Address Hold Time			125		100		100		ns
$t_{h(CS)}$	Chip Select Hold Time			125		100		100		ns
$t_{h(rd)}$	Read Hold Time			280		230		180		ns
$t_{h(da)}$	Data In Hold Time (Note 2)			0 (30)		0 (20)		0 (10)		ns
t_{PZL}	Chip Enable to Output ON Delay	Output load: one standard TTL gate plus 50pF			175		150		125	ns
t_{POI}	Write to Output Invalid Delay			30		30		30		ns
t_{POZ}	Chip Enable to Output OFF Delay			30		30		30		ns
$t_{a(CE)}$	Chip Enable Access Time		Chip Enable rise time ≤20ns		280		230		180	ns
$t_{a(ad)}$	Address Access Time (Note 6)				300		250		200	ns

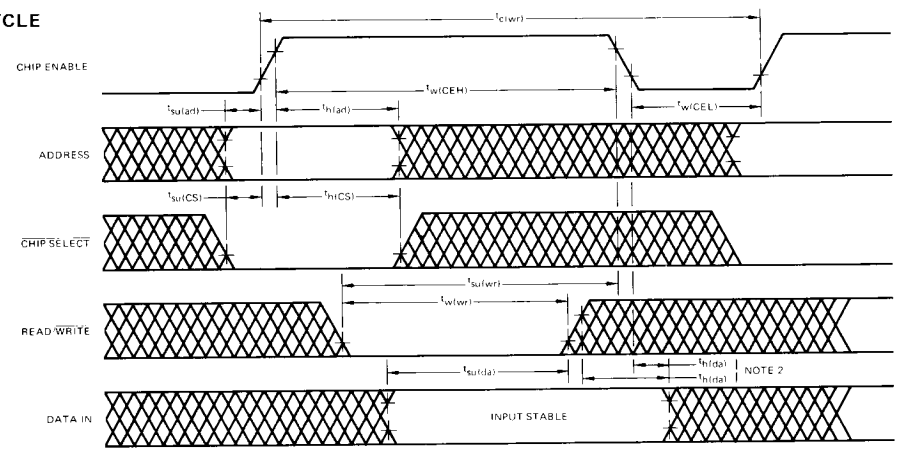
Notes:
1. Typical values are at $T_A = 25°C$, nominal supply voltages and nominal processing parameters.
2. Data Hold time ($t_{h(da)}$) may be optionally specified with respect to either the rising edge of Read/Write or the falling edge of Chip Enable. The zero value shown in the Characteristics table is with respect to Chip Enable. Data hold time with respect to Read/Write is shown in parenthesis.
3. Input signal (except Chip Enable) timing references are 0.6V and 2.2V.
4. Chip Enable timing references are at 10% and 90% of $V_{IH}(CE)$.
5. Output timing references are 0.4V and 2.4V.
6. Slope of access time versus load capacitance is approximately 0.1ns/pF.
7. V_{CC} supplies the final output transistor only. Except for leakage, V_{CC} supply current during CE on is dependent on output loading only.

SWITCHING WAVEFORMS

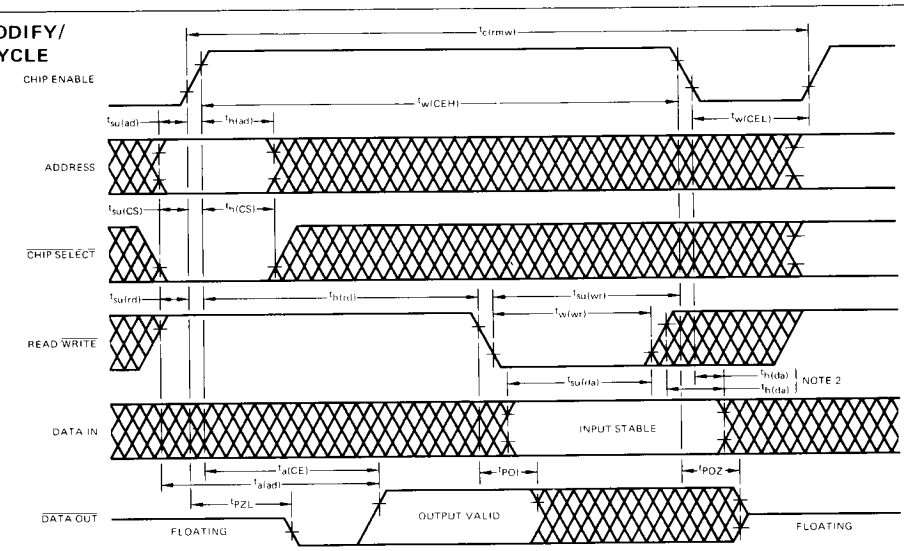
READ CYCLE



WRITE CYCLE



READ/MODIFY/ WRITE CYCLE



APPLICATION INFORMATION

INTERFACE SIGNALS

The 12 Address inputs are used to specify one of 2^{12} locations within the memory (2^{12} = 4096). The Chip Select signal acts as a high order address so that several memory chips may be operated together for capacities greater than 4k words. Registers are included on chip for the Chip Select and Address signals in order to simplify system timing requirements. After the Chip Select input has been latched by the rising edge of CE, the select status of the chip cannot be altered by changing the state of Chip Select line. Chip Select only affects the data control circuitry.

The Data In signal timing is specified relative to the rising edge of R/$\overline{W}$. The Data In and Read/Write circuitry are static and the input data set-up requirement is independent of the write pulse width. The hold time for input data may be timed relative to either R/$\overline{W}$ or to CE, for extra flexibility in system design.

The Read/Write line controls the type of operation being performed. It may be thought of as a normally high signal that is pulsed low when writing is desired. The normally high state prevents unintentional modification of data. R/$\overline{W}$ should also be high during all refresh operations, unless Chip Select is high.

The Chip Enable input is a high level clock signal that controls the basic timing of all internal operations. When CE is low the memory enters the standby mode and dissipates very little power. Active operations begin when CE goes high. In a memory system with an array of storage chips, it is usually the case that only a few devices will be active at any one time, thus keeping the average power dissipation at very low levels.

The Data Out circuitry is three-state and designed to permit wired-OR connection of several chips for greater memory depth than 4k. Unclocked or unselected devices will have high impedance outputs, allowing a selected and clocked device to dominate the output data bus. The output data is inverted relative to the input data; that is, information written in as a logic one will be read out as a logic zero. Valid output is always preceeded by a period of low output data.

All input circuitry in the Am9060 memories is purely capacitive and does not cause clock related current surges to flow in the input lines. This feature improves noise immunity margins and helps simplify input driving requirements.

Current surges occur in the V_{DD} and V_{BB} supplies in conjunction with both the rising and falling transitions of Chip Enable. Both voltages must be carefully decoupled to V_{SS} to prevent the current spikes from generating excessive noise.

REFRESH

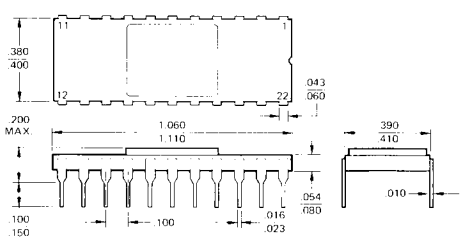
Information is stored as the presence or absence of charge within each internal cell. Leakage currents eventually drain away any charge present in a cell and information is lost. To prevent data loss, a cell can have its charge level restored before too much charge has leaked off. Each cell must be refreshed at least once every 2 ms, worst case.

The 4096 cells in the memory matrix are organized as an array of 64 rows and 64 columns. When any cell within a row is actively cycled, all 64 locations in the row are refreshed. Thus the refresh requirement is met if all 64 rows are accessed every 2 ms. Address lines A_0 through A_5 specify the rows.

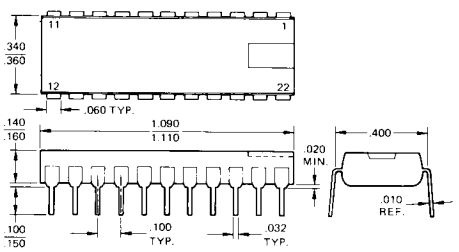
The Chip Select input only controls the Data Out and Read/Write circuitry so that a chip need not be selected in order to be refreshed. This allows parallel refreshing of many devices without causing contention on output busses.

PHYSICAL DIMENSIONS

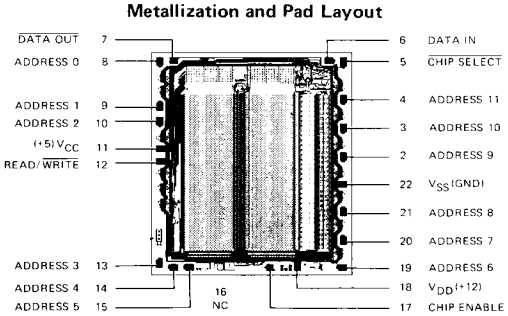
22-Pin Side Brazed



22-Pin Molded



Metallization and Pad Layout



1 — Connected to Substrate (—5V)V_{BB}

DIE SIZE 136" X 161"