DEVICE DESCRIPTION

The 2141 is produced with HMOS, a new high-performance MOS technology which incorporates on-chip substrate bias generation to achieve high-performance. This process, combined with new design ideas, gives the 2141 its unique features. Both low power and ease-of-use have been obtained in a single part. The low-power feature is controlled with the Chip Select input, which is not a clock and does not have to be cycled. Multiple read or write operations are possible during a single select period. Access times are equal to cycle times, resulting in data rates up to 8.3 MHz for the 2141-2. This is considerably higher performance than for clocked static designs.

Whenever the 2141 is deselected, it automatically reduces its power requirements to a fraction of the active power, as shown in Figure 1. This is achieved by switching off the power to unnecessary portions of the internal peripheral circuitry. This feature adds up to significant system power savings. The average power per device declines as system size grows because a continually higher portion of the memory is deselected. Device power dissipation asymptotically approaches the standby power level, as shown in Figure 2.

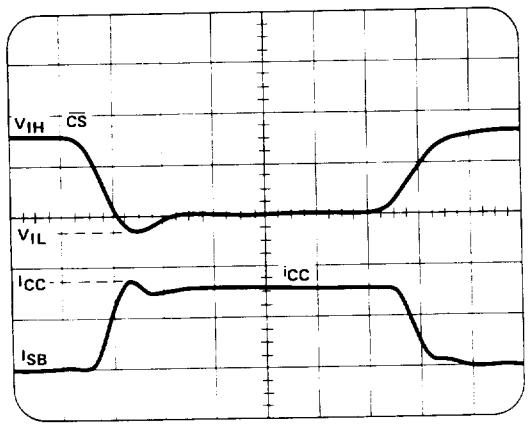


FIGURE 1. i_{CC} WAVEFORM.

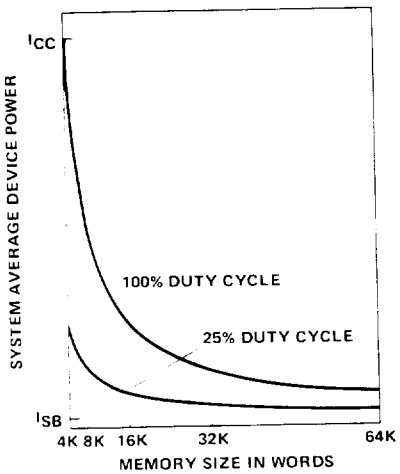


FIGURE 2. AVERAGE DEVICE DISSIPATION VS. MEMORY SIZE.

There is no functional constraint on the amount of time the 2141 is deselected. However, there is a relationship between deselect time and Chip Select access time. With no compensation, the automatic power switch would cause an increase in Chip Select access time, since some time is lost in repowering the device upon selection. A feature of the 2141 design is its ability to compensate for this loss. The amount of compensation is a function of deselect time, as shown in Figure 3. For short deselect times, Chip Select access time becomes slower than address access time, since full compensation typically requires 60ns. For longer deselect times, Chip Select access time actually becomes faster than address access time because the compensation more than offsets the time lost in powering up. The spec accounts for this characteristic by specifying two Chip Select access times, t_{ACS1} and t_{ACS2}.

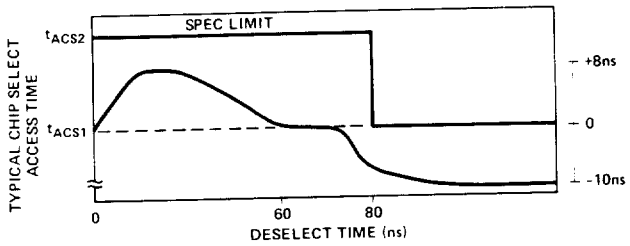


FIGURE 3. t_{ACS} VS. DESELECT TIME.

The power switching characteristic of the 2141 requires more careful decoupling than would be required of a constant power device. It is recommended that a 0.1μF ceramic capacitor be used on every other device, with a 22μF to 47μF bulk electrolytic decoupler every 32 devices. The actual values to be used will depend on board layout, trace widths and duty cycle. Power supply gridding is recommended for PC board layout. A very satisfactory grid can be developed on a two-layer board with vertical traces on one side and horizontal traces on the other, as shown in Figure 4.

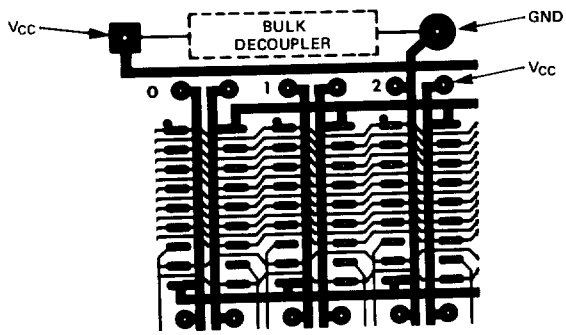
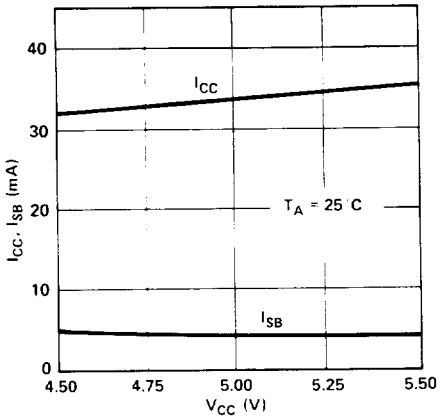


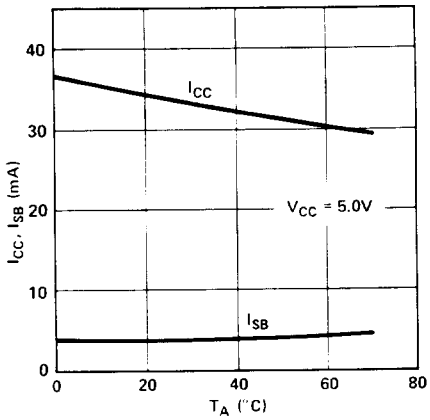
FIGURE 4. PC LAYOUT.

TYPICAL D.C. AND A.C. CHARACTERISTICS

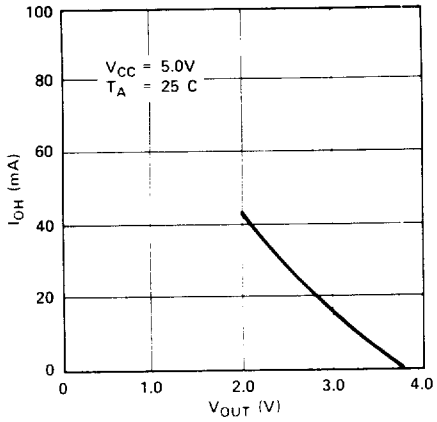
GRAPH 1
SUPPLY CURRENT VS.
SUPPLY VOLTAGE



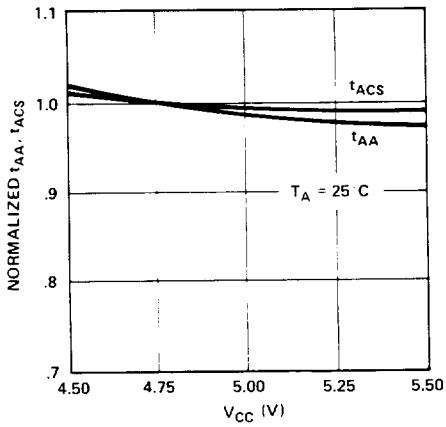
GRAPH 2
SUPPLY CURRENT VS.
AMBIENT TEMPERATURE



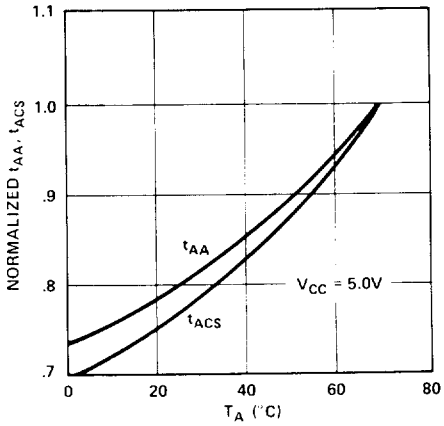
GRAPH 3
OUTPUT SOURCE CURRENT VS.
OUTPUT VOLTAGE



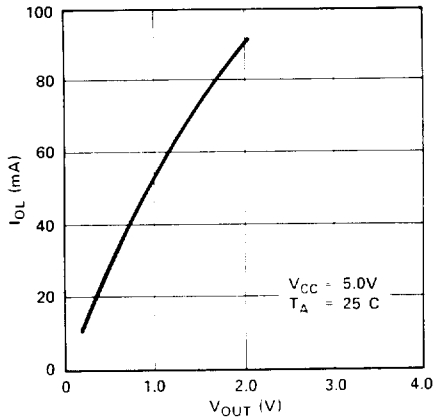
GRAPH 4
NORMALIZED ACCESS TIME
VS. SUPPLY VOLTAGE



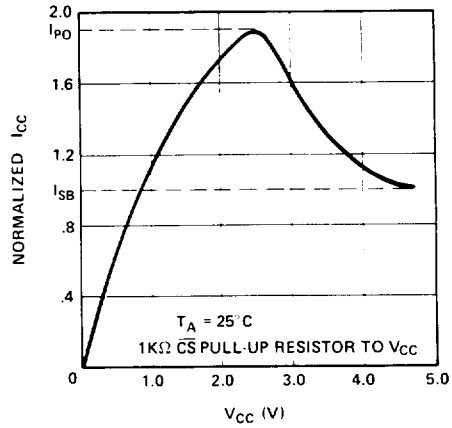
GRAPH 5
NORMALIZED ACCESS TIME VS.
AMBIENT TEMPERATURE



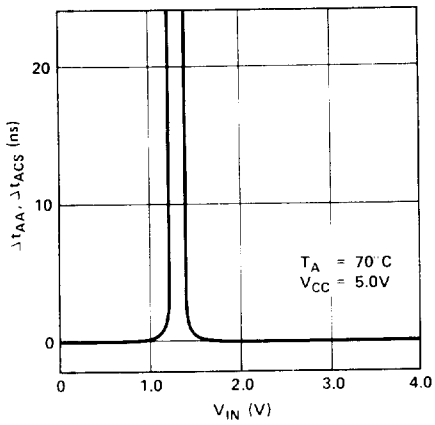
GRAPH 6
OUTPUT SINK CURRENT VS.
OUTPUT VOLTAGE



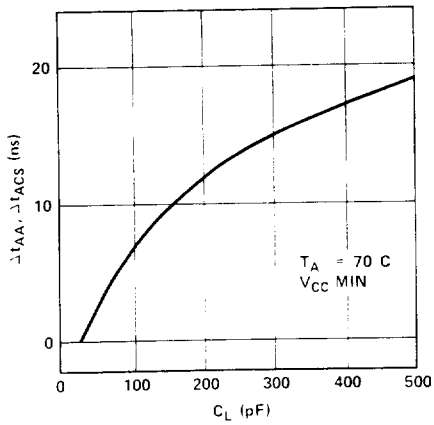
GRAPH 7
TYPICAL POWER-ON CURRENT
VS. POWER SUPPLY VOLTAGE



GRAPH 8
ACCESS TIME CHANGE VS.
INPUT VOLTAGE



GRAPH 9
ACCESS TIME CHANGE VS.
OUTPUT LOADING



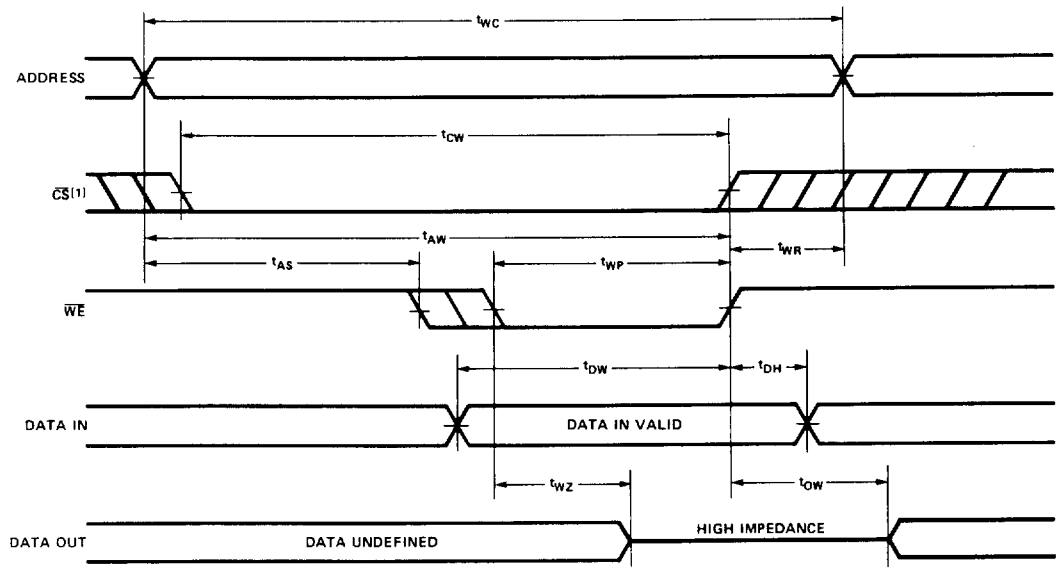
A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = +5V±10%, unless otherwise noted.

WRITE CYCLE

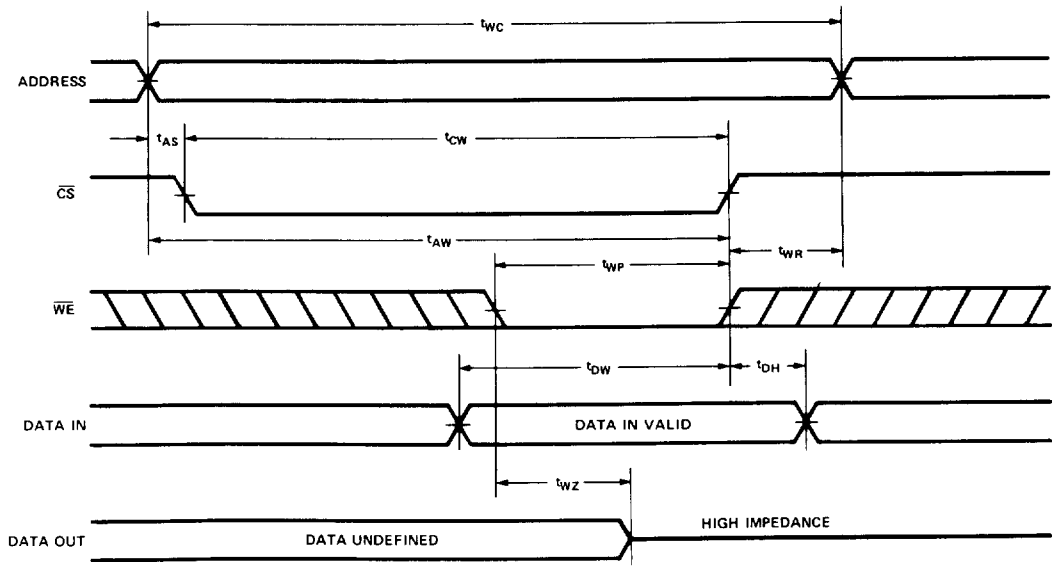
Symbol	Parameter	2141-2 Min.	2141-2 Max.	2141-3/L-3 Min.	2141-3/L-3 Max.	2141-4/L-4 Min.	2141-4/L-4 Max.	2141-5/L-5 Min.	2141-5/L-5 Max.	Unit
t_{WC}	Write Cycle Time	120		150		200		250		ns
t_{CW}	Chip Selection to End of Write	110		135		180		230		ns
t_{AW}	Address Valid to End of Write	110		135		180		230		ns
t_{AS}	Address Setup Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	60		60		60		75		ns
t_{WR}	Write Recovery Time	10		15		20		20		ns
t_{DW}	Data Valid to End of Write	50		60		60		75		ns
t_{DH}	Data Hold Time	5		5		5		5		ns
t_{WZ}	Write Enabled to Output in High Z	10	70	10	80	10	80	10	80	ns
t_{OW}	Output Active from End of Write	5		5		5		5		ns

WAVEFORMS

WRITE CYCLE #1 ($\overline{WE}$ CONTROLLED)



WRITE CYCLE #2 ($\overline{CS}$ CONTROLLED)



Note: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

A.C. CHARACTERISTICS

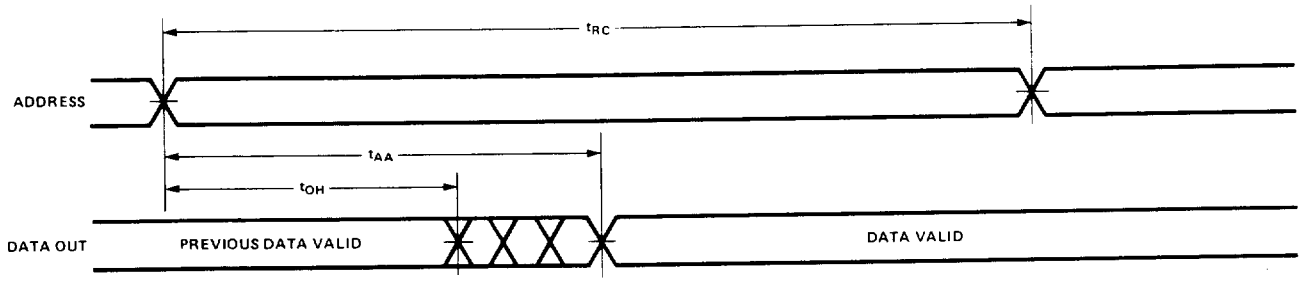
T_A = 0°C to 70°C, V_{CC} = +5V±10%, unless otherwise noted.

READ CYCLE

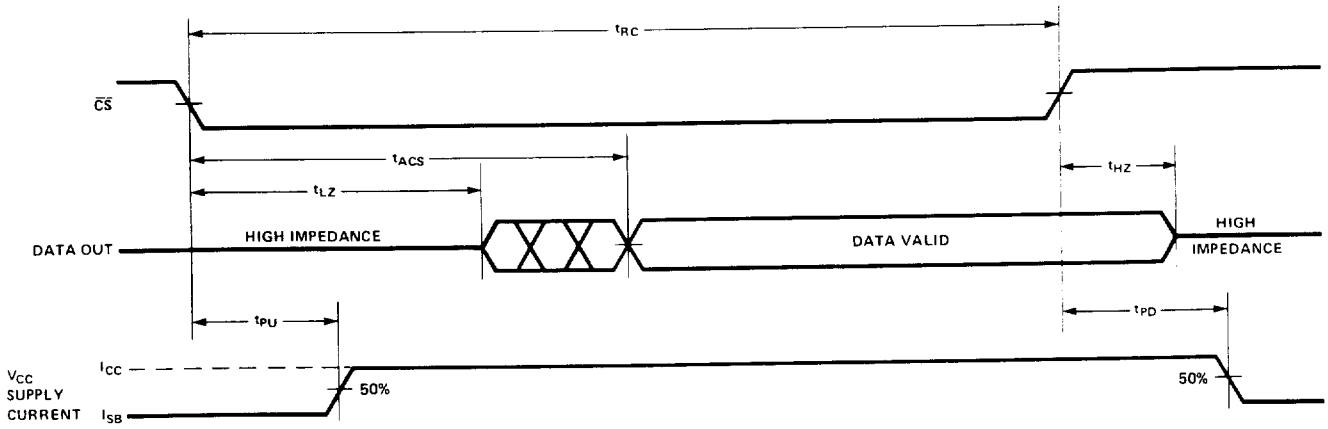
Symbol	Parameter	2141-2 Min.	2141-2 Max.	2141-3/L-3 Min.	2141-3/L-3 Max.	2141-4/L-4 Min.	2141-4/L-4 Max.	2141-5/L-5 Min.	2141-5/L-5 Max.	Unit
t_{RC}	Read Cycle Time	120		150		200		250		ns
t_{AA}	Address Access Time		120		150		200		250	ns
t_{ACS1}[1]	Chip Select Access Time		120		150		200		250	ns
t_{ACS2}[2]	Chip Select Access Time		130		160		200		250	ns
t_{OH}	Output Hold from Address Change	10		10		10		10		ns
t_{LZ}[3]	Chip Selection to Output in Low Z	30		30		30		30		ns
t_{HZ}[3]	Chip Deselection to Output in High Z	0	60	0	60	0	60	0	60	ns
t_{PU}	Chip Selection to Power Up Time	0		0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time		60		60		60		60	ns

WAVEFORMS

READ CYCLE NO. 1 [4,5]



READ CYCLE NO. 2 [4,6]



Notes:

1. Chip deselected for greater than 55ns prior to selection.
2. Chip deselected for a finite time that is less than 55ns prior to selection. (If the deselect time is 0ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
4. $\overline{WE}$ is high for Read Cycles.
5. Device is continuously selected, $\overline{CS}$ = V_{IL}.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to 85°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin With
Respect to Ground ..... -1.5V to +7V
Power Dissipation 1.2W
D.C. Output Current 20mA

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±10% unless otherwise noted.

Symbol	Parameter	2141-2/-3 Min.	2141-2/-3 Typ.[1]	2141-2/-3 Max.	2141-4/-5 Min.	2141-4/-5 Typ.[1]	2141-4/-5 Max.	2141L-3/L-4/L-5 Min.	2141L-3/L-4/L-5 Typ.[1]	2141L-3/L-4/L-5 Max.	Unit	Conditions
I_{LI}	Input Load Current (All Input Pins)		0.01	10		0.01	10		0.01	10	µA	V_{CC}=Max., V_{IN}= GND to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		0.1	10		0.1	10		0.1	10	µA	$\overline{CS}$=V_{IH}, V_{CC}=Max., V_{OUT}=GND to 4.5V
I_{CC}	Operating Current		45	70		40	55		30	40	mA	V_{CC}=Max., $\overline{CS}$=V_{IL}, Outputs Open
I_{SB}	Standby Current			20			12			5	mA	V_{CC}=Min. to Max., $\overline{CS}$=V_{IH}
I_{PO}[2]	Peak Power-On Current			40			30			18	mA	V_{CC}=GND to V_{CC} Min. $\overline{CS}$=Lower of V_{CC} or V_{IH} Min.
V_{IL}	Input Low Voltage	-1.0		0.8	-1.0		0.8	-1.0		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	2.0		6.0	V	
V_{OL}	Output Low Voltage			0.4			0.4			0.4	V	I_{OL} = 8.0mA
V_{OH}	Output High Voltage	2.4			2.4			2.4			V	I_{OH} = -4.0mA
I_{OS}[3]	Output Short Circuit Current	-120		120	-120		120	-120		120	mA	V_{OUT}=GND to V_{CC}

Notes: 1. Typical limits are at V_{CC} = 5V, T_A = +25°C, and specified loading.
2. I_{CC} exceeds I_{SB} maximum during power-on, as shown in Graph 7. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.
3. Duration not to exceed one minute.

A.C. TEST CONDITIONS

Input Pulse Levels	GND to 3.5 Volts
Input Rise and Fall Times	10 nsec
Input and Output Timing Reference Levels	1.5 Volts
Output Load	1 TTL Load plus 100pF

CAPACITANCE [4]

T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Max.	Unit	Conditions
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	6	pF	V_{OUT} = 0V

Note 4. This parameter is sampled and not 100% tested.

2141
4096 X 1 BIT STATIC RAM

	2141-2	2141-3	2141-4	2141-5	2141L-3	2141L-4	2141L-5
Max. Access Time (ns)	120	150	200	250	150	200	250
Max. Active Current (mA)	70	70	55	55	40	40	40
Max. Standby Current (mA)	20	20	12	12	5	5	5

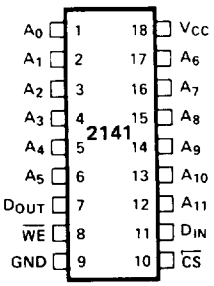
- **HMOS Technology**
- **Industry Standard 2147 Pinout**
- **Completely Static Memory — No Clock or Timing Strobe Required**
- **Equal Access and Cycle Times**
- **Single +5V Supply**
- **Automatic Power-Down**
- **Directly TTL Compatible — All Inputs and Output**
- **Separate Data Input and Output**
- **Three-State Output**
- **High Density 18-Pin Package**

The Intel® 2141 is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit using HMOS, a high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

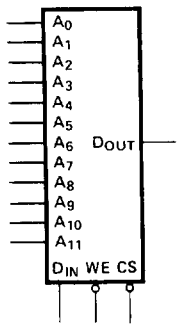
$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the 2141 — the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are de-selected.

The 2141 is placed in an 18-pin package configured with the industry standard pinout, the same as the 2147. It is directly TTL compatible in all respects: inputs, output, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

PIN CONFIGURATION



LOGIC SYMBOL



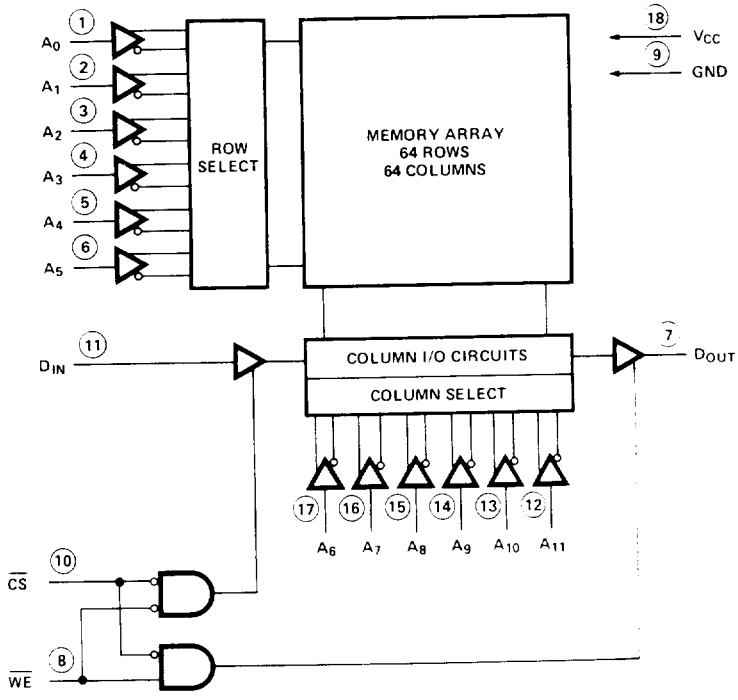
PIN NAMES

A_0–A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
D_{IN}	DATA INPUT		
D_{OUT}	DATA OUTPUT		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

BLOCK DIAGRAM



AUGUST 1978