256 BIT FULLY DECODED RANDOM ACCESS MEMORY

- **Access Time -- Typically Below 650 nsec - 1101A1, 850 nsec - 1101A**
- **Low Power Standby Mode**
- **Low Power Dissipation -- Typically less than 1.5 mW/bit during access**
- **Directly DTL and TTL Compatible**
- **Three-state Output -- OR-tie Capability**
- **Simple Memory Expansion -- Chip Select Input Lead**
- **Fully Decoded -- On Chip Address Decode and Sense**
- **Inputs Protected -- All Inputs Have Protection Against Static Charge**
- **Ceramic and Plastic Package -- 16 Pin Dual In-Line Configuration**

The 1101A is an improved version of the 1101 which requires only two power supplies (+5V and −9V) for operation. The 1101A is a direct pin for pin replacement for the 1101.

The Intel 1101A is a 256 word by 1 bit random access memory element using normally off P-channel MOS devices integrated on a monolithic array. It uses fully dc stable (static) circuitry and therefore requires no clocks to operate.

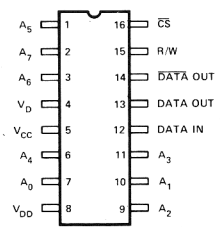
The 1101A is designed primarily for small buffer storage applications where high performance, low cost, and ease of interfacing with other standard logic circuits are important design objectives. The unit will directly interface with standard bipolar integrated logic circuits (TTL, DTL, etc.) The data output buffers are capable of driving TTL loads **directly**. A separate chip select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-tied.

For applications requiring a faster access time we recommend the 1101A1 which is a selection from the 1101A and has a guaranteed maximum access time of 1.0 μsec.

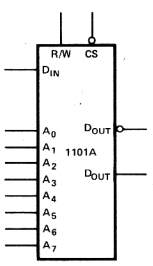
The Intel 1101A is fabricated with **silicon gate technology**. This **low threshold** technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

Intel's **silicon gate technology** also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

PIN CONFIGURATION



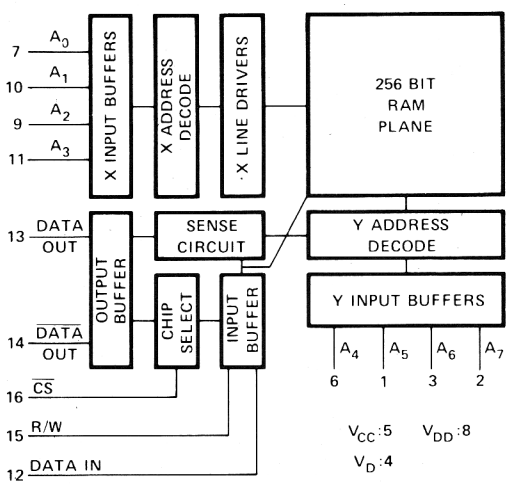
LOGIC SYMBOL



PIN NAMES

D_{IN}	DATA INPUT	$\overline{CS}$	CHIP SELECT
$A_0 - A_7$	ADDRESS INPUTS	D_{OUT}	DATA OUTPUT
R/W	READ/WRITE INPUT		

BLOCK DIAGRAM



Absolute Maximum Ratings[1]

Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +160°C
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{CC}	+0.5V to −20V
Supply Voltages V_{DD} and V_D with Respect to V_{CC}	−20V
Power Dissipation	1 WATT

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{DD} = −9V ± 5%, V_D = −9V ± 5%, unless otherwise specified

SYMBOL	TEST	MIN.	TYP.[2]	MAX.	UNIT	CONDITIONS
I_{LI}	**INPUT LOAD CURRENT** (ALL INPUT PINS)		**<1.0**	**500**	**nA**	**V_{IN} = 0.0 V**
I_{LO}	OUTPUT LEAKAGE CURRENT		<1.0	500	nA	V_{OUT} = 0.0 V, $\overline{CS}$ = V_{CC} −2
I_{DD1}	POWER SUPPLY CURRENT, V_{DD}		13	19	mA	T_A = 25°C
I_{DD2}	POWER SUPPLY CURRENT, V_{DD}			25	mA	T_A = 0°C
I_{D1}	POWER SUPPLY CURRENT, V_D		12	18	mA	T_A = 25°C,
I_{D2}	POWER SUPPLY CURRENT, V_D			24	mA	T_A = 0°C,
						Continuous Operation I_{OL} = 0.0 mA
V_{IL}	**INPUT "LOW" VOLTAGE**	**−10**		**V_{CC}−4.5**	**V**	
V_{IH}[3]	**INPUT "HIGH" VOLTAGE**	**V_{CC}−2**		**V_{CC}+0.3**	**V**	
I_{OLI}	OUTPUT SINK CURRENT	3.0	8		mA	V_{OUT} = +0.45 V, T_A = +25°C
I_{OL2}	OUTPUT SINK CURRENT	2.0			mA	V_{OUT} = +0.45 V, T_A = +70°C
I_{CF}	OUTPUT CLAMP CURRENT		6	13	mA	V_{OUT} = −1.0 V
I_{OHI}	OUTPUT SOURCE CURRENT	−3.0	−8		mA	V_{OUT} = 0.0 V, T_A = +25°C
I_{OH2}	OUTPUT SOURCE CURRENT	−2.0	−7		mA	V_{OUT} = 0.0 V, T_A = +70°C
V_{OL}	OUTPUT "LOW" VOLTAGE			+0.45	V	I_{OL} = 2.0 mA
V_{OH}	OUTPUT "HIGH" VOLTAGE	+3.5	+4.9		V	I_{OH} = −100μA
C_{IN}[4]	INPUT CAPACITANCE (ALL INPUT PINS)		7	10	pF	V_{IN} = V_{CC}
C_{OUT}[4]	OUTPUT CAPACITANCE		7	10	pF	V_{OUT} = V_{CC}
C_V[4]	V_D POWER SUPPLY CAPACITANCE		20	35	pF	V_D = V_{CC}
						f = 1 MHz, T_A = 25°C

Note 1: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are at nominal voltages and T_A = 25°C.

Note 3: A TTL driving the 1101A, 1101A1 must have its output high ≥ V_{CC}−2 even if it is loaded by other bipolar gates.

Note 4: This parameter is periodically sampled and is not 100% tested.

A.C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_D = −9V ± 5%, V_{DD} = −9V ± 5%

READ CYCLE

SYMBOL	TEST		MIN.	TYP.	MAX.	UNIT
t_{RC}	Read Cycle	1101A	1.5			µsec
		1101A1	1.0			µsec
t_{AC}	Address to Chip Select Delay	1101A			1.2(1)	µsec
		1101A1			0.7(1)	µsec
t_A	Access Time	1101A		0.85	1.5	µsec
		1101A1		0.65	1.0	µsec
t_{OH}	Previous Read Data Valid		0.05			µsec

WRITE CYCLE

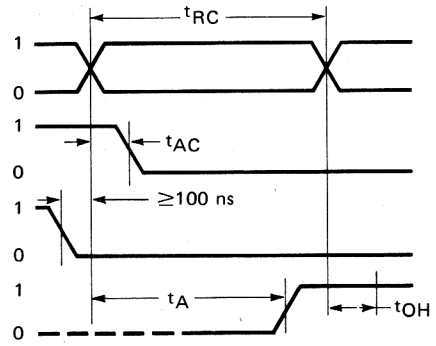
t_{WC}	Write Cycle	0.8			µsec
t_{WD}	Address to Write Pulse Delay	0.3			µsec
t_{WP}	Write Pulse Width	0.4			µsec
t_{DW}	Data Set up Time	0.3			µsec
t_{DH}	Data Hold Time	0.1			µsec

CHIP SELECT AND DESELECT

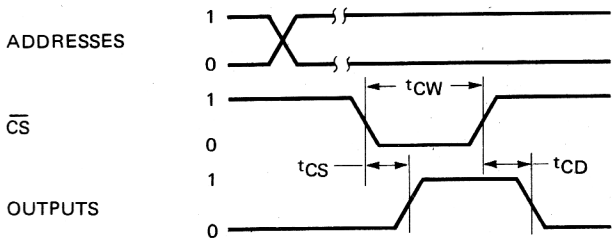
t_{CW}	Chip Select Pulse Width	0.4			µsec
t_{CS}	Access Time Through Chip Select Input		0.2	0.3	µsec
t_{CD}	Chip Deselect Time		0.1	0.3	µsec

CONDITIONS OF TEST:
Input pulse amplitudes: 0 to 5V, Input pulse rise and fall time: 10 nsec. Speed measurements referenced to 1.5V levels (unless otherwise noted). Output load is 1 TTL gate and C_L = 20 pF; measurements made at output of TTL gate ($t_{PD} \leq$ 10 nsec)

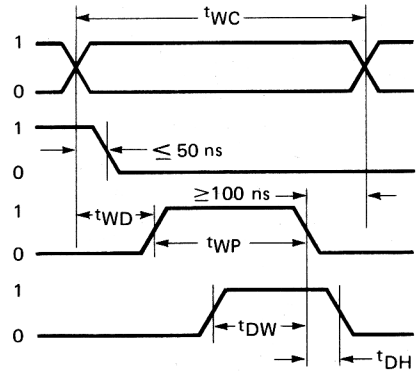
READ CYCLE



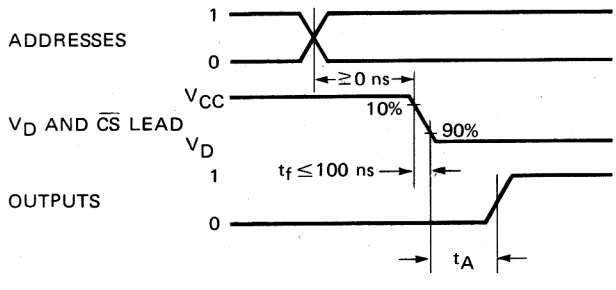
CHIP SELECT AND DESELECT



WRITE CYCLE



POWER SWITCHING OF V_D



V_{DD} = −9V ± 5%

Note 1: Maximum value for t_{AC} measured at minimum read cycle.

Absolute Maximum Ratings[1]

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Storage Temperature	−65°C to +160°C
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{CC}	+0.5V to −20V
Supply Voltages V_{DD} and V_D with Respect to V_{CC}	−20V
Power Dissipation	1 WATT

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{DD} = −9V ± 5%, V_D = −9V ± 5%, unless otherwise specified

SYMBOL	TEST	MIN.	TYP.[2]	MAX.	UNIT	CONDITIONS
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I_{DD1}	POWER SUPPLY CURRENT, V_{DD}		13	19	mA	T_A = 25°C
I_{DD2}	POWER SUPPLY CURRENT, V_{DD}			25	mA	T_A = 0°C
I_{D1}	POWER SUPPLY CURRENT, V_D		12	18	mA	T_A = 25°C,
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						Continuous Operation I_{OL} = 0.0 mA
V_{IL}	**INPUT "LOW" VOLTAGE**	**−10**		**V_{CC}−4.5**	**V**	
V_{IH}[3]	**INPUT "HIGH" VOLTAGE**	**V_{CC}−2**		**V_{CC}+0.3**	**V**	
I_{OL1}	OUTPUT SINK CURRENT	3.0	8		mA	V_{OUT} = +0.45 V, T_A = +25°C
I_{OL2}	OUTPUT SINK CURRENT	2.0			mA	V_{OUT} = +0.45 V, T_A = +70°C
I_{CF}	OUTPUT CLAMP CURRENT		6	13	mA	V_{OUT} = −1.0 V
I_{OH1}	OUTPUT SOURCE CURRENT	−3.0	−8		mA	V_{OUT} = 0.0 V, T_A = +25°C
I_{OH2}	OUTPUT SOURCE CURRENT	−2.0	−7		mA	V_{OUT} = 0.0 V, T_A = +70°C
V_{OL}	OUTPUT "LOW" VOLTAGE			+0.45	V	I_{OL} = 2.0 mA
V_{OH}	OUTPUT "HIGH" VOLTAGE	+3.5	+4.9		V	I_{OH} = −100μA
C_{IN}[4]	INPUT CAPACITANCE (ALL INPUT PINS)		7	10	pF	V_{IN} = V_{CC}
C_{OUT}[4]	OUTPUT CAPACITANCE		7	10	pF	V_{OUT} = V_{CC}
C_V[4]	V_D POWER SUPPLY CAPACITANCE		20	35	pF	V_D = V_{CC}
						f = 1 MHz, T_A = 25°C

Note 1: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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