64KX4 Bit High-Speed CMOS Static RAM (Sep. I/O)

FEATURES

- Fast Access Time: 15, 20, 25ns (max.): KM64259B
  20, 25ns (max.): KM64260B
- Low Power Dissipation
  Standby (TTL) : 40mA (max.)
  (CMOS): 2mA (max.)
  Operating: 15ns: 140mA (max.): KM64259B only
  20ns: 130mA (max.)
  25ns: 120mA (max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  —No clock or refresh required
- Three State Outputs
- Standard Pin Configuration
  KM64259BP/KM64260BP: 28-pin DIP (300 mil.)
  KM64259BJ/KM64260BJ: 28-pin SOJ (300 mil.)

GENERAL DESCRIPTION

The KM64259B and KM64260B are a 262,144-bit high-speed Static Random Access Memory organized as 65,536 words by 4 bits.

The KM64259B and KM64260B have seperate input and output lines for fast read and write access. The data output pins stay in High-Z state when write enable is low (KM64259B only), or chip select is high.

The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology.

It is particularly well suited for use in high-density high-speed system applications.

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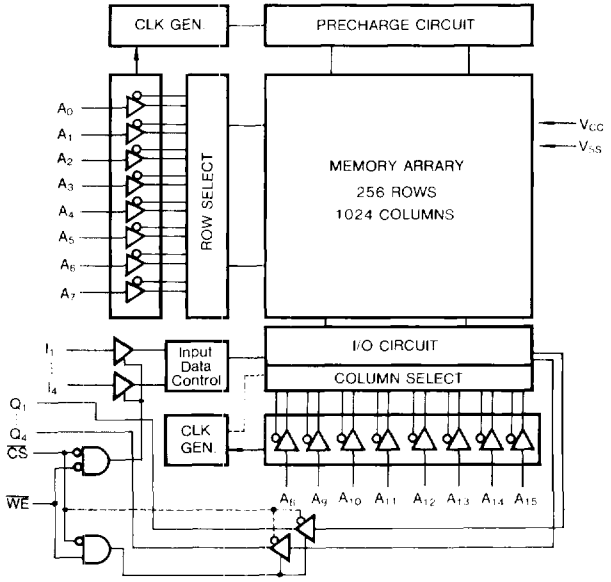
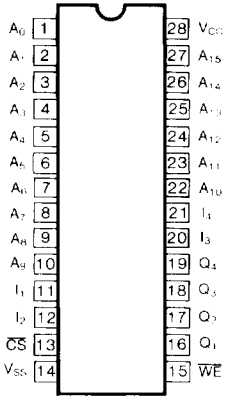
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{15}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$I_1 \sim I_4$	Data Inputs
$Q_1 \sim Q_4$	Data Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260°C, 10sec (Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.)=−3.0V for ≤10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}				2	μA
Output Leakge Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL}. $V_{I/O}$=V_{SS} to V_{CC}				2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{OUT}=0mA	15ns			140	mA
			20ns			130	mA
			25ns			120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}				40	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}−0.2V, V_{IN}≥V_{CC}−0.2Vor V_{IN}≤0.2V				2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA				0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4.0mA		2.4			V

* Typ: V_{CC}=5V, T_A=25°C

CAPACITANCE* (f=1MHz, T_A=25°C)

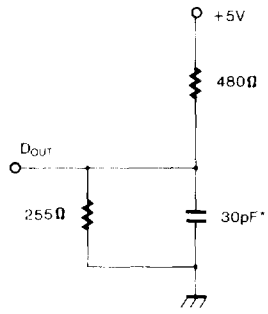
Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	7	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	7	pF

AC CHARACTERISTICS

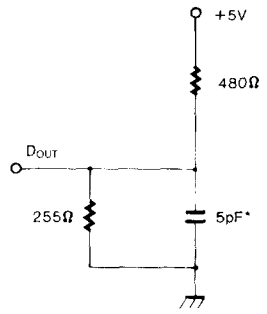
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ} & t_{OW})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM64259BP/J-15		KM64259BP/J-20 KM64260BP/J-20		KM64259BP/J-25 KM64260BP/J-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		20		25		ns
Address Access Time	t_{AA}		15		20		25	ns
Chip Select to Output	t_{CO}		15		20		25	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		ns
Chip Disable to High-Z Output	t_{HZ}	0	10	0	10	0	10	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Chip Select to Power Up Time	t_{PU}	0		0		0		ns
Chip Disable to Power Down Time	t_{PD}		15		20		25	ns

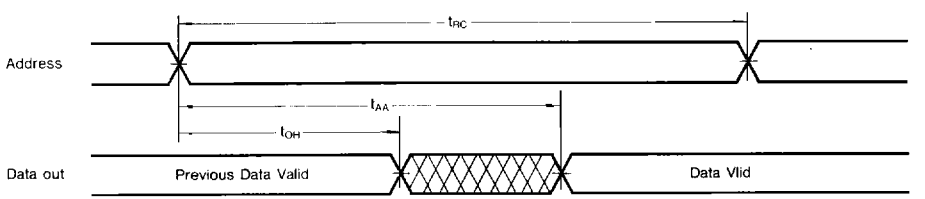
WRITE CYCLE

Parameter	Symbol	KM64259BP/J-15		KM64259BP/J-20 KM64260BP/J-20		KM64259BP/J-25 KM64260BP/J-25		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		20		25		ns
Chip Select to End of Write	t_{CW}	12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	12		13		15		ns
Write Pulse Width	t_{WP}	12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Data to Write Time Overlap	t_{DW}	8		10		13		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
Write to Output High-Z (KM64259B)	t_{WHZ}	0	8	0	9	0	10	ns
End Write to Output Low-Z (KM64259B)	t_{OW}	0		0		0		ns
Data Valid to Output Valid (KM64260B)	t_{DO}				20		25	ns
Write to Output Valid (KM64260B)	t_{WO}				18		20	ns

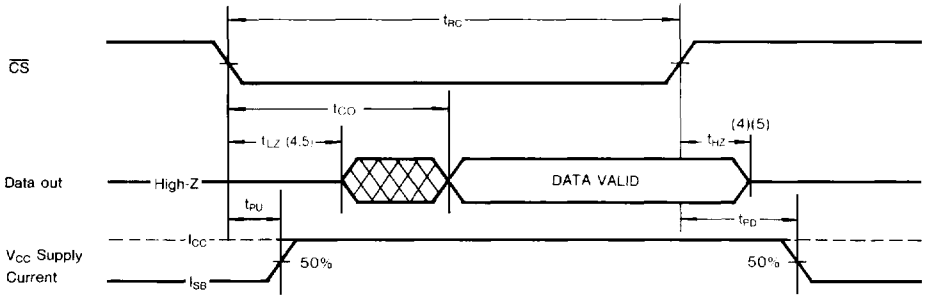
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=V_{IL}, $\overline{WE}$=V_{IH})



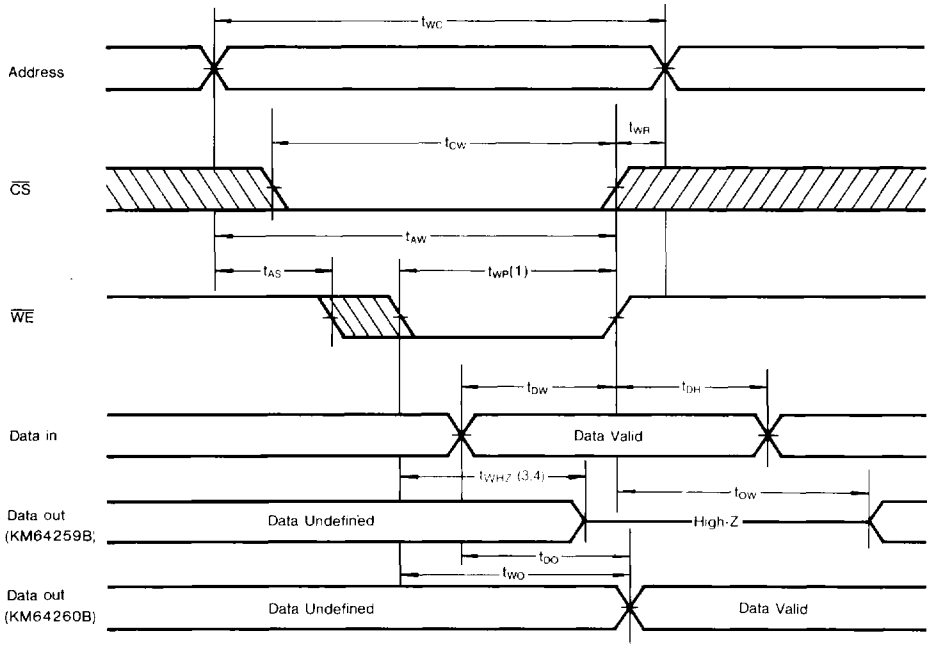
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



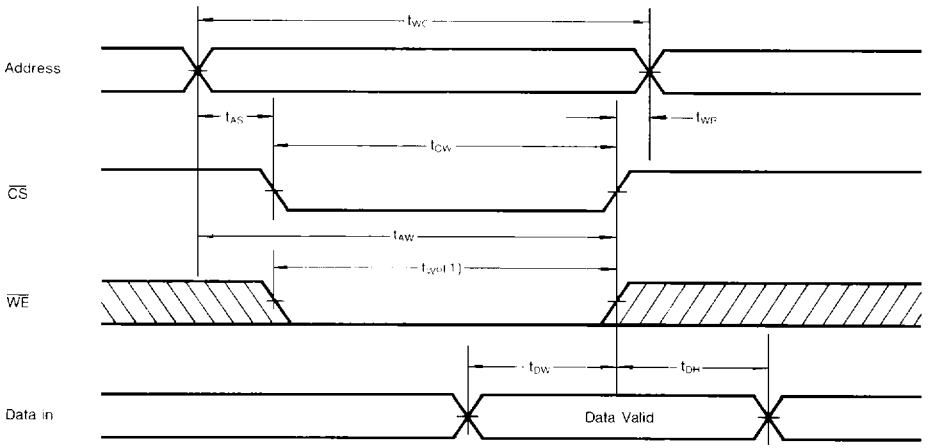
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (b).
5. This parameter is sampled and not 100% tested.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Note (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load (B).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WHZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

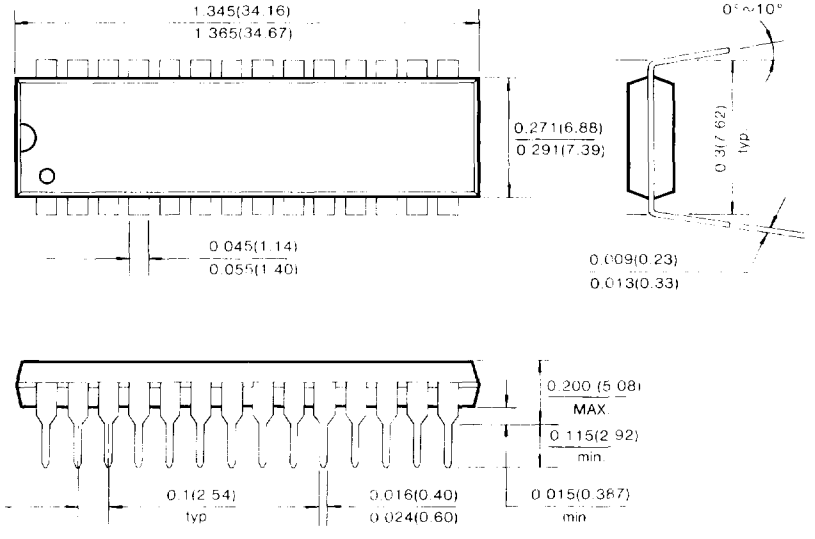
$\overline{CS}$	$\overline{WE}$	Mode	D_{OUT} Pin	Supply Current
H	X**	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	Read	D_{OUT}	I_{CC}
L	L	Write*	High-Z (KM64259B) D_{OUT} (KM64260B)	I_{CC}

* Write cycle timing controlled by write enable ($\overline{WE}$)
** X means Don't Care

PACKAGE DIMENSIONS

28 PIN PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (Millimeters)



28 PIN PLASTIC SMALL OUT LINE J FORM PACKAGE