

T-46-13-27



ER5911

1K (128 x 8 or 64 x 16) Serial Electrically Erasable PROM

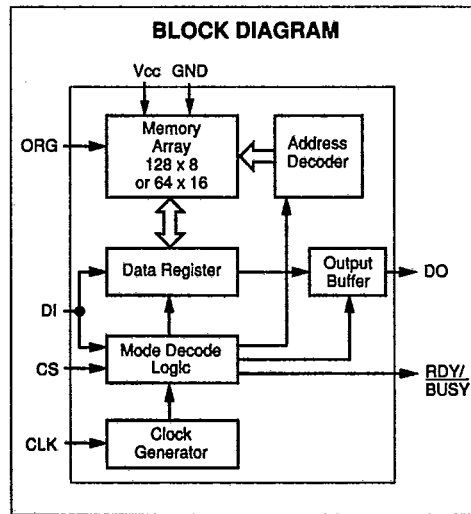
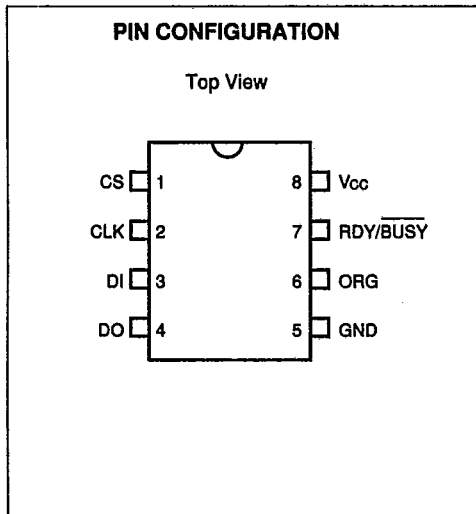


FEATURES

- User-selectable organization: 64 x 16 or 128 x 8
- Single +5V only operation
- Binary addressing
- Fully automatic self-timed erase/write mode
- Word and chip erasable
- Unlimited read accesses
- Fully TTL compatible inputs and outputs
- ESD Protection: Inputs are designed to meet 1.0kV per test method 3015.1, MIL-STD 883
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word
- Power-on/off data protection circuitry
- Available for extended temperature ranges:
 - Commercial: 0°C to 70°C
 - Industrial: -40°C to 85°C

DESCRIPTION

The ER5911 is a low cost, serial EEPROM manufactured in Microchip's highly reliable SNOS technology. This device features +5V only operation, a self-timed reprogramming cycle and two user-selectable memory array organizations, 64 x 16 or 128 x 8, which are selectable externally by means of a one bit code applied to control pin ORG. The Input (DI) and Output (DO) pins are controlled by separate serial formats. When separate lines are used the DO output pin is valid only in the read mode and is in the high impedance state in all other modes, thus eliminating bus contention. Five instructions may be executed and the instruction length will be twelve bits when using the 128 x 8 organization and eleven bits when the 64 x 16 organization is used. The instruction format has a logical 1 as a start a bit, four bits as an opcode and either six or seven address bits.



ER5911

T-46-13-27

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

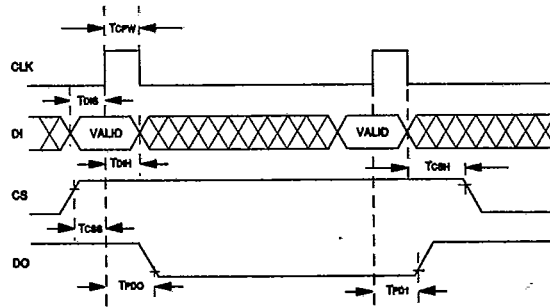
All inputs and outputs with respect to ground +7V to -0.3V
 Storage temperature (unpowered and without data retention) -65°C to +150°C
 Ambient temperature with power applied -65°C to +125°C
 Soldering temperature of leads (10 seconds) +300°C
 ESD protection on all pins 1.0kV (typ.)

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

| PIN FUNCTION TABLE | |
|--------------------|---------------------------|
| Name | Function |
| CS | Chip Select |
| CLK | Clock Input |
| DI | Serial Data Input |
| DO | Serial Data Output |
| Vcc | +5V Power Supply |
| RDY/BUSY | Status Output |
| GND | Ground |
| ORG | Memory Array Organization |

| DC CHARACTERISTICS | | Vcc = +5V +10% Commercial: Tamb = 0°C to 70°C Industrial: Tamb = -40°C to +85°C | | | | | |
|--------------------------------------|-----------------|---|-----|---------|----|-------|-------------------------------|
| Characteristic | Sym | Min | Typ | Max | | Units | Conditions |
| | | | | C | I | | |
| Input Voltage | | | | | | | |
| High Level | V _{IH} | 2.0 | — | Vcc+1.0 | | V | |
| Low Level | V _{IL} | -0.3 | — | +0.8 | | V | |
| Output Voltage | | | | | | | |
| High Level | V _{OH} | 2.4 | — | Vcc | | V | I _{OH} = -400µA |
| Low Level | V _{OL} | — | — | 0.4 | | V | I _{OL} = 1.6mA |
| Leakage Current | | | | | | | |
| Input | I _{LI} | — | — | +10 | | µA | V _{IN} = GND to Vcc |
| Output | I _{LO} | — | — | +10 | | µA | V _{OUT} = GND to Vcc |
| Current | | | | | | | |
| Chip Selected | I _{CC} | — | — | 10 | 12 | mA | Vcc = 5.5V |
| Chip Selected (PROGRAM & ERAL modes) | I _{CC} | — | — | 12 | 15 | mA | Vcc = 5.5V |
| Chip Deselected (Standby) | I _{CC} | — | — | 3 | 5 | mA | Vcc = 5.5V |
| Power Consumption | | | | | | | |
| Chip Selected | P _{CC} | — | — | 55 | 66 | mW | Vcc = 5.5V |
| Chip Selected (PROGRAM & ERAL modes) | P _{CC} | — | — | 66 | 83 | mW | Vcc = 5.5V |
| Chip Deselected (STANDBY) | P _{CC} | — | — | 17 | 28 | mW | Vcc = 5.5V |

FIGURE 1 - SYNCHRONOUS DATA TIMING



| AC CHARACTERISTICS (See Figure 1) | | | | | | |
|------------------------------------|------|-----|-----|-----|-------|------------------------|
| Characteristic | Sym | Min | Typ | Max | Units | Conditions |
| CLK Frequency | fCLK | 0 | — | 250 | KHZ | CL = 100pf |
| CLK Duty Cycle | DCLK | 25 | — | 75 | % | VO _L = 0.8V |
| Chip Select Setup Time | tCSS | 0.2 | — | — | μS | VO _H = 2.0V |
| Chip Select Hold Time | tCSH | 0 | — | — | μS | CL = 100pf |
| Data Input Setup Time | tDIS | 0.4 | — | — | μS | VO _L = 0.8V |
| Data Input Hold Time | tDIH | 0.4 | — | — | μS | VO _H = 2.0V |
| CLK Pulse Width | tCPW | 2.0 | — | — | μS | |
| Data Output Delay | tPD1 | - | — | 2.0 | μS | |
| Data Output Delay | tPDO | - | — | 2.0 | μS | |
| Status Low Time (programming time) | tPR | 20 | 40 | 75 | ms | |

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and puts it into standby mode.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the ER5911. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK is a Don't Care if CS is LOW (device deselected). If CS is HIGH but a start condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e. waiting for start condition).

CLK cycles are not required during the self timed PROGRAM (i.e. auto erase/write) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table).

Data In (DI)

Data In is used to clock in Start bit, opcode, address and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (T_{PD0} after the positive edge of CLK). This output is in High-Z mode except if data is clocked out as a result of a READ instruction.

DI and DO can be connected together to perform a 3-wire interface (CS, CLK, DI/DO).

Care must be taken with the leading dummy zero which is output after a READ command has been detected. Also, the controlling device must not drive the DI/DO bus during ERAL and PROGRAM cycles.

Organization (ORG)

ORG is the Memory Array Organization Selection Input. When the ORG pin is connected to +5V the 64 x 16 organization is selected. When it is connected to ground the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64 x 16 organization.

Ready/Busy (RDY/BSY)

Pin 7 provides RDY/BSY status information. RDY/BSY is low if the device is performing a PROGRAM or ERAL operation. When it is high, the internal self-timed PROGRAM or ERAL operation has been completed, and the device is ready to receive a new instruction.

POWER-ON DATA PROTECTION CIRCUITRY

During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

FUNCTIONAL DESCRIPTION

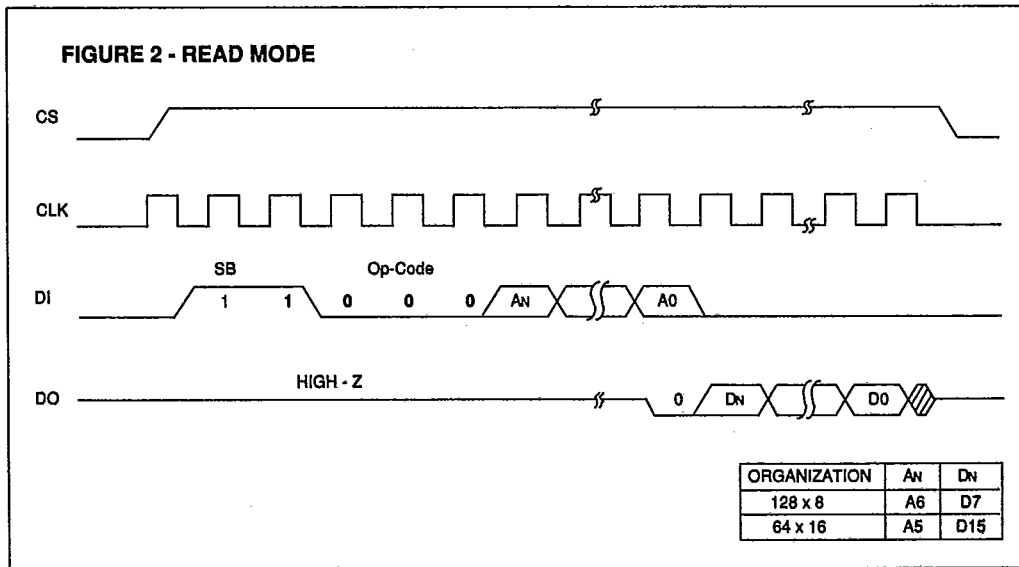
| INSTRUCTION SET | | | | | | | |
|-----------------|-----------|--------|---------|---------|---------|---------|-----------------------|
| Instruction | Start Bit | Opcode | Address | | Data | | Comments |
| | | | 128 x 8 | 64 x 16 | 128 x 8 | 64 x 16 | |
| READ | 1 | 1000 | A6-A0 | A5-A0 | | | Read Address AN-A0 |
| PROGRAM | 1 | X100 | A6-A0 | A5-A0 | D7-D0 | D15-D0 | Program Address AN-A0 |
| PEN | 1 | 0011 | 0000000 | 0000000 | | | Program Enable |
| PDS | 1 | 0000 | 0000000 | 0000000 | | | Program Disable |
| ERAL | 1 | 0010 | 0000000 | 0000000 | | | Erase All Addresses |

Data In/ Data Out (DI/DO)

It is possible to connect the Data In and Data out pins together. However, with this configuration it is possible for a "but conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

Read Mode

The READ instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a serial-out shift register. A dummy bit (logical "0") precedes the data output string. The output data changes during the high states of the system clock.



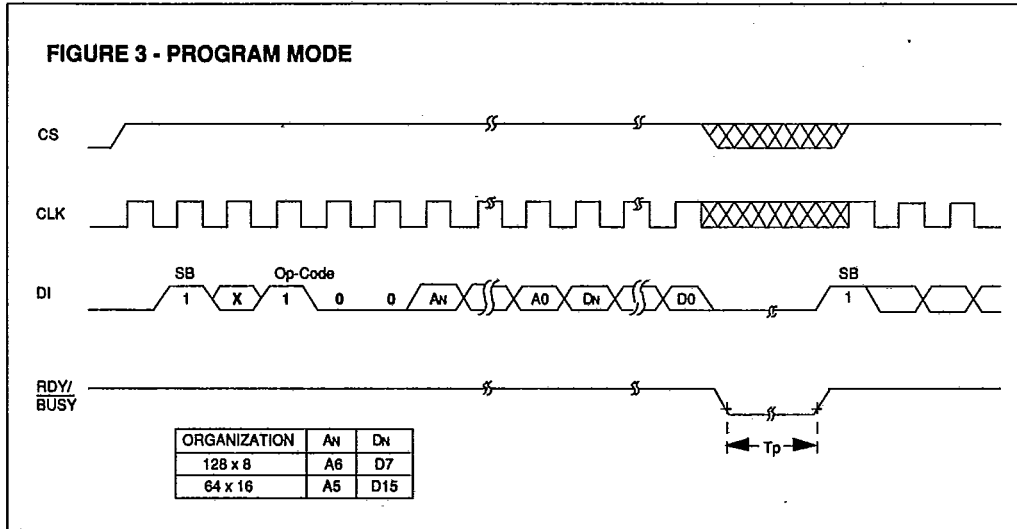
Program Mode

The PROGRAM instruction is followed by either eight or sixteen bits of data, which are to be written into the specified address.

After the last data bit (D0) has been shifted into the data register the contents of the specified address will be erased and the new data written to the same address.

During the automatic erase/write sequence the RDY/BUSY output will go low for the duration of the automatic programming cycle as indicated by T_p .

During a program cycle the internal erase and write operations occur automatically and are self-timed on the device. A single memory location may also be erased by programming that address with all "1's".



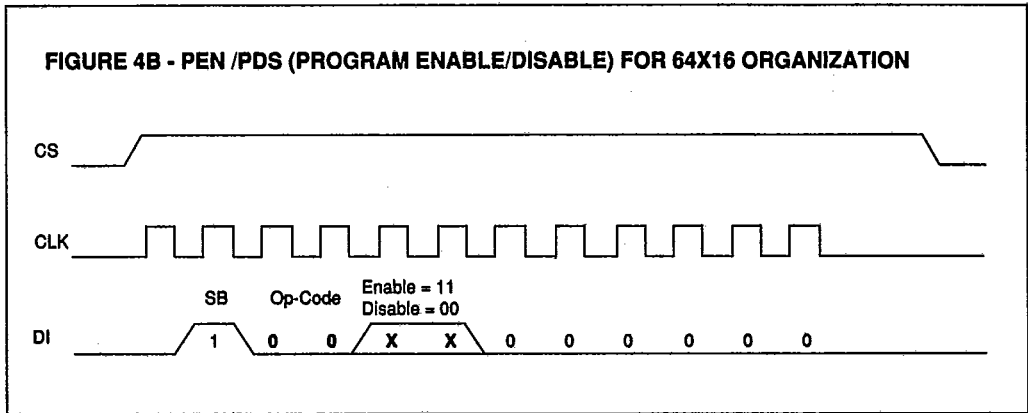
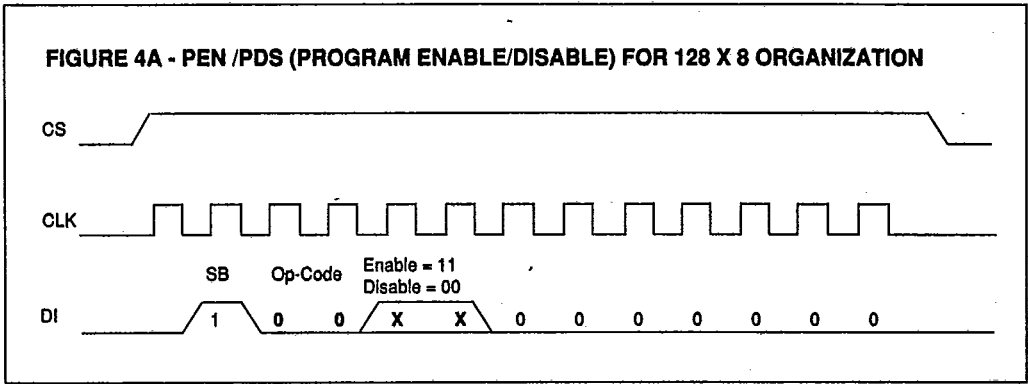
ER5911

T-46-13-27

Program Enable and Program Disable (PEN/PDS)

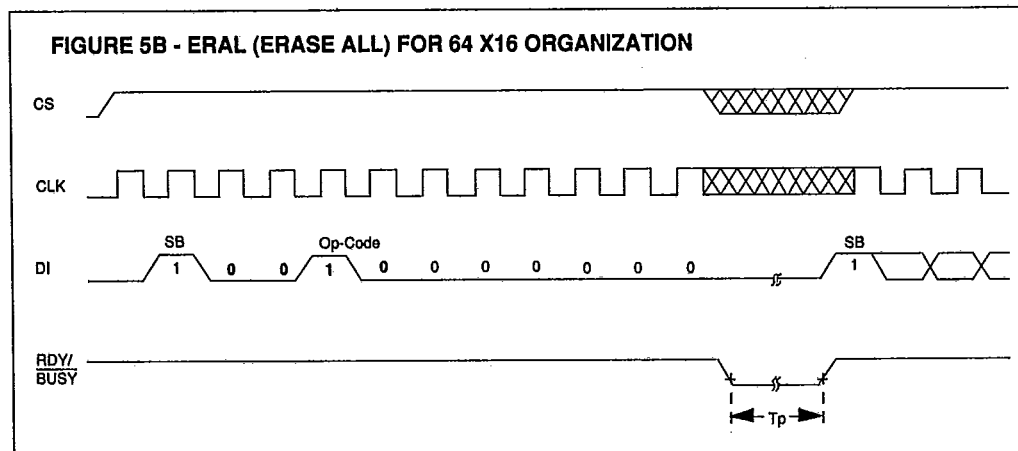
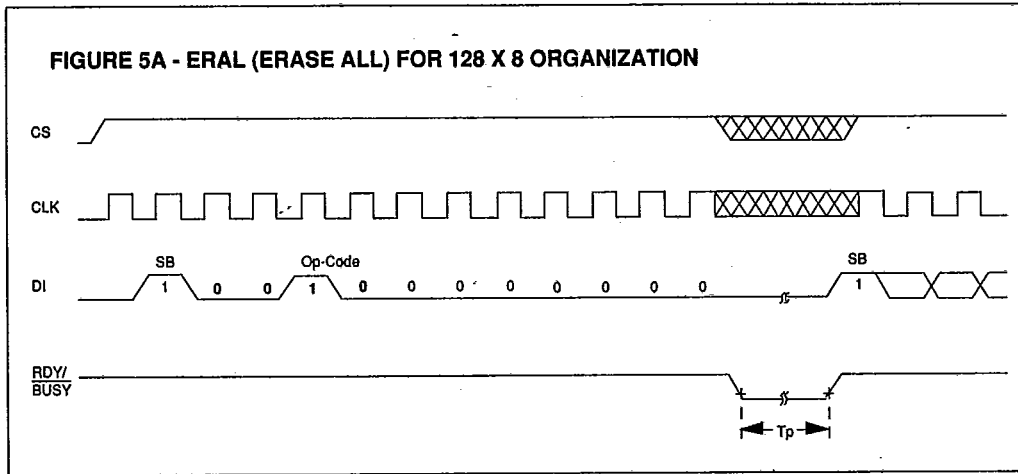
Programming must be preceded once by a programming enable (PEN) instruction. Programming remains enabled until a programming disable (PDS) instruction is executed. The programming disable instruction is pro-

vided to protect against accidental data disturb. Execution of a READ instruction is independent of both PEN and PDS instructions.



Chip Erase (ERAL)

Entire chip erasing is provided for ease of programming and is implemented with the ERAL (erase all registers) instruction. Erasing the chip means that all registers in the memory array have each bit set to a 1.



ER5911

T-46-13-27

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

ER5911 - I / P

| | | |
|--------------------|----------------------------|-----------------------------|
| Package: | J | CERDIP |
| | P | Plastic DIP (OTP Available) |
| Temperature Range: | Blank | 0° C to 70° C |
| | I | -40° C to 85° C |
| Device | 5911 1K SNOS Serial EEPROM | |