



# 32K x 8 High-Speed CMOS EPROM

## Features

- CMOS for optimum speed/power
- High speed
  - $t_{AA} = 25$  ns max. (commercial)
  - $t_{AA} = 35$  ns max. (military)
- Low power
  - 275 mW max.
  - Less than 85 mW when deselected
- Byte-wide memory organization
- 100% reprogrammable in the windowed package
- EPROM technology
- Capable of withstanding >2001 V static discharge
- Available in
  - 32-pin PLCC
  - 28-pin TSOP-I
  - 28-pin, 600-mil plastic or hermetic DIP
  - 32-pin hermetic LCC

## Functional Description

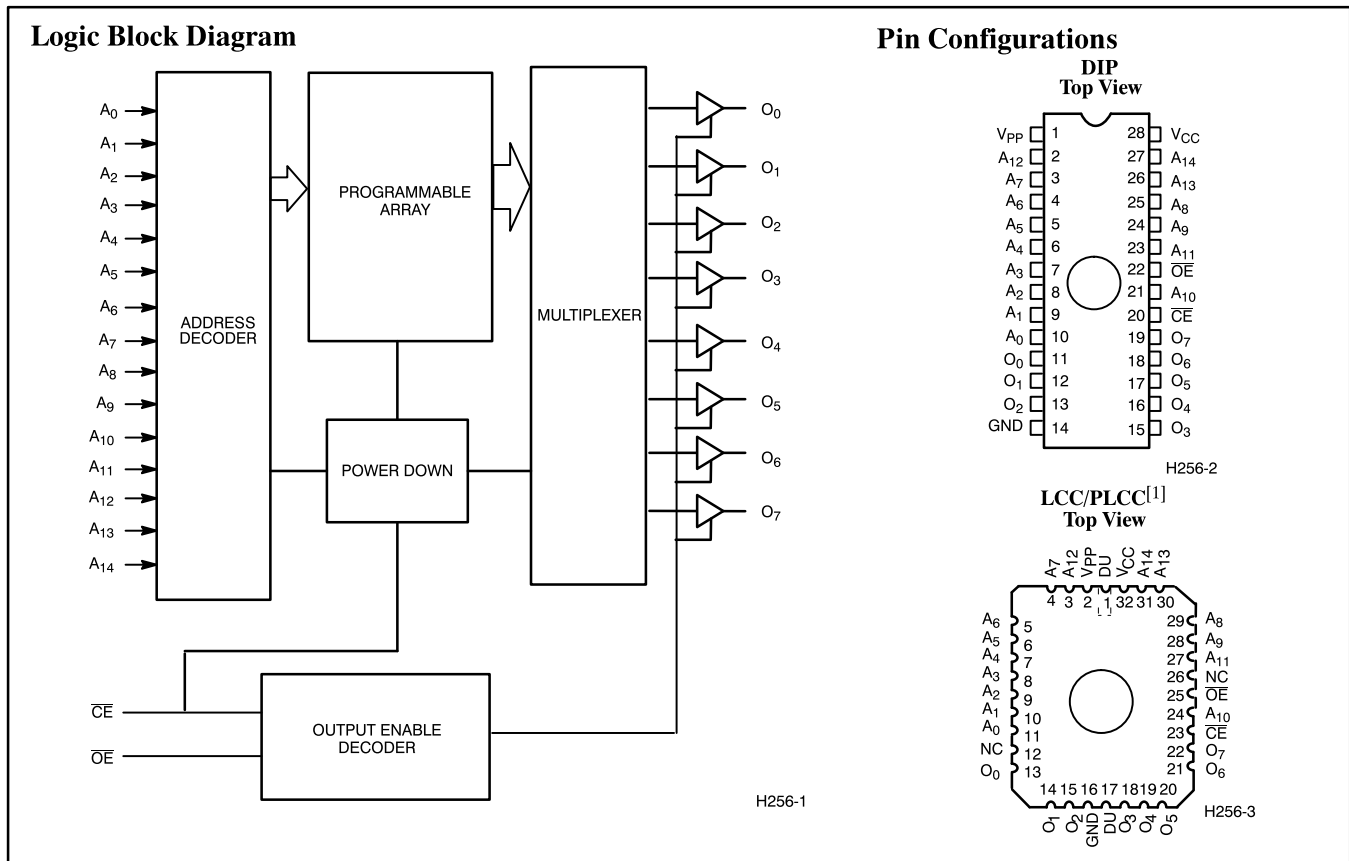
The CY27H256 is a high-performance, 256K CMOS EPROM organized in 32 Kbytes. It is available in industry-standard 28-pin, 600-mil DIP, 32-pin LCC and PLCC, and 28-pin TSOP-I packages. These devices offer high-density storage combined with 40-MHz performance. The CY27H256 is available in windowed and opaque packages. Windowed packages allow the device to be erased with UV light for 100% reprogrammability.

The CY27H256 is equipped with a power-down chip enable ( $\overline{CE}$ ) input as well as an output enable ( $\overline{OE}$ ) input. When  $\overline{CE}$  is deasserted, the device powers down to a low-power stand-by mode. The  $\overline{OE}$  pin three-states the outputs without putting the device into stand-by mode. While  $\overline{CE}$  offers lower power,  $\overline{OE}$  provides a more

rapid transition to and from three-stated outputs.

The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms. The EPROM cell requires only 12.75 V for the supervoltage and low programming current allows for gang programming. The device allows for each memory location to be tested 100%, because each location is written to, erased, and repeatedly exercised prior to encapsulation. Each device is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

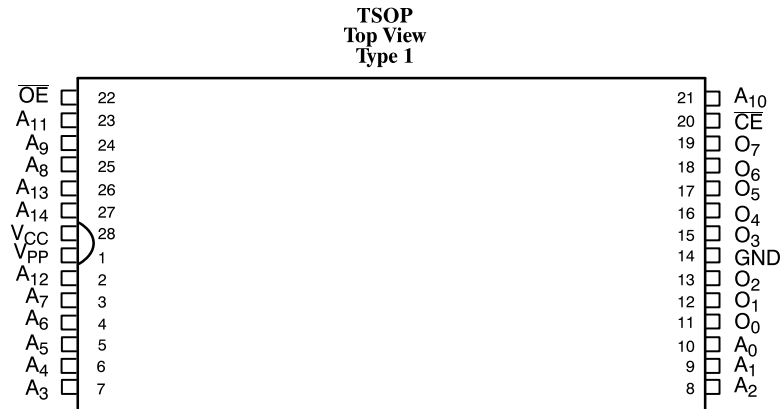
The CY27H256 is read by asserting both the  $\overline{CE}$  and the  $\overline{OE}$  inputs. The contents of the memory location selected by the address on inputs  $A_{14}-A_0$  will appear at the outputs  $O_7-O_0$ .



**Note:**

1. For LCC/PLCC only: Pins 1 and 17 are common and tied to the die attach pad. They should not be used.

Pin Configurations (continued)



H256-4

**Selection Guide**

		27H256-25	27H256-30	27H256-35	27H256-45	27H256-55	27H256-70
Maximum Access Time (ns)		25	30	35	45	55	70
$\overline{CE}$ Access Time (ns)	Com'l	30	35	35	45	55	70
	Mil			40	45	55	70
$\overline{OE}$ Access Time (ns)	Com'l	12	15	15	15	20	25
	Mil			20	20	20	25
$I_{CC}^{[2]}$ (mA) Power Supply Current	Com'l	75	75	50	50	50	50
	Mil			85	60	60	60
$I_{SB}^{[3]}$ (mA) Stand-by Current	Com'l	15	15	15	15	15	15
	Mil			25	25	25	25

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature .....  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$
- Ambient Temperature with Power Applied .....  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Supply Voltage to Ground Potential .....  $-0.5\text{V}$  to  $+7.0\text{V}$
- DC Voltage Applied to Outputs in High Z State .....  $-0.5\text{V}$  to  $+5.5\text{V}$
- DC Input Voltage .....  $-3.0\text{V}$  to  $+7.0\text{V}$
- Transient Input Voltage .....  $-3.0\text{V}$  for  $< 20\text{ ns}$
- DC Program Voltage .....  $13.0\text{V}$

**Notes:**

- 2.  $V_{CC} = \text{Max.}$ ,  $I_{OUT} = 0\text{ mA}$ ,  $f = 10\text{ MHz}$ .
- 3.  $V_{CC} = \text{Max.}$ ,  $\overline{CE} = V_{IH}$ .

- UV Erasure .....  $7258\text{ Wsec/cm}^2$
- Static Discharge Voltage .....  $>2001\text{V}$   
(per MIL-STD-883, Method 3015)
- Latch-Up Current .....  $>200\text{ mA}$

**Operating Range**

Range	Ambient Temperature	$V_{CC}$
Commercial	$0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	$5\text{V} \pm 10\%$
Industrial <sup>[4]</sup>	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	$5\text{V} \pm 10\%$
Military <sup>[5]</sup>	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	$5\text{V} \pm 10\%$

- 4. Contact a Cypress representative for industrial temperature range specification.
- 5.  $T_A$  is the "instant on" case temperature.



**Electrical Characteristics** Over the Operating Range<sup>[6, 7]</sup>

Parameter	Description	Test Conditions	27H256-25 27H256-30		27H256-35		27H256-45 27H256-55 27H256-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = - 4.0 mA	2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 12.0 mA		0.45		0.45		0.45	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs	2.0	V <sub>CC</sub> +0.5	2.0	V <sub>CC</sub> +0.5	2.0	V <sub>CC</sub> +0.5	V
V <sub>IL</sub>	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		0.8		0.8		0.8	V
I <sub>Ix</sub>	Input Leakage Current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-10	+10	-10	+10	-10	+10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disable	-10	+10	-10	+10	-10	+10	μA
I <sub>CC</sub>	Power Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=10 MHz	Com'l	75		50		50	mA
			Mil				85		60
I <sub>SB</sub>	Stand-By Current	V <sub>CC</sub> =Max., CE = V <sub>IH</sub>	Com'l	15		15		15	mA
			Mil				25		25

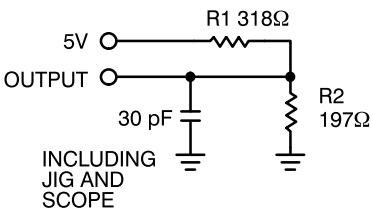
**Capacitance**<sup>[7]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

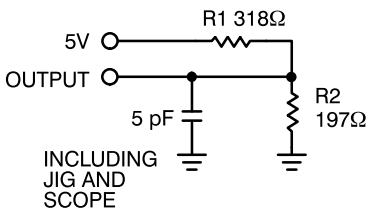
**Notes:**

- 6. See the last page of this specification for Group A subgroup testing information.
- 7. See Introduction to CMOS PROMs in this Data Book for general information on testing.

**AC Test Loads and Waveforms**

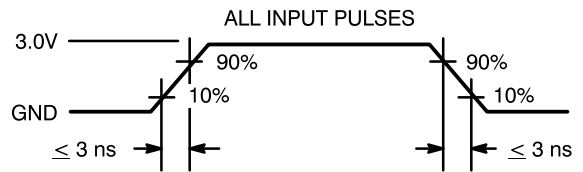


(a) Normal Load



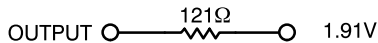
(b) High-Z Load

H256-5



H256-6

Equivalent to: THÉVENIN EQUIVALENT

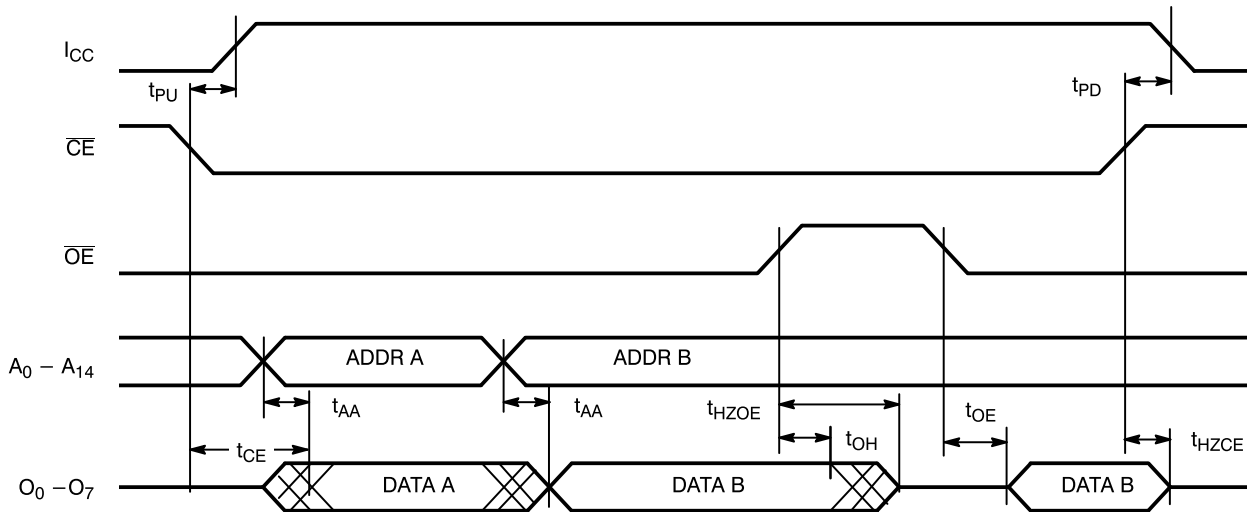




Switching Characteristics Over the Operating Range

Parameter	Description	27H256-25		27H256-30		27H256-35		27H256-45		27H256-55		27H256-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{AA}$	Address to Output Valid		25		30		35		45		55		70	ns
$t_{OE}$	$\overline{OE}$ Active to Output Valid		12		15		15		15		20		25	ns
$t_{HZOE}$	$\overline{OE}$ Inactive to High Z		12		15		15		15		20		25	ns
$t_{CE}$	$\overline{CE}$ Active to Output Valid		30		35		35		45		55		70	ns
$t_{HZCE}$	$\overline{CE}$ Inactive to High Z		12		15		15		15		20		25	ns
$t_{PU}$	$\overline{CE}$ Active to Power-Up	0		0		0		0		0		0		ns
$t_{PD}$	$\overline{CE}$ Inactive to Power-Down		30		35		40		40		50		60	ns
$t_{OH}$	Output Data Hold	0		0		0		0		0		0		ns

Switching Waveform



H256-7



**Erasure Characteristics**

Wavelengths of light less than 4000 Angstroms begin to erase the CY27H256 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm<sup>2</sup>. For an ultraviolet lamp with a 12 mW/cm<sup>2</sup> power rating, the exposure time would be approximately 35 minutes. The CY27H256 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the

EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm<sup>2</sup> is the recommended maximum dosage.

**Programming Modes**

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

**Table 1. Programming Electrical Characteristics**

Parameter	Description	Min.	Max.	Unit
V <sub>PP</sub>	Programming Power Supply	12.5	13	V
I <sub>PP</sub>	Programming Supply Current		50	mA
V <sub>IHP</sub>	Programming Input Voltage HIGH	3.0	V <sub>CC</sub>	V
V <sub>ILP</sub>	Programming Input Voltage LOW	-0.5	0.4	V
V <sub>CCP</sub>	Programming V <sub>CC</sub>	6.0	6.5	V

**Table 2. Mode Selection**

Mode	Pin Function <sup>[8]</sup>					
	$\overline{CE}$	$\overline{OE}$	V <sub>PP</sub>	A <sub>0</sub>	A <sub>9</sub>	Data
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	A <sub>0</sub>	A <sub>9</sub>	O <sub>7</sub> – O <sub>0</sub>
Output Disable	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	A <sub>0</sub>	A <sub>9</sub>	High Z
Stand-by	V <sub>IH</sub>	X	V <sub>IH</sub>	X	X	High Z
Program	V <sub>ILP</sub>	V <sub>IHP</sub>	V <sub>PP</sub>	A <sub>0</sub>	A <sub>9</sub>	D <sub>7</sub> – D <sub>0</sub>
Program Verify	V <sub>IHP</sub>	V <sub>ILP</sub>	V <sub>PP</sub>	A <sub>0</sub>	A <sub>9</sub>	O <sub>7</sub> – O <sub>0</sub>
Program Inhibit	V <sub>IHP</sub>	V <sub>IHP</sub>	V <sub>PP</sub>	A <sub>0</sub>	A <sub>9</sub>	High Z
Signature Read (MFG)	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>HV</sub> <sup>[9]</sup>	34H
Signature Read (DEV)	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>HV</sub> <sup>[9]</sup>	21H

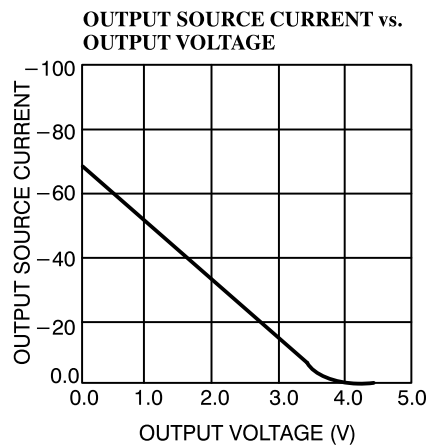
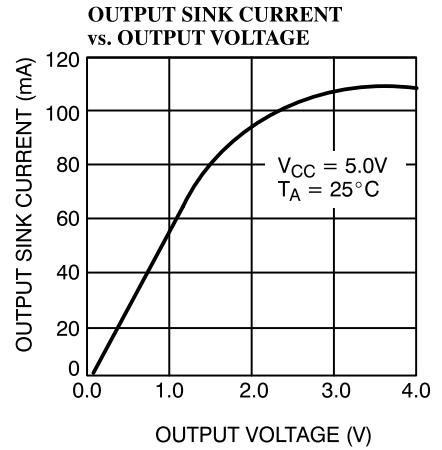
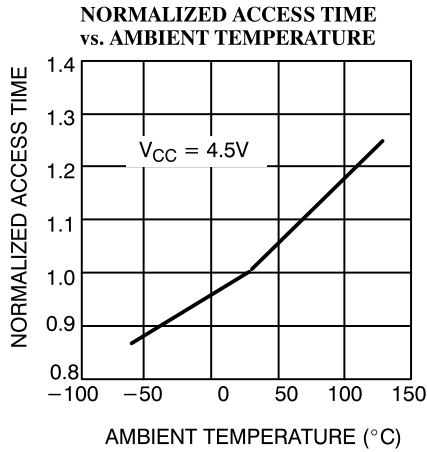
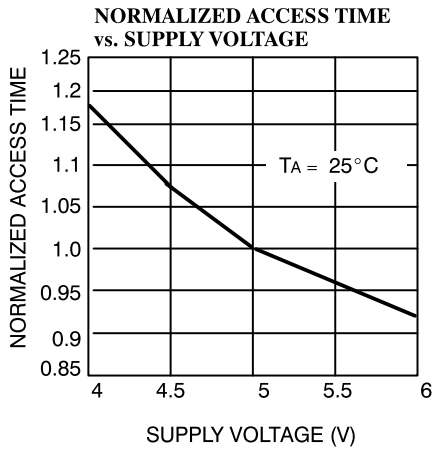
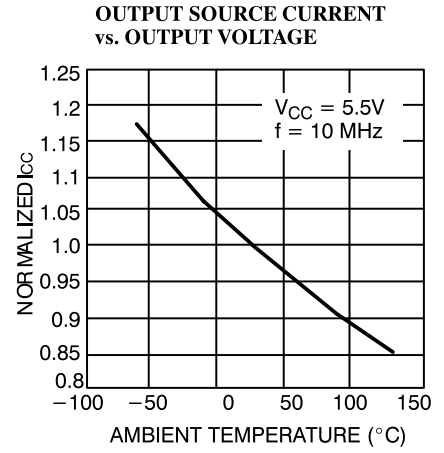
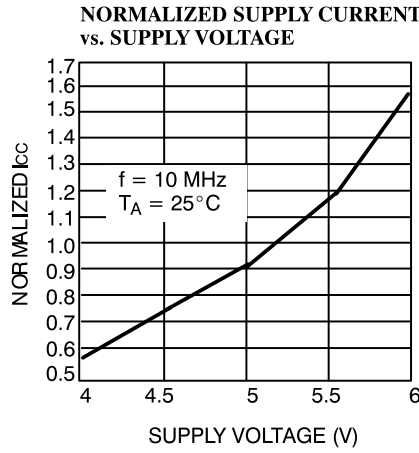
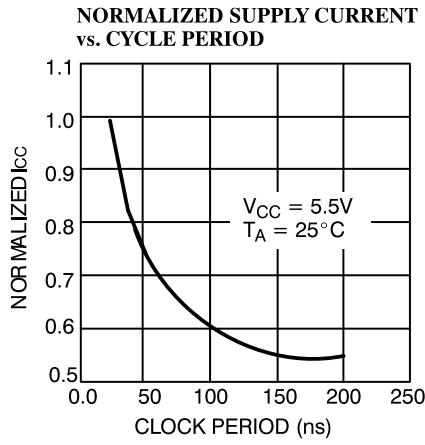
**Notes:**

8. X can be V<sub>IL</sub> or V<sub>IH</sub>.

9. V<sub>HV</sub>=12±0.5V



Typical DC and AC Characteristics





Ordering Information<sup>[10]</sup>

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY27H256-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H256-25ZC	Z28	28-Lead Thin Small Outline Package	
30	CY27H256-30JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H256-30PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H256-30WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H256-30ZC	Z28	28-Lead Thin Small Outline Package	
35	CY27H256-35JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H256-35PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H256-35WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H256-35ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H256-35LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military
	CY27H256-35QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
45	CY27H256-45JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H256-45PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H256-45WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H256-45ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H256-45DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27H256-45LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H256-45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H256-45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
55	CY27H256-55JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H256-55PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H256-55WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H256-55ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H256-55DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27H256-55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H256-55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H256-55WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
70	CY27H256-70JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H256-70PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H256-70WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H256-70ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H256-70DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27H256-70LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H256-70QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H256-70WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

Note:

10. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.



**MILITARY SPECIFICATIONS**  
**Group A Subgroup Testing**

**DC Characteristics**

Parameter	Subgroups
V <sub>OH</sub>	1, 2, 3
V <sub>OL</sub>	1, 2, 3
V <sub>IH</sub>	1, 2, 3
V <sub>IL</sub>	1, 2, 3
I <sub>IX</sub>	1, 2, 3
I <sub>OZ</sub>	1, 2, 3
I <sub>CC</sub>	1, 2, 3
I <sub>SB</sub>	1, 2, 3

**Switching Characteristics**

Parameter	Subgroups
t <sub>AA</sub>	7, 8, 9, 10, 11
t <sub>OE</sub>	7, 8, 9, 10, 11
t <sub>CE</sub>	7, 8, 9, 10, 11

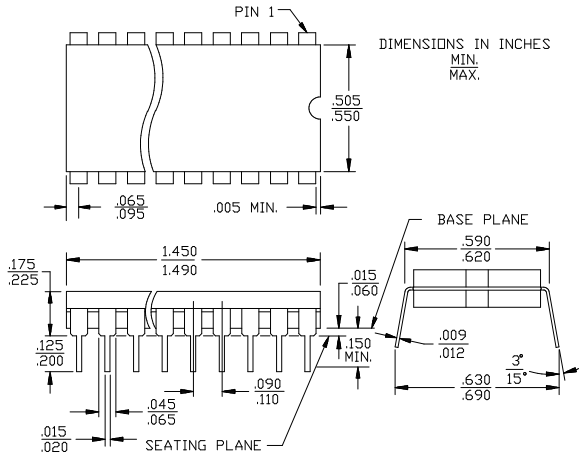
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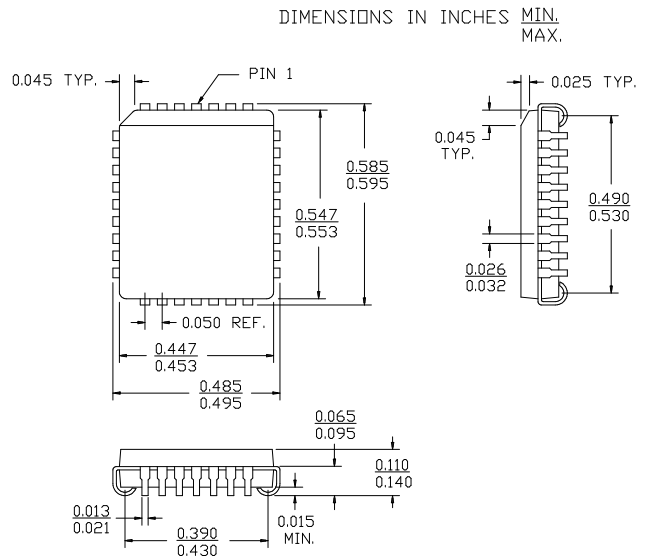


Package Diagrams

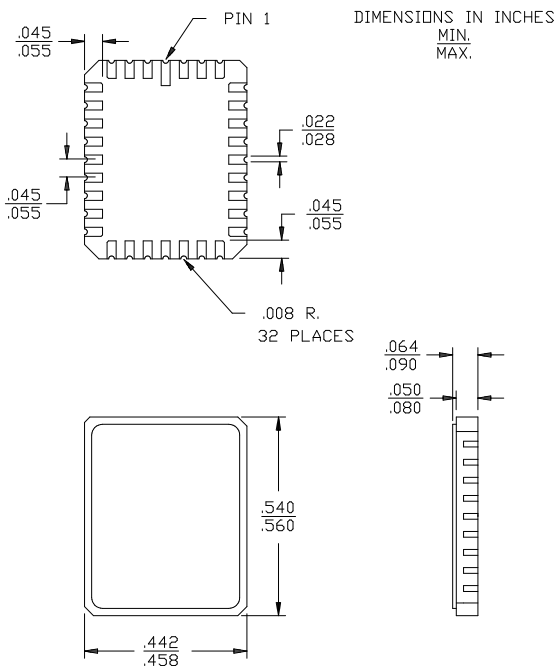
**28-Lead (600-Mil) CerDIP D16**  
 MIL-STD-1835 D-10 Config. A



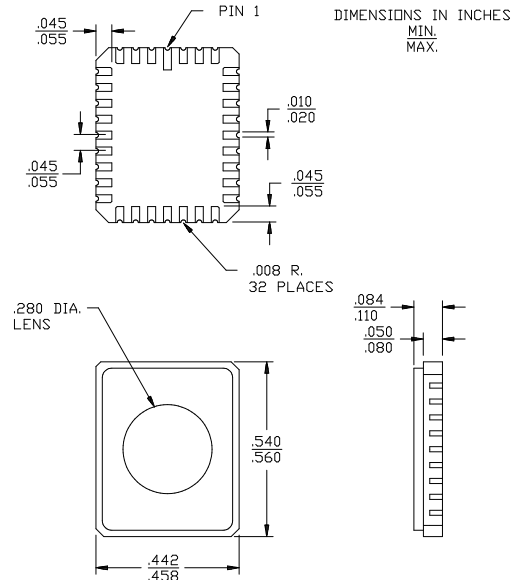
**32-Lead Plastic Leaded Chip Carrier J65**



**32-Pin Rectangular Leadless Chip Carrier L55**  
 MIL-STD-1835 C-12



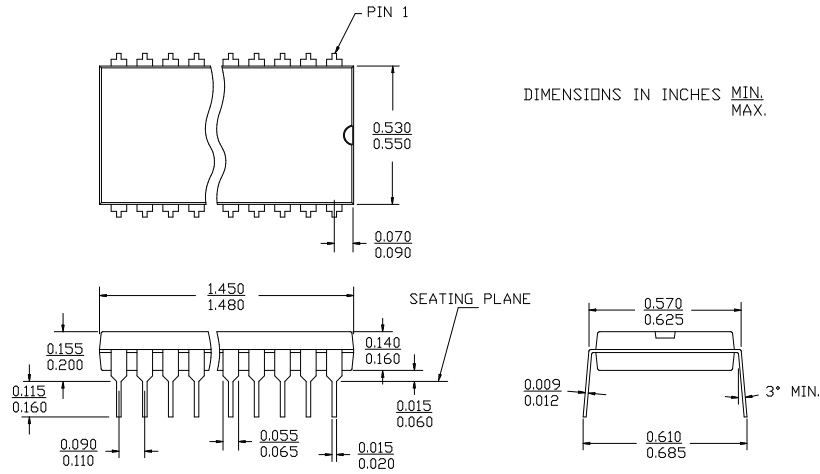
**32-Pin Windowed Rectangular Leadless Chip Carrier Q55**  
 MIL-STD-1835 C-12



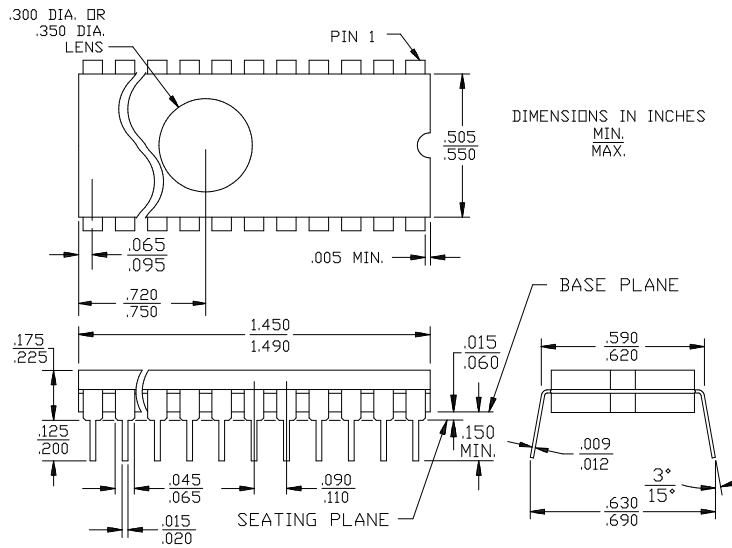


Package Diagrams (continued)

28-Lead (600-Mil) Molded DIP P15



28-Lead (600-Mil) Windowed CerDIP W16  
 MIL-STD-1835 D-10 Config. A





Package Diagrams (continued)

28-Lead Thin Small Outline Package Z28

