

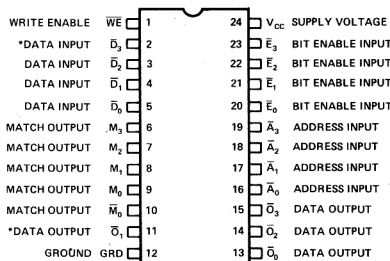
# HIGH SPEED 16 BIT CONTENT ADDRESSABLE MEMORY

- Organization – 4 Words x 4 Bits
- Max. Delay of 30 nsec Over 0°C to 75°C Temperature
- Open Collector Outputs – OR Tie Capability
- High Current Sinking Capability – 15 mA max.
- Low Input Load Current – 0.25 mA max.
- DTL & TTL Compatible
- Bit Enable Input – Bit Masking
- Standard 24 Pin Dual In-Line

The Intel 3104 is a high speed 16 bit Content Addressable Memory (CAM). It is a linear select 4 word by 4 bit array which is designed to compare data on its inputs with data already stored in its memory and

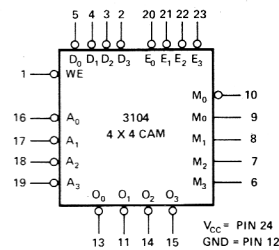
to indicate a match when these data are identical. This equality search is performed on all bits in parallel. The 3104 can also be used as a read/write RAM with linear selection addressing.

### PIN CONFIGURATION

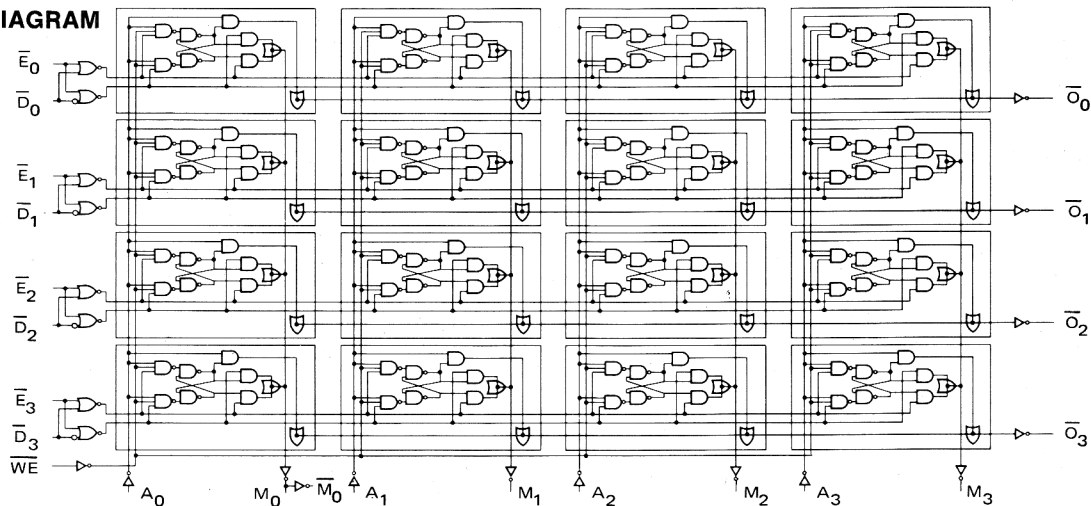


\*DATA IN and DATA OUT are of the same logic level. For a chip that is not selected, the data output is at a high level.

### LOGIC SYMBOL



### LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Temperature Under Bias	-65°C to +125°C
Storage Temperature	-65°C to +160°C
All Output or Supply Voltages	-0.5 to +7 Volts
All Input Voltages	-1.0 to +5.5 Volts
Output Currents	100 mA

**\*COMMENT:**

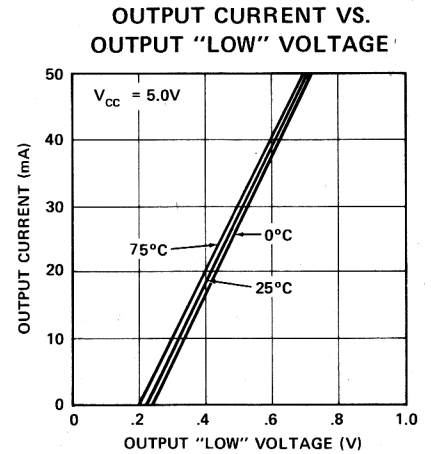
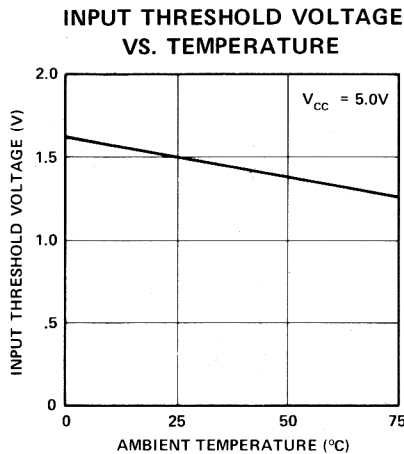
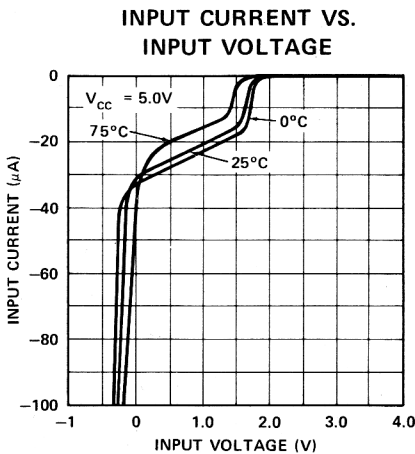
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. Characteristics**  $T_A = 0^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ ; unless otherwise specified.

SYMBOL	PARAMETER	LIMIT			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
$I_{FA}$	ADDRESS INPUT LOAD CURRENT			-0.25	mA	$V_{CC} = 5.25\text{V}$ $V_A = .45\text{V}$
$I_{FE}$	BIT ENABLE INPUT LOAD CURRENT			-0.25	mA	$V_{CC} = 5.25\text{V}$ $V_E = .45\text{V}$
$I_{FW}$	WRITE ENABLE INPUT LOAD CURRENT			-0.25	mA	$V_{CC} = 5.25\text{V}$ $V_W = .45\text{V}$
$I_{FD}$	DATA INPUT LOAD CURRENT			-0.25	mA	$V_{CC} = 5.25\text{V}$ $V_D = .45\text{V}$
$I_{RA}$	ADDRESS INPUT LEAKAGE CURRENT			10	$\mu\text{A}$	$V_{CC} = 5.25\text{V}$ $V_A = 5.25\text{V}$
$I_{RE}$	BIT ENABLE INPUT LEAKAGE CURRENT			10	$\mu\text{A}$	$V_{CC} = 5.25\text{V}$ $V_E = 5.25\text{V}$
$I_{RW}$	WRITE ENABLE INPUT LEAKAGE CURRENT			10	$\mu\text{A}$	$V_{CC} = 5.25\text{V}$ $V_W = 5.25\text{V}$
$I_{RD}$	DATA INPUT LEAKAGE CURRENT			10	$\mu\text{A}$	$V_{CC} = 5.25\text{V}$ $V_D = 5.25\text{V}$
$I_{CEX}$	OUTPUT LEAKAGE CURRENT (ALL OUTPUTS)			50	$\mu\text{A}$	$V_{CC} = 5.25\text{V}$ $V_{CEX} = 5.25\text{V}$
$V_{OL}$	OUTPUT "LOW" VOLTAGE (ALL OUTPUTS)			0.45	V	$V_{CC} = 4.75\text{V}$ $I_{OL} = 15\text{mA}$ (Three other Outputs Sink 15mA each)
$V_{IL}$	INPUT "LOW" VOLTAGE (ALL INPUTS)			0.85	V	$V_{CC} = 5\text{V}$
$V_{IH}$	INPUT "HIGH" VOLTAGE (ALL INPUTS)	2.0			V	$V_{CC} = 5\text{V}$
$I_{CC}$	POWER SUPPLY CURRENT			125	mA	$V_{CC} = 5.25\text{V}$
$C_{IN}^{**}$	INPUT CAPACITANCE		5		pF	$V_{IN} = +2.0\text{V}$ , $V_{CC} = 0.0\text{V}$ $f = 1\text{ MHz}$
$C_{OUT}^{**}$	OUTPUT CAPACITANCE		8		pF	$V_{OUT} = +2.0\text{V}$ , $V_{CC} = 0.0\text{V}$ $f = 1\text{ MHz}$

\*\*This parameter is periodically sampled and is not 100% tested.

**Typical D.C. Characteristics**

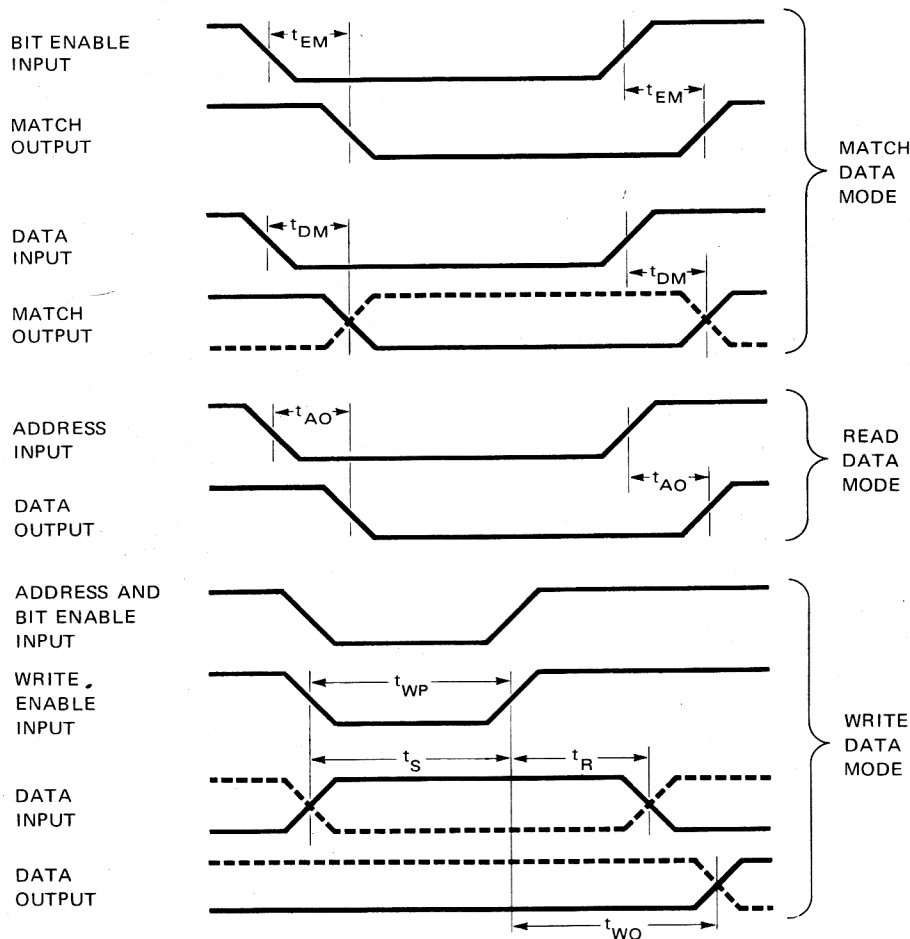
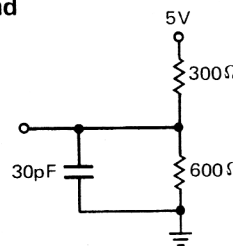


### Switching Characteristics

**Conditions of Test:**

- Input Pulse amplitudes - - 2.5V
- Input pulse rise and fall times of 5 nanoseconds between 1 volt and 2 volts
- Speed measurements are made at 1.5 volt levels
- Output loading is 15 mA and 30 pF

**15mA Test Load**



**A.C. Characteristics**  $T_A = 0^\circ\text{C to } +75^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ ; unless otherwise specified.

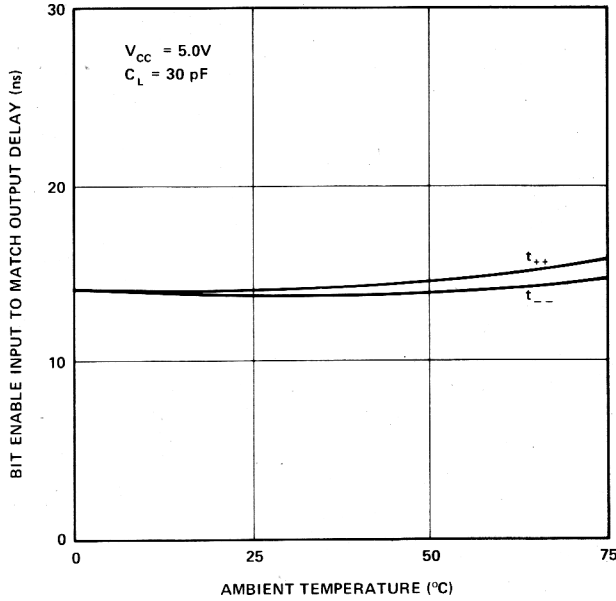
SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP. <sup>(1)</sup>	MAX.	
$t_{EM}$	BIT ENABLE INPUT TO MATCH OUTPUT DELAY		15	30	ns
$t_{DM}$	DATA INPUT TO MATCH OUTPUT DELAY		16	30	ns
$t_{AO}$	ADDRESS INPUT TO OUTPUT DELAY		14	30	ns
$t_{WP}$	WRITE ENABLE PULSE WIDTH	40	25		ns
$t_{WO}$	WRITE ENABLE TO OUTPUT DELAY		-	40	ns
$t_S$	SET-UP TIME ON DATA INPUT		-	40	ns
$t_R$	RELEASE TIME ON DATA INPUT	0	-		ns

Note 1. Typical values are at nominal voltages and  $T_A = 25^\circ\text{C}$ .

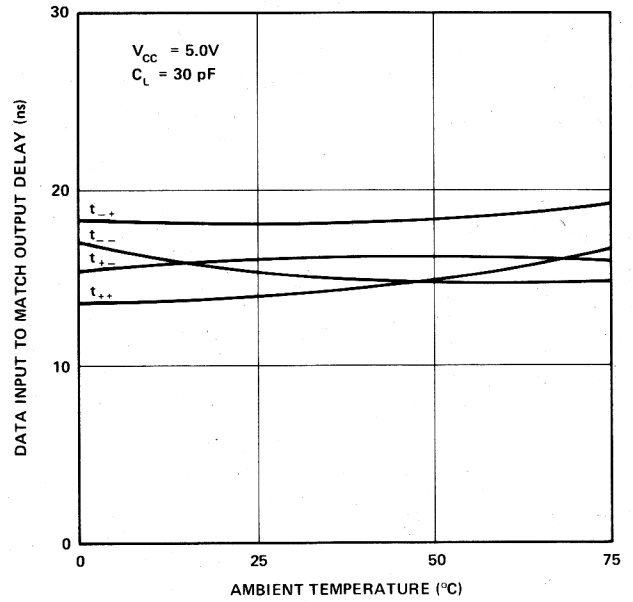
RAMs

Typical A.C. Characteristics

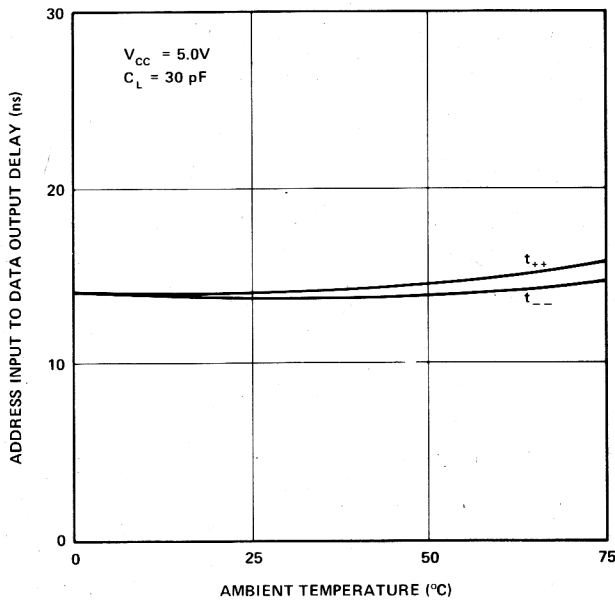
BIT ENABLE INPUT TO MATCH OUTPUT DELAY VS. TEMPERATURE



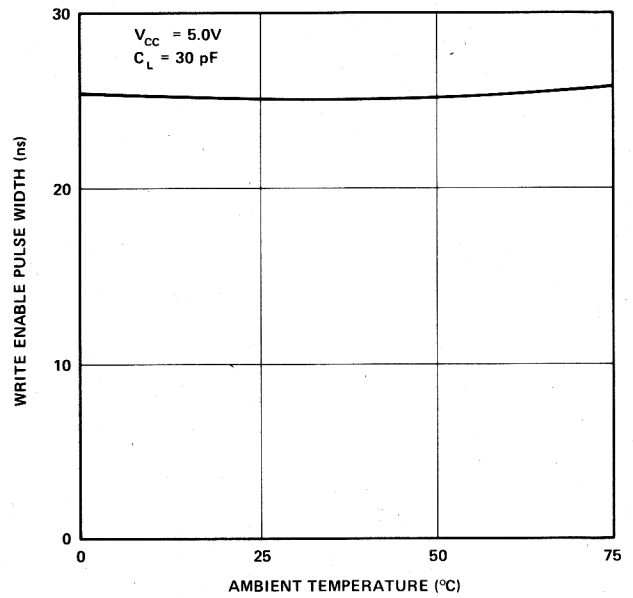
DATA INPUT TO MATCH OUTPUT DELAY VS. TEMPERATURE



ADDRESS INPUT TO DATA OUTPUT DELAY VS. TEMPERATURE



WRITE ENABLE PULSE WIDTH VS. TEMPERATURE



RAMs