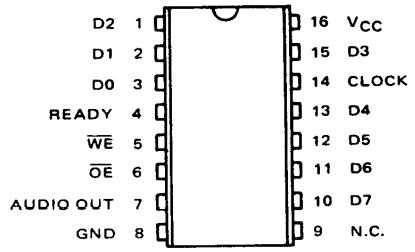
The Engineering Staff of
TEXAS INSTRUMENTS
Semiconductor Group

SN 76489 AN

DUAL-IN-LINE PACKAGE
(TOP VIEW)



FEATURES

- 3 Programmable Tone Generators
- Programmable White Noise Generator
- Programmable Attenuation
- Simultaneous Sounds
- TTL Compatible
- Up to 4MHz Clock Input*

DESCRIPTION

The SN76489AN digital complex sound generator is an I^2L/Bipolar IC designed to provide low cost tone/noise generation capability in microprocessor systems. The SN76489AN is a data bus based I/O peripheral.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	*MIN*	*TYP*	*MAX*	*UNITS*
Supply Voltage, V_{CC}	4.5	5.0	5.5	V
High Level Output Voltage, V_{OH} (pin 4)			5.5	V
Low Level Output Current, I_{OL} (pin 4)			2	mA
Operating Free-Air Temperature, T_A	0		70	°C

*Part SN76494N is identical to the SN76489A except that the maximum clock input frequency is 500kHz. A "divide-by-eight" stage is deleted from the input circuitry and only 4 clock pulses are required to load the data, compared to 32 pulses for the SN76489AN.

OPERATION

1. TONE GENERATORS

Each tone generator consists of a frequency synthesis section and an attenuation section. The frequency synthesis section requires 10 bits of information (FO-F9) to define half the period of the desired frequency (n). FO is the most significant bit and F9 is the least significant bit. This information is loaded into a 10 stage tone counter, which is decremented at a N/16 rate where N is the input clock frequency. When the tone counter decrements to zero, a borrow signal is produced. This borrow signal toggles the frequency flip-flop and also reloads the tone counter. Thus, the period of the desired frequency is twice the value of the period register.

The frequency can be calculated by the following:

$$f = \frac{N}{32n}$$

where N = ref clock in Hz
n = 10 bit binary number

The output of the frequency flip-flop feeds into a four stage attenuator. The attenuator values, along with their bit position in the data word, are shown in Table 1. Multiple attenuation control bits may be true simultaneously. Thus, the maximum attenuation is 28 db.

Table 1: ATTENUATION CONTROL

BIT POSITION				
A0	*A1*	*A2*	*A3*	*WEIGHT*
0	0	0	1	2 db
0	0	1	0	4 db
0	1	0	0	8 db
1	0	0	0	16 db
1	1	1	1	OFF

2. NOISE GENERATOR

The Noise Generator consists of a noise source and an attenuator. The noise source is a shift register with an exclusive OR feedback network. The feeback network has provisions to protect the shift register from being locked in the zero state.

Table 2: NOISE FEEDBACK CONTROL

FB	*CONFIGURATION*
0	"Periodic" Noise
1	"White" Noise

Whenever the noise control register is changed, the shift register is cleared. The shift register will shift at one of four rates as determined by the two NF bits. The fixed shift rates are derived from the input clock.

Table 3: NOISE GENERATOR FREQUENCY CONTROL

BITS		
NFO	*NFI*	*SHIFT RATE*
0	0	N/512
0	0	N/1024
1	0	N/2048
1	1	Tone Generator #3 Output

The output of the noise source is connected to a programmable attenuator as shown in Figure 4.

3. OUTPUT BUFFER/AMPLIFIER

The output buffer is a conventional operational amplifier summing circuit. It sums the three tone generator outputs, and the noise generator output. The output buffer will generate up to 10mA.

4. CPU to SN76489AN INTERFACE

The microprocessor interfaces with the SN76489AN by means of the 8 data lines and 3 control lines ($\overline{WE}$, $\overline{CE}$ and READY). Each tone generator requires 10 bits of information to select the frequency and 4 bits of information to select the attenuation. A frequency update requires a double byte transfer, while an attenuator update requires a single byte transfer.

If no other control registers on the chip are accessed, a tone generator may be rapidly updated by initially sending both bytes of frequency and register data, followed by just the second byte of data for succeeding values. The register address is latched on the chip, so the data will continue going into the same register. This allows the 6 most significant bits to be quickly modified for frequency sweeps.

5. CONTROL REGISTERS

The SN76489AN has 8 internal registers which are used to control the 3 tone generators and the noise source. During all data transfers to the SN76489AN, the first byte contains a three bit field which determines the destination control register. The register address codes are shown in Table 4.

Table 4: REGISTER ADDRESS FIELD

R0	R1	R2	DESTINATION CONTROL REGISTER
0	0	0	Tone 1 Frequency
0	0	0	Tone 1 Attenuation
0	1	0	Tone 2 Frequency
0	1	1	Tone 2 Attenuation
1	0	0	Tone 3 Frequency
1	0	1	Tone 3 Attenuation
1	1	0	Noise Control
1	1	1	Noise Attenuation

6. DATA FORMATS

The formats required to transfer data are shown below.

	REG ADDR			DATA			
1	R0	R1	R2	F6	F7	F8	F9

BIT 0 FIRST BYTE BIT 7
UPDATE NOISE SOURCE (SINGLE BYTE TRANSFER)

	DATA						
0	x	F0	F1	F2	F3	F4	F5

BIT 0 SECOND BYTE BIT 7

	REG ADDR					SHIFT	
1	R0	R1	R2	x	FB	NF0	NF1

BIT 0 BIT 7
UPDATE ATTENUATOR (SINGLE BYTE TRANSFER)

	REG ADDR			DATA			
1	R0	R1	R2	A0	A1	A2	A3

BIT 0 BIT 7

7. The microprocessor selects the SN76489AN by placing $\overline{CE}$ into the true state (low voltage). Unless $\overline{CE}$ is true, no data can occur. When $\overline{CE}$ is true, the $\overline{WE}$ signal strobes the contents of the data bus to the appropriate control register. The data bus contents must be valid at this time.

   The SN76489AN requires approximately 32 clock cycles to load the data into the control register. The open collector READY output is used to synchronize the microprocessor to this transfer and is pulled to the false state (low voltage) immediately following the leading edge of $\overline{CE}$. It is released to go to the true state (external pullup) when the data transfer is completed.

   The data transfer timing is shown below.

Figure 1. DATA TRANSFER TIMING

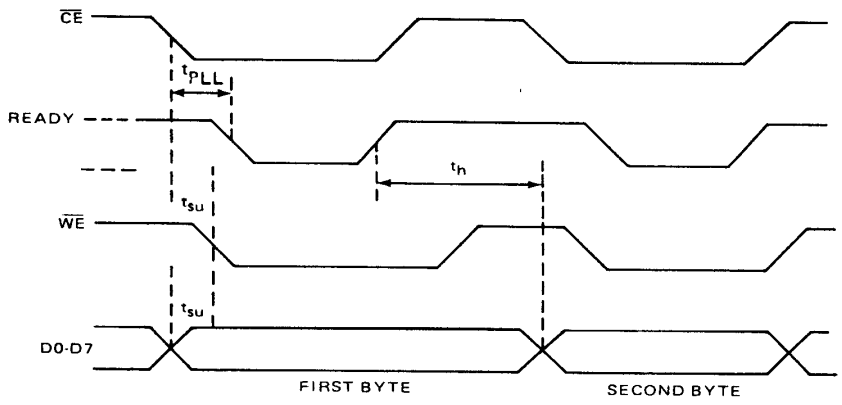


Table 5: FUNCTION TABLE*

Inputs		Output
$\overline{CE}$	$\overline{WE}$	READY
L	L	L
L	H	L
H	L	H
H	H	H

*This table is valid when the device is:

(1) not being clocked, and
(2) is initialized by pulling $\overline{WE}$ and $\overline{CE}$ high.

8. PIN ASSIGNMENT

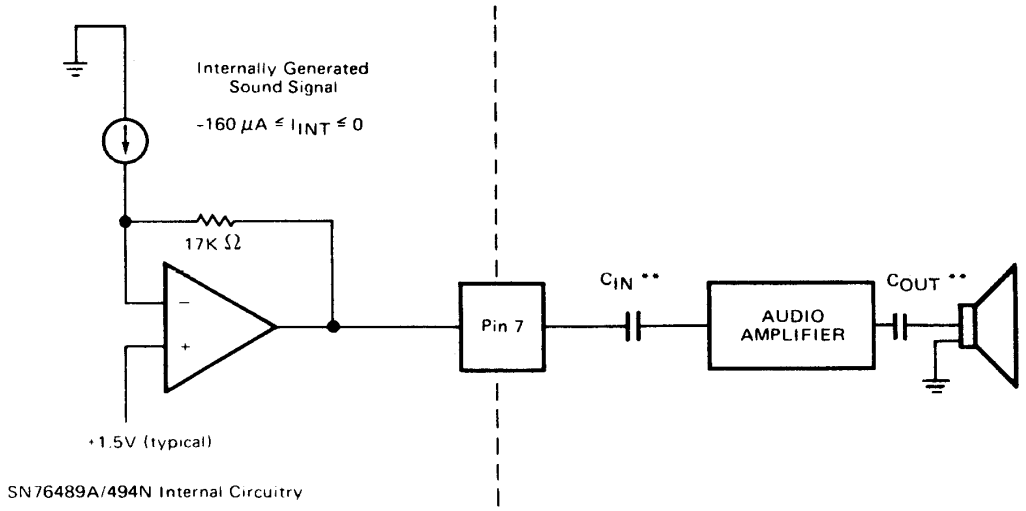
The table below defines the SN76489AN pin assignment and describes the function of each pin.

SIGNATURE	*PIN*	*I/O*	*DESCRIPTION*
$\overline{CE}$	6	IN	Chip Enable – when active (low) date may be transferred from CPU to the SN76489AN.
DO(MSB)	3	IN	D0 through D7 – Input data bus through which the control data is input.
D1	2	IN	
D2	1	IN	
D3	15	IN	
D4	13	IN	
D5	12	IN	
D6	11	IN	
D7	10	IN	
VCC	16	IN	Supply Voltage (5V nom)
GND	8	OUT	Ground Reference
CLOCK	14	IN	Input Clock
$\overline{WE}$	5	IN	Write Enable – when active (low), $\overline{WE}$ indicates that data is available from the CPU to the SN76489AN.
READY	4	OUT	When active (high), READY indicates that the data has been read. When READY is low, the microprocessor should enter a wait state until READY is high.
N.C.	9		No external connection should be made in this pin.
AOUT	7	OUT	Audio Drive Out

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_I	Input Current	V_{IN} = GND to V_{CC}	$\overline{CE}$		-25	-175	μA
		D0-D7, $\overline{WE}$, CLK			-10	-10	μA
V_{OL}	Low Level Output Voltage	I_{OUT} = 2mA	READY		.25	.4	Volts
I_{CC}	Supply Current	Outputs Open			30	50	mA
C_I	Input Capacitance					15	pF
I_{OH}	High Level Output Current	READY	Vcc < 5.0V			20	μA
			5.0V < Vcc < 5.5V			300	
V_{IH}	High Level Input Voltage	D0-D7, $\overline{WE}$, $\overline{CE}$, CLK		2			Volts
V_{IL}	Low Level Input Voltage	D0, D7, $\overline{WE}$, $\overline{CE}$, CLK				.8	Volts
2dB	Attenuation			1	2	3	dB
4dB	Attenuation			3	4	5	dB
8dB	Attenuation			7	8	9	dB
16dB	Attenuation			15	16	17	dB

Figure 2. EXTERNAL AUDIO INPUT INTERFACE



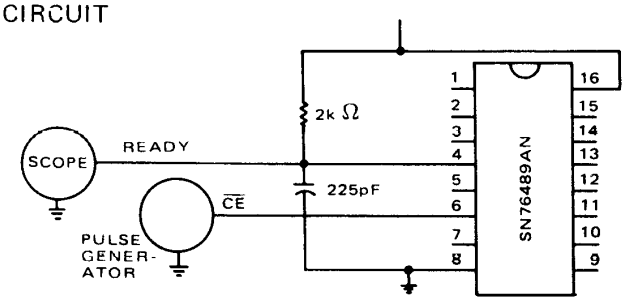
* * These capacitance values are determined by the frequency response desired and the audio amplifier used.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

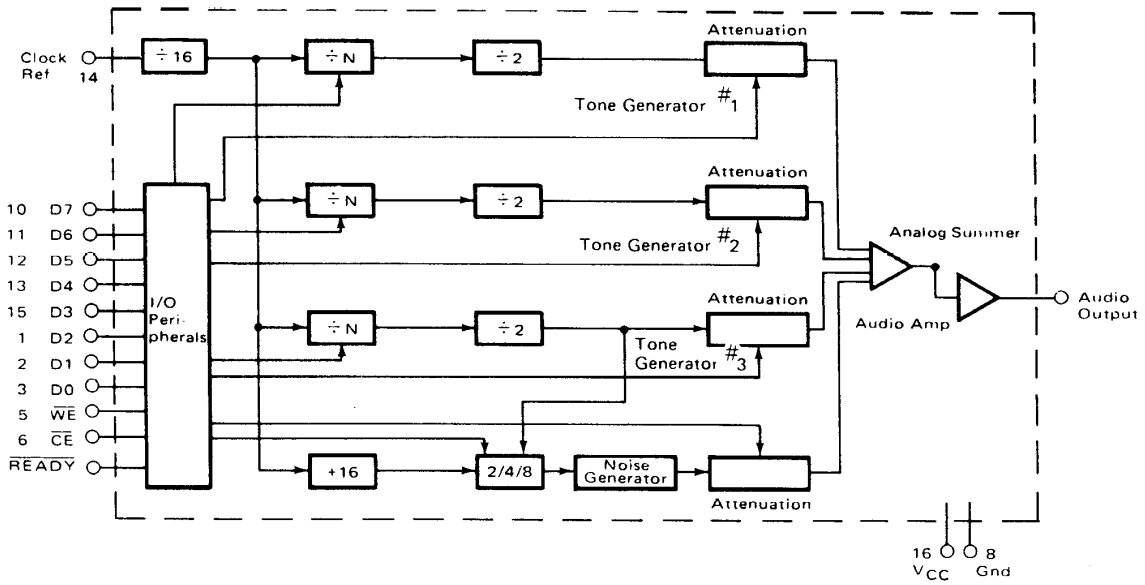
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
*$\overline{CE}$ to READY	C_L = 225pF				
t_{PLL}, 50% to 50%	R_L = 2K to VCC		90	150	ns
f_{clock}, Input Clock Frequency	Clock Transition Time (10% to 90%) 10μS	DC	3.579	4	MHz
Setup Time, t_{su}	DATA W.R.T. $\overline{WE}$	0			ns
(see Figure 1)	$\overline{CE}$ W.R.T. $\overline{WE}$	0			ns
Hold Time, t_h (see Figure 1)	DATA W.R.T. READY	0			ns

*$\overline{CE}$ Pulse: 0-3V, $t_{rise} \leq$ 7nS, $t_{fall} \leq$ 7nS

Figure 3. t_{PLL} TEST CIRCUIT



BLOCK DIAGRAM



BLOCK DIAGRAM DESCRIPTION

This device consists of three programmable tone generators, a programmable noise generator, a clock scaler, individual generator attenuators and an audio summer output buffer. The SN76489AN has a parallel 8 bit interface through which the microprocessor transfers the data which controls the audio output.

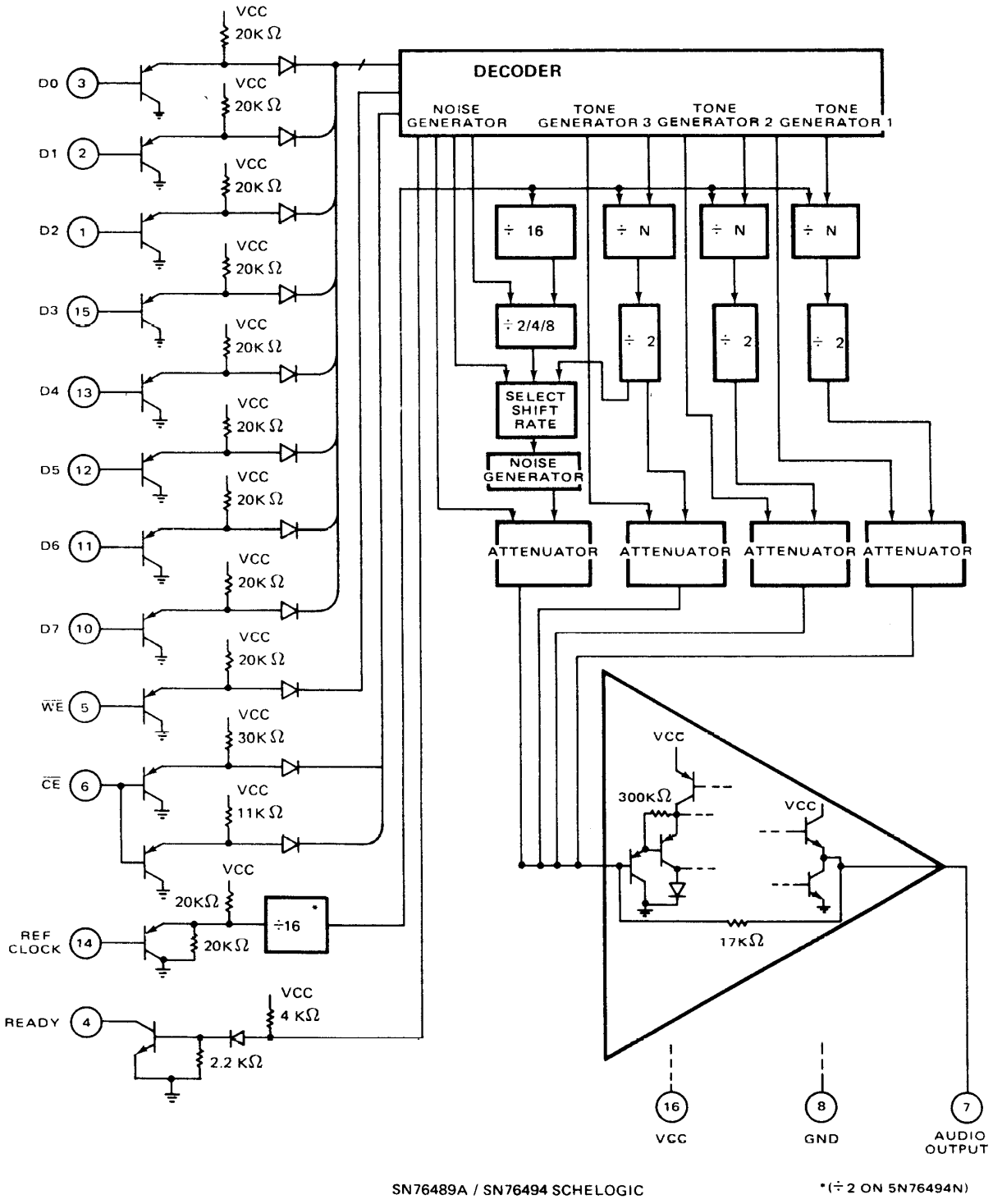

DECODER
NOISE GENERATOR
TONE GENERATOR 3
TONE GENERATOR 2
TONE GENERATOR 1
÷ 16
÷ N
÷ 2/4/8
÷ 2
SELECT SHIFT RATE
NOISE GENERATOR
ATTENUATOR
VCC
20K Ω
30K Ω
11K Ω
4 KΩ
2.2 KΩ
300KΩ
17KΩ
D0
D1
D2
D3
D4
D5
D6
D7
WE
CE
REF CLOCK
READY
AUDIO OUTPUT
GND
SN76489A / SN76494 SCHELOGIC
*(÷ 2 ON 5N76494N)

Figure 4.