MSM5232RS

8 CHANNEL TONE GENERATOR

FOR MUSICAL INSTRUMENTS

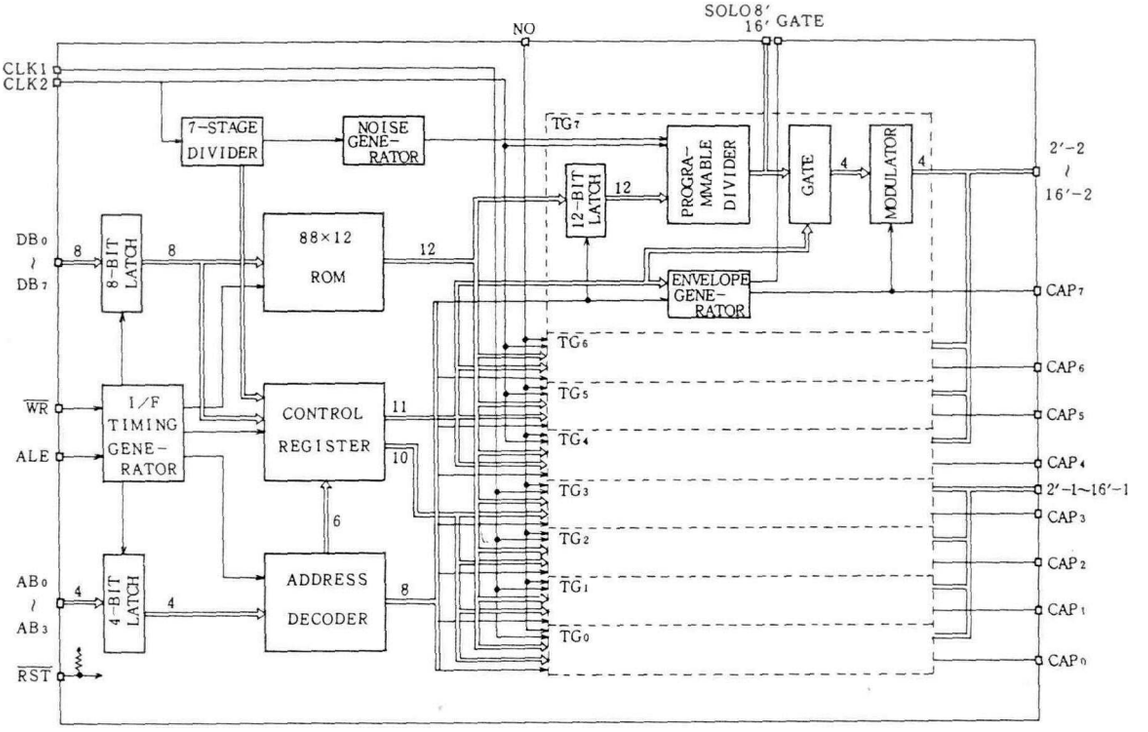
The MSM5232RS is an integrated circuit used as a sound source for musical instruments and contains a frequency divider circuit and envelope generator for 8 scale generation, and an 8 bit bus interface circuit integrated in one chip. The device is capable of outputting 8 tones simultaneously within a 7 octaves range while under microprocessor control.

FEATURES

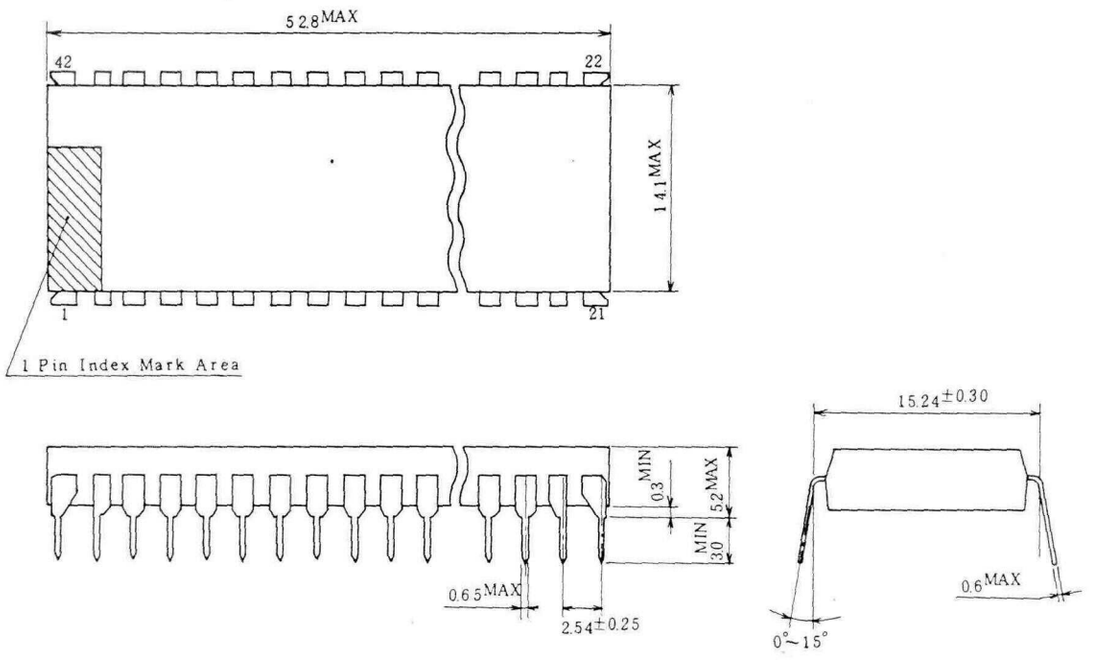
- o 4 + 4 polyphonic tone output composed into 2 groups.
  Each group is independently provided with clock input, output bus, and control register so that many beautiful and deep sounds can be generated.
- o Generation of 7 octave scales in addition to noise output,
- o 4 kinds of feet output; 2', 4', 8', and 16'.
- o The envelope generator is incorporated.
  There are two kinds of envelope waveforms; lasting sound and damping sound.
  In addition, the attack and decay time constant can be changed.
- o Interface to cope with an 8 bit microprocessor.
- o ROM is incorporated to convert key number data to divided frequency to generate scales.
- o Low power dissipation due to the CMOS IC.

(This specification is subject to change without prior notice.)

BLOCK DIAGRAM

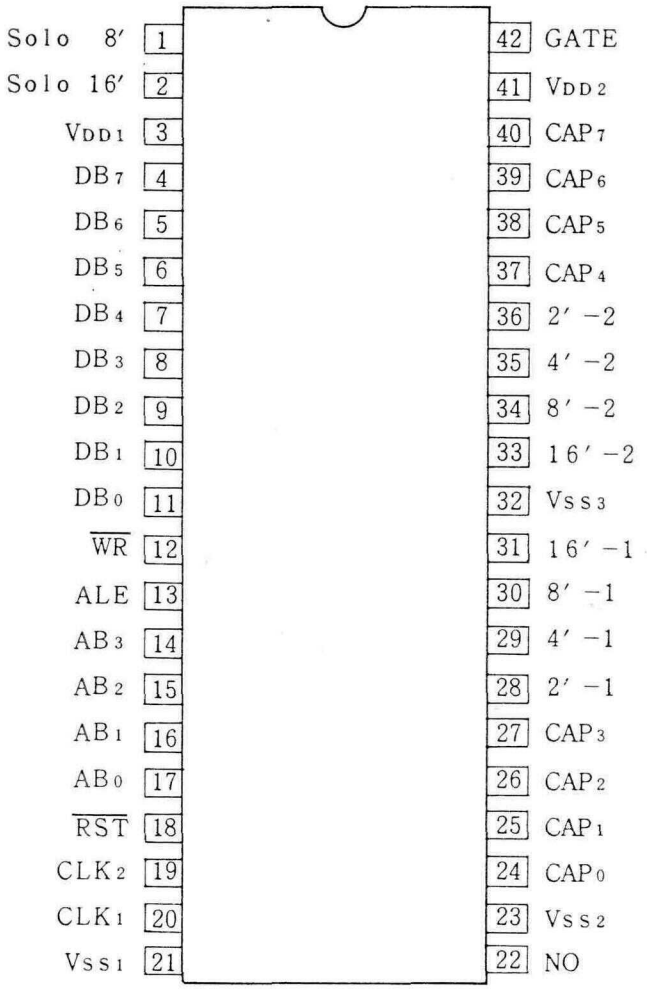


EXTERNAL DIMENSIONS



TERMINAL CONNECTION

(Top View) 42 Lead Plastic DIP



ELECTRICAL CHARACTERISTICS

o Maximum Absolute Rating

(Ta = −10 ~ +70℃)

Item	Symbol	Condition	Rated value	Unit
Power voltage	V_{SS1}		−6.5 ~ +0.3	V
	V_{SS2} V_{SS3}		−16 ~ +0.3	V
Input voltage	V_{I1}	CLK1, 2, $\overline{WR}$, ALE, $\overline{RST}$ $DB_{0\sim7}$, $AB_{0\sim3}$	V_{SS1} −0.3 ~ V_{DD1} +0.3	V
	V_{I2}	$CAP_{0\sim7}$	V_{SS2} −0.3 ~ V_{DD2} +0.3	V
Output current	I_{O1}	NO, SOLO8′, SOLO16′, GATE 2′−1,2, 4′−1, 2, 8′−1,2, 16′−1, 2	−10 ~ +10	mA
	I_{O2}	$CAP_{0\sim7}$	−20 ~ +20	mA
Tolerable loss	P_D	Ta = 25℃	800	mW
Storage temperature	Tstg	———	−55 ~ +150	℃

o Operating Range

Item	Symbol	Condition	Range	Unit
Power voltage	V_{SS1}	———	−5.25 ~ −4.75	V
	V_{SS2} V_{SS3}	———	−16 ~ −4.75	V
Operating temperature	T_{OP}	———	−10 ~ 70	℃

DC CHARACTERISTICS

(Ta=-10~+70t:)

Item	Symbol	Condition	V_{SS1} [V]	V_{SS2} [V]	MIN	MAX	Unit
"L" input current	I_{IL1}	Input terminals other than $\overline{RST}$ $V_I=V_{SS1}$	−5.25	—	—	−1	μA
	I_{IL2}	$\overline{RST}$ $V_I=V_{SS1}$	−5.0	—	−25	−120	
"H" input current	I_{IH1}	Input terminals other than $\overline{RST}$ $V_I=V_{DD}$	−5.25	—	—	1	μA
	I_{IH2}	$\overline{RST}$ $V_I=V_{DD}$			—	1	
"L" input voltage	V_{IL1}	ABn, DBn, $\overline{WR}$, ALE	−4.75	—	—	V_{SS1}+0.8	V
	V_{IL2}	CLK_1, CLK_2			—	V_{SS1}+0.8	
	V_{IL3}	$\overline{RST}$				V_{SS1}+1.0	
"H" input voltage	V_{IH1}	ABn, DBn, $\overline{WR}$, ALE	−4.75	—	V_{SS1}+2.4	—	V
	V_{IH2}	CLK_1, CLK_2			−0.8	—	
	V_{IH3}	$\overline{RST}$			−1.0	—	
EG inversion voltage	V_T	———	—	−5	−1.5	−0.5	V
			—	−12	−3.6	−1.2	
"L" output voltage	V_{OL}	NO, GATE, SOLO8′ SOLO16′ I_O=0.1mA	—	−5	—	−4.5	V
			—	−12	—	−11.5	
"H" output voltage	V_{OH}	NO, GATE, SOLO8′ SOLO16′ I_O=−0.1mA	—	−5	−0.5	—	V
			—	−12	−0.5	—	
Current consumption	$\|I_{SS1}\|$	f_{CLK1}, f_{CLK2}=2.12MHz	−5.25	—	—	5	mA
	$\|I_{SS2}\|$	———	—	−5	—	1	
			—	−12	—	3	
Input capacity	C_I	f=1MHz	—	—	—	15	pF

(Ta = 25℃)

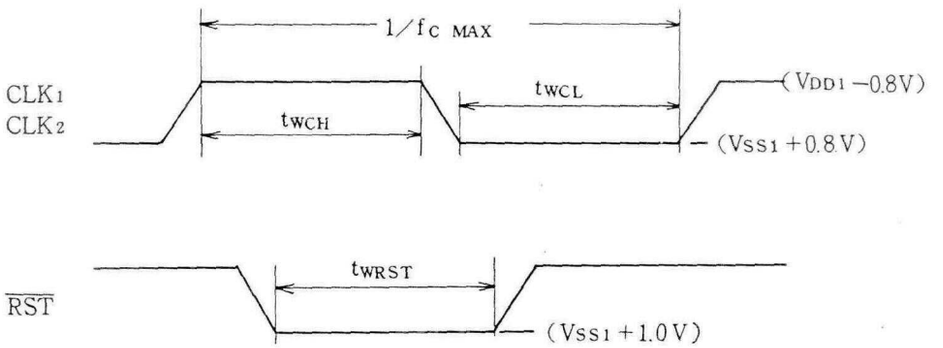
Item	Symbol	Condition	V_{SS1} (V)	V_{SS2} (V)	MIN	MAX	Unit
CAPn terminal output current	I_{CA}	$V_O = V_{SS2}$	—	−5	−1.4	−2.8	mA
			—	−12	−3.7	−7.4	
	I_{CRF}	$V_O = V_{DD2}$	—	−5	85	170	μA
			—	−12	200	400	
	I_{CRS}	$V_O = V_{DD2}$	—	−5	8.5	17	
			—	−12	20	40	
	I_{CZ}	$V_O = V_{SS2}$ or V_{DD2}	—	−15	−1	1	μA
TBn output current	I_{TF}	$V_O = V_{DD2}$, $V_{CAP} = V_{SS2}$	—	—	—	1	μA
	I_{TT}	$V_O = V_{DD2}$, $V_{CAP} = V_{SS2} + 2V$	—	—	1	—	
	I_{TN}	$V_O = V_{DD2}$, $V_{CAP} = V_{DD2}$ Single CH is only ON	—	−5	30	60	
			—	−12	190	380	μA

SWITCHING CHARACTERISTICS

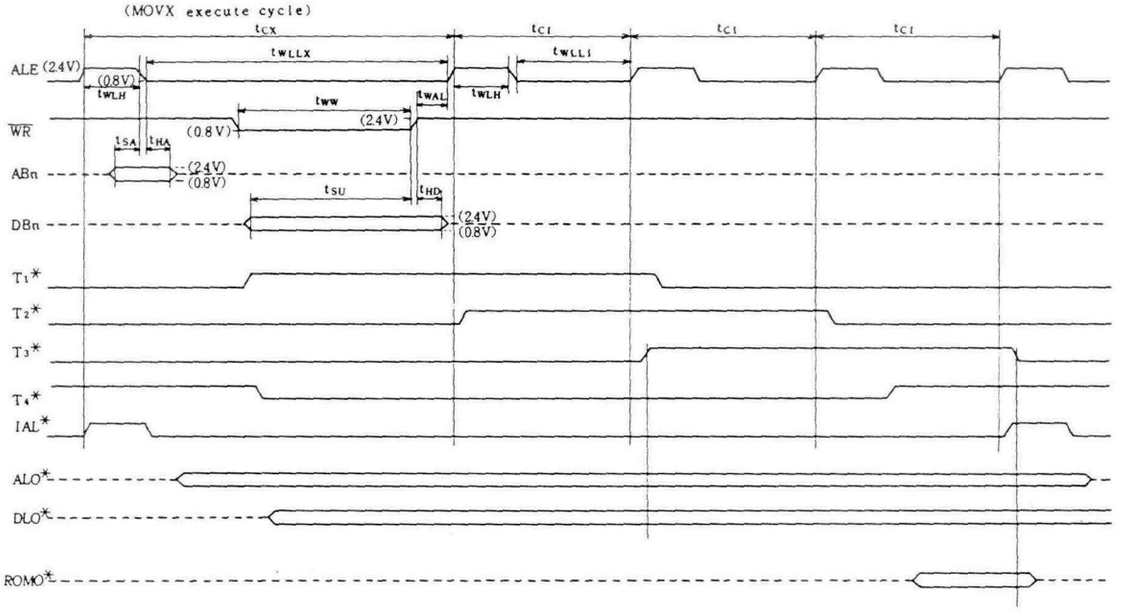
(V_{SS1} = −4.75 ~ −5.25 V, Ta = −10 ~ 70℃)

Item	Symbol	Condition	MIN	MAX	Unit
Maximum input frequency	$f_{C\,MAX}$		2.5	—	MHz
ALE cycle time	t_{CX}		1.0	—	μs
	t_{CI}		0.5	10	
Input pulse width	t_{WCH}		150	—	ns
	t_{WCL}		150	—	
	t_{WLH}		150	—	
	t_{WLLX}		500	—	
	t_{WLLI}		200	—	
	t_{WW}		400	—	
	t_{WRST}		10	—	μs
Set-up time	t_{SA}		100	—	ns
	t_{SD}		300	—	
Hold time	t_{HA}		100	—	ns
	t_{HD}		80	—	
Input timing	t_{WAL}		0	—	ns

Input waveforms



Interface timing



* These signals denote timing in IC.

Note: The voltage values at timing definition points are set according to Vss1 which is used as a reference.

TERMINAL EXPLANATION

- DB_0 ~ DB_7

  These are the data input terminals which are connected to the CPU data bus; various data are input through these terminals.

- AB_0 ~ AB_3

  These are the address input terminals. Using this input, an internal register is selected to write data in.

- ALE

  This input is put in the "H" section, where signals sent to AB_0 ~ AB_3 are inputted in the data latch and latched on at the trailing edge.

o /WR

This input is entered in the "L" section, where signals sent to DB_0 ~ DB_7 are inputted in the data latch and latched on at the trailing edge.

o CLK_1 and CLK_2

They are input into the standard clock and output scales can be obtained through the frequency-dividing of this input.
CLK_1 sets the standard frequency for tone generators TG_0 ~ TG_3 (group 1), and CLK_2 for tone generators TG_4 ~ TG_7 (group 2).

o /RST

This is the input terminals for internal parts initialization and are incorporated with the pull-up resistance. Figure 2 shows internal register conditions after initialization.

o CAP_0 ~ CAP_7

These are terminals that connect the capacitor to the envelope generator. The envelope is generated by charging and discharging its capacity through the enclosed resistance. In addition, when operation of the envelope generator is inhibited, a high impedance state results, and envelope waveforms can be inputted from the outside.

o 2' - 1 ~ 16' - 1 and 2' - 2 ~ 16' - 2

These are tone bus output terminals divided into group 1 and group 2, each of which consists of 4 registers; 2', 4', 8', and 16'. Four tone generators are connected to each tone bus, and they are mixed in a form of current addition. This is why it is important to receive this output from outside at a low impedance.

o SOLO 8' and SOLO 16'

These are solo sound source output terminals that constantly output square waveforms of 8' and 16' tones from tone generator TG_7.

o GATE

This terminal outputs the solo output ON/OFF signals.
In the solo mode case, GF of TG_7 is outputted, and in cases when the solo mode is inhibited, it is set to the "L" level.

o NO

This is the noise sound source output terminal that always outputs noise generated by the incorporated pseudo random pulse generation circuit.

o VDD_1 and VSS_1

These are power terminals for 5V lines.

o VDD_2, VSS_2, and Vss_3

These are power terminals for 5 ~ 15V lines,

Note: Connect VDD_1 and VDD_2 and VSS_2 and VSS_3 externally and respectively before use.

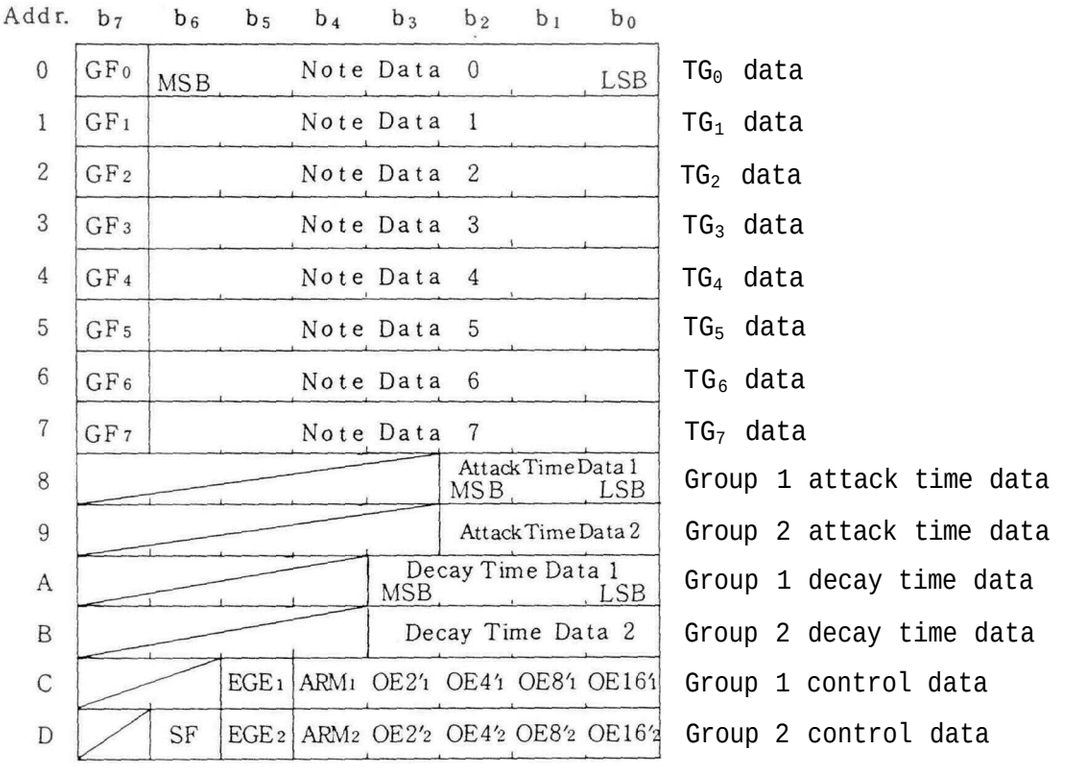


Fig. 1 Internal Register Map

Addr.	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	Condition
0	0	*	*	*	*	*	*	*	GF=0, pitch indefinite
1	0	*	*	*	*	*	*	*	
2	0	*	*	*	*	*	*	*	〃
3	0	*	*	*	*	*	*	*	〃
4	0	*	*	*	*	*	*	*	
5	0	*	*	*	*	*	*	*	〃
6	0	*	*	*	*	*	*	*	〃
7	0	*	*	*	*	*	*	*	〃
8						0	0	0	Attack time = 2 ms
9						0	0	0	〃
A					0	0	0	0	Decay time = 40 ms
B					0	0	0	0	〃
C			0	0	0	0	0	0	Damping sound assigned, EG inhibited and all registers OFF
D		0	0	0	0	0	0	0	Damping sound assigned, solo mode inhibited, and all registers OFF

Note: * mark shows that it *is* indefinite
(a previous condition *is* maintained)

Fig. 2 Internal Condition after Initial Reset

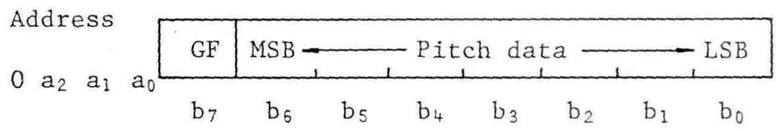
OPERATION EXPLANATION

o Interface

This integrated circuit is controlled by writing control data in the internal registers. DB_0 ~ DB_7, AB_0 ~ AB_3, WR and ALE signals are connected directly to the bus and CPU control signals (in case of a low speed CPU), or indirectly through some external parts (in case of a high speed CPU). The device is incorporated with the address latch to allow direct connection to the address data multiplexed bus in case of low speed CPUs. CPUs which can be connected directly: 8085A, 8048/49 (6 MHz).

(l) Type of input data

a) TG data

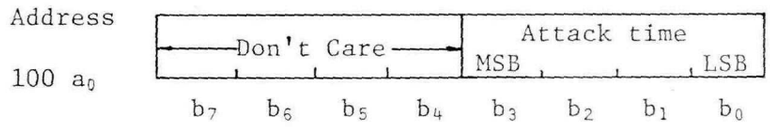


The data assign ON/OFF and tone generator pitch. It assigns one of the 8 TGs by the lower order 3 bits (a_2 ~ a_0) of the address.

- GF (gate flag)
  1: TG *ON*
  2: TG OFF

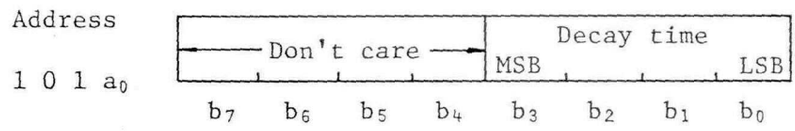
- Pitch data
  Data are written only when the pitch information *is* b_7 = 1 (TG ON). In the case when b_7 = 0, the contents of b_6 ~ b_0 are optional. (The contents do not change.)

b) Attack time data



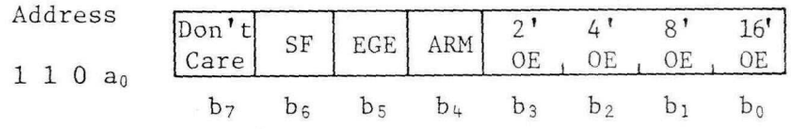
The attack time data assigns the envelope generator's attack time. One of 2 TG groups is selected by the lowermost order bit a_0, of the address. (a_0 = 0: Group 1 and a_0 = 1: Group 2).

c) Decay time data



The decay time data assigns the decay/release time of the envelope generator. One of the 2 TG groups is selected by the lowermost order bit a_0. (a_0 = 0: Group 1 and a_0 = 1: group 2).

d) Control data



The data sets the operational mode of individual TG groups. One of 2 TG groups is assigned a mode by the lowermost order bit a_0 of the address. (a_0 = 0: Group 1 and a_0 = 1: Group 2).

- SF (solo flag, significant only for group 2)
  - 1: Solo mode assignment
  - 0: Solo mode release

- EGE (envelope generator enable)
  - 1: Envelope generator operation
  - 0: Envelope generator inhibited

- ARM (attack release mode)
  - 1: Assignment of lasting sound
  - 0: Assignment of damping sound

• 2' OE, 4' OE, 8' OE, and 16' OE

1: Individual register output ON

0: Individual register output OFF

(2) Timing

Signals sent to the address and data bus are temporarily latched respectively by the trailing edge of ALE and /WR in the internal address and data latch, and pitch data are converted by the incorporated ROM into divided frequency data, and after that, the data is written in an assigned register by the address. Accordingly, it is essential that signals to the address and data bus are stabilized during the period before set-up time and after the trailing edge holding time of ALE and /WR respectively.

The timing of writing in each register is set by a strobe pulse generated from the timing generation circuit according to an ALE signal. Since this strobe pulse is generated at the timing shown in the timing chart, it is essential that more than four ALE pulses are added before the next writing operation.

o Tone Generator

This integrated circuit is incorporated with 8 tone generators (TG) and these tone generators are individually capable of generating scales and envelopes independently. An individual TG has 4 registers which output a pitch of 2', 4', 8', and 16' respectively.

Eight tone generators are divided into 2 groups; 1 group consists of 4 tone generators, and the TG output is connected by group, to the internal tone bus. Moreover, the control and envelope data are set by these groups. Furthermore, clock input. which serves

as *a* standard for pitch, is divided into groups.

(l) Frequency dividing circuit

This circuit divides standard clock (CLK_1, CLK_2) frequency to obtain an output frequency which is assigned by the pitch data, and consists of a programmable counter which generates tones in octaves, and a binary counter which generates the tones between octaves. Table 1 shows the relationship between pitch data and divided frequency.

(2) Envelope generator

This circuit generates signals for TG output amplitude modulation, and functions to form the waveforms shown in Figure 3 by the charging and discharging of the external capacitor through the incorporated resistance of control data and the time constant.

When 0 is written in EGE bit in the control data, incorporated resistance is open, then external envelope signals can be input from the CAPn terminal.

a) Operation mode

ARM = 1 (lasting sound assigned)

When GF in the TG data register is 1, it is set in the attack condition, and when GF is 0, it is set in the release condition.

ARM = 0 (damping sound assigned)

It is set in che attack condition at a point where GF is changed from 0 to 1, and it is set in the decay condition

when the electrical potential of the CAPn terminal exceeds the EG inversion voltage VT. When GF is turned to 0, it is set in the damping condition, irrespective of the preceeding condition.

b) Explanation of individual conditions

Attack condition

CAPn terminal is connected to VDD_2 through incorporated resistance

Decay/release condition

CAPn terminal is connected to VSS_2 through incorporated resistance (R_{RF} or R_{RS}).

Damping condition

CAPn terminal is connected to Vss_2 through incorporated resistance(R_{RF}).

c) Time constant control

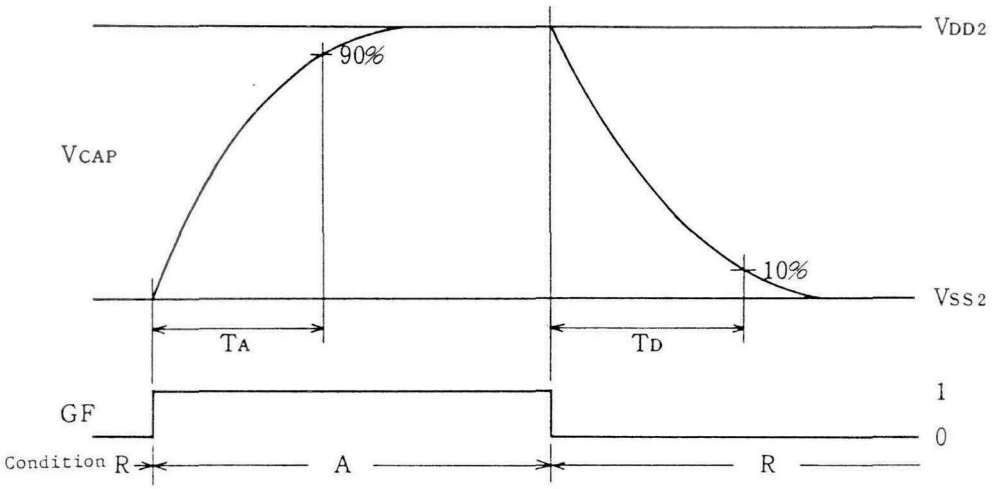
The speed of attack or decay/release is set by the contents of individual attack time or decay time registers. The time constant is controlled by changing charge or discharge current flow time by the opening or closing of resistance. In case of decay/release, however, two kinds of resistance are changed over because the change width is wide. The time constant is *always a* minimum value in the damping condition.

(3) Modulation circuit

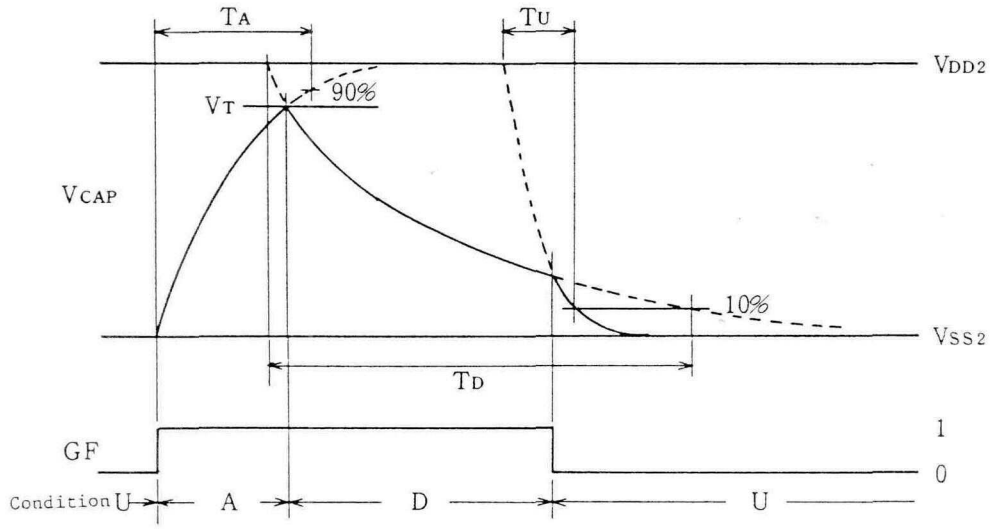
This circuit is used to convert a square wave of frequency by dividing circuit output into amplitude-modulated current output through the amplitude modulation signal. Four circuits are provided for each TG, and the output is connected to the tone bus of 2 ' , 4 ' , 8 ' , and 1 6 ' . The modulation signal is common to the 4 circuits but it can be turned ON/OFF for each feet by the OE bit in the control data.

o Noise Generator

The device is incorporated with the noise generator which employs a pseudo random pulse generator by means of the shift register to generate noise as a noise source. This output is supplied as a noise source for individual tone generators, and at the same time, is constantly output to the NO terminal.



(a) ARM = 1



(b) ARM = 0

Fig. 3 Waveforms Generated by Envelope Generator

Table 1 Pitch Data vs Divided Frequency

Pitch data	Programmable counter divided frequency	Binary divided frequency			
		2′	4′	8′	16′
0	506	1/16	1/32	1/64	1/128
1	478				
2	451				
3	426				
4	402				
5	379				
6	358				
7	338				
8	319				
9	301				
A	284				
B	268				
C	253				
D	478	1/8	1/16	1/32	1/64
E	451				
F	426				
10	402				
1	379				
2	358				
3	338				
4	319				
5	301				
6	284				
7	268				
8	253				
9	478	1/4	1/8	1/16	1/32
A	451				
B	426				
C	402				
D	379				
E	358				
F	338				
20	319				
1	301				
2	284				
3	268				
4	253				
5	478	1/2	1/4	1/8	1/16
6	451				
7	426				

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Pitch data	Programmable counter divided frequency	Binary divided frequency			
		2′	4′	8′	16′
8	402				
9	379				
A	358				
B	338				
C	319				
D	301				
E	284				
F	268				
30	253	1/2	1/4	1/8	1/16
1	478	1/1	1/2	1/4	1/8
2	451				
3	426				
4	402				
5	379				
6	358				
7	338				
8	319				
9	301				
A	284				
B	268				
C	253				
D	478	1/1	1/1	1/2	1/4
E	451				
F	426				
40	402				
1	379				
2	358				
3	338				
4	319				
5	301				
6	284				
7	268				
8	253				
9	478	1/1	1/1	1/1	1/2
A	451				
B	426				
C	402				
D	379				
E	358				
F	338				

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Pitch data	Programmable counter divided frequency	Binary divided frequency			
		2′	4′	8′	16′
50	319				
1	301				
2	284				
3	268				
4	253				
5					
6					
7	13	1/16	1/32	1/64	1/128
7F	(Noise generator)	1/1	1/2	1/4	1/8

Note: The contents of pitch data 57 H are used as data for tests.

Table 2 Output Frequency Error

Tone name	Pitch data	Equal temperament	8' output frequency	Cent error
C	18	261.63 Hz	261.74 Hz	+0.75
C#	19	277.18	277.07	−0.70
D	1A	293.66	293.66	−0.06
D#	1B	311.13	310.89	−1.31
E	1C	329.63	329.45	−0.92
F	1D	349.23	349.45	+1.08
F#	1E	369.99	369.94	−0.24
G	1F	392.00	391.83	−0.71
G#	20	415.30	415.17	−0.55
A	21	440.00	440.00	
A#	22	466.16	466.34	+0.65
B	23	493.88	494.18	+1.04
C	24	523.25	523.48	+0.75

Table 3 Table of Attack Time Data vs Attack Time

Attack time data b_2	b_1	b_0	Resistance ON Duty cycle	Attack time nominal value
0	0	0	1/1	2 ms
0	0	1	1/2	4
0	1	0	1/4	8
0	1	1	1/8	16
1	*	0	1/16	32
1	*	1	1/32	64

*: Don't care
Capacity to be added by external equipment = 0.39UF

Table 4 Table of Decay Time Data vs Decay Time

Decay time data b_3	b_2	b_1	b_0	Resistance ON Duty cycle	Decay time nominal value
0	0	0	0	1/1	40 ms
0	0	0	1	1/2	80
0	0	1	0	1/4	160
0	0	1	1	1/8	320
0	1	*	0	1/16	640
0	1	*	1	1/32	1.3 s
1	0	0	0	1/1	0.33
1	0	0	1	1/2	0.5
1	0	1	0	1/4	1
1	0	1	1	1/8	2
1	1	*	0	1/16	4
1	1	*	1	1/32	8

*: Don't care
Capacity to be added by external equipment = 0.39UF

(Note that a simplified mark may be employed for a product's model name)