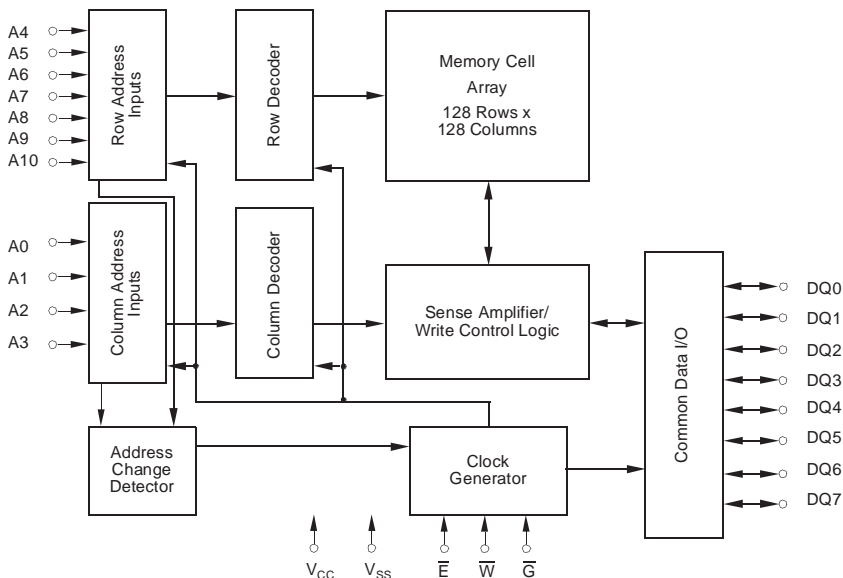




# U6216A

## Block Diagram



## Truth Table

Operating Mode	$\bar{E}$	$\bar{W}$	$\bar{G}$	DQ0 - DQ7
Standby/not selected	H	*	*	High-Z
Internal Read	L	H	H	High-Z
Read	L	H	L	Data Outputs Low-Z
Write	L	L	*	Data Inputs High-Z

\* H or L

## Characteristics

All voltages are referenced to  $V_{SS} = 0$  V (ground).

All characteristics are valid in the power supply voltage range and in the operating temperature range specified.

Dynamic measurements are based on a rise and fall time of  $\leq 5$  ns, measured between 10 % and 90 % of  $V_I$ , as well as

input levels of  $V_{IL} = 0$  V and  $V_{IH} = 3$  V. The timing reference level of all input and output signals is 1.5 V,

with the exception of the  $t_{18}$ -times and  $t_{1(0X)}$ , in which cases transition is measured  $\pm 200$  mV from steady-state voltage.

Maximum Ratings	Symbol	Min.	Max.	Unit
Power Supply Voltage	$V_{CC}$	-0.5	7	V
Input Voltage	$V_I$	-0.5	$V_{CC} + 0.5$	V
Output Voltage	$V_O$	-0.5	$V_{CC} + 0.5$	V
Power Dissipation	$P_D$		1	W
Operating Temperature	$T_a$	0	70	$^{\circ}\text{C}$
	C-Type	-40	85	$^{\circ}\text{C}$
	K-Type			
Storage Temperature	$T_{stg}$	-55	125	$^{\circ}\text{C}$

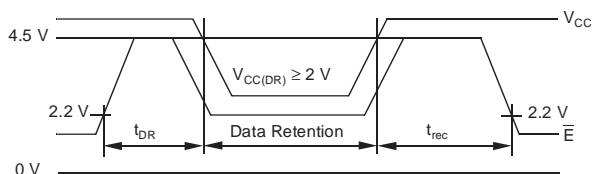
Recommended Operating Conditions	Symbol	Conditions	Min.	Max.	Unit
Power Supply Voltage	$V_{CC}$		4.5	5.5	V
Data Retention Voltage	$V_{CC(DR)}$		2.0		V
Input Low Voltage*	$V_{IL}$		-0.3	0.8	V
Input High Voltage	$V_{IH}$		2.2	$V_{CC} + 0.3$	V

\* -1 V at Pulse Width 50 ns

Electrical Characteristics	Symbol	Conditions	Min.	Max.	Unit
Supply Current - Operating Mode	$I_{CC(OP)}$	$V_{CC} = 5.5\text{ V}$ $V_{IL} = 0.8\text{ V}$ $V_{IH} = 2.2\text{ V}$ $t_{cW} = 70\text{ ns}$ $= 85\text{ ns}$		50 45	mA mA
Supply Current - Standby Mode (CMOS level)	$I_{CC(SB)}$	$V_{CC} = 5.5\text{ V}$ $V(\bar{E}) = V_{CC} - 0.2\text{ V}$		30 5	$\mu\text{A}$ $\mu\text{A}$
Standard Low Power (L)					
Supply Current - Standby Mode (TTL level)	$I_{CC(SB)1}$	$V_{CC} = 5.5\text{ V}$ $V(\bar{E}) = 2.2\text{ V}$		3	mA
Supply Current - Data Retention Mode (Standard)	$I_{CC(DR)}$	$V_{CC(DR)} = 3\text{ V}$ $= 2\text{ V}$ $V(\bar{E}) = V_{CC(DR)} - 0.2\text{ V}$		10 5	$\mu\text{A}$ $\mu\text{A}$
Output High Voltage	$V_{OH}$	$V_{CC} = 4.5\text{ V}$ $I_{OH} = -1.0\text{ mA}$	2.4		V
Output Low Voltage	$V_{OL}$	$V_{CC} = 4.5\text{ V}$ $I_{OL} = 4.0\text{ mA}$		0.4	V
Input High Leakage Current	$I_{IH}$	$V_{CC} = 5.5\text{ V}$ $V_{IH} = 5.5\text{ V}$		2	$\mu\text{A}$
Input Low Leakage Current	$I_{IL}$	$V_{CC} = 5.5\text{ V}$ $V_{IL} = 0\text{ V}$	-2		$\mu\text{A}$
Output High Current	$I_{OH}$	$V_{CC} = 4.5\text{ V}$ $V_{OH} = 2.4\text{ V}$		-1	mA
Output Low Current	$I_{OL}$	$V_{CC} = 4.5\text{ V}$ $V_{OL} = 0.4\text{ V}$	4		mA
Output Leakage Current High at Three-State Outputs	$I_{OHZ}$	$V_{CC} = 5.5\text{ V}$ $V_{OH} = 5.5\text{ V}$		2	$\mu\text{A}$
Low at Three-State Outputs	$I_{OLZ}$	$V_{CC} = 5.5\text{ V}$ $V_{OL} = 0\text{ V}$	-2		$\mu\text{A}$

Switching Characteristics	Symbol		Min.		Max.		Unit
	Alt.	IEC	07	08	07	08	
Time to Output in Low-Z	$t_{LZ}$	$t_{l(QX)}$	5	5	10	10	ns
Cycle Time							
Write Cycle Time	$t_{WC}$	$t_{cW}$	70	85			ns
Read Cycle Time	$t_{RC}$	$t_{cR}$	70	85			ns
Access Time							
$\bar{E}$ LOW to Data Valid	$t_{ACE}$	$t_{a(E)}$			70	85	ns
$\bar{G}$ LOW to Data Valid	$t_{OE}$	$t_{a(G)}$			35	45	ns
Address to Data Valid	$t_{AA}$	$t_{a(A)}$			70	85	ns
Pulse Widths							
Write Pulse Width	$t_{WP}$	$t_{w(W)}$	40	50			ns
Chip Enable to End of Write	$t_{CW}$	$t_{w(E)}$	45	55			ns
Setup Times							
Address Setup Time	$t_{AS}$	$t_{su(A)}$	0	0			ns
Chip Enable to End of Write	$t_{CW}$	$t_{su(E)}$	45	55			ns
Write Pulse Width	$t_{WP}$	$t_{su(W)}$	40	50			ns
Data Setup Time	$t_{DS}$	$t_{su(D)}$	30	30			ns
Data Hold Time							
Address Hold from End of Write	$t_{DH}$	$t_{h(D)}$	0	0			ns
	$t_{AH}$	$t_{h(A)}$	0	0			ns
Output Hold Time from Address Change	$t_{OH}$	$t_{v(A)}$	5	5			ns
$\bar{E}$ HIGH to Output in High-Z	$t_{HZCE}$	$t_{dis(E)}$	0	0	30	30	ns
$\bar{W}$ LOW to Output in High-Z	$t_{HZWE}$	$t_{dis(W)}$	0	0	25	30	ns
$\bar{G}$ HIGH to Output in High-Z	$t_{HZOE}$	$t_{dis(G)}$	0	0	30	30	ns

## Data Retention Mode



$$V_{CC(DR)} - 0.2 \text{ V} \leq V_{\bar{E}(DR)} \leq V_{CC(DR)} + 0.3 \text{ V}$$

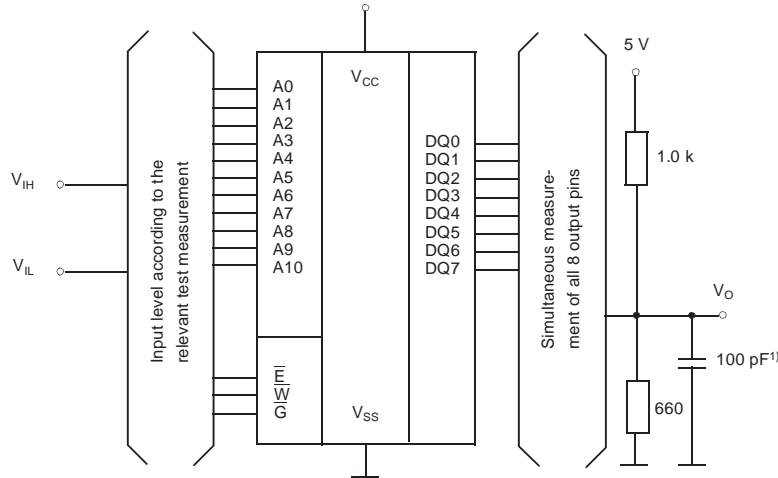
Chip Deselect to Data Retention Time

$t_{DR}$ : min 0 ns

Operating Recovery Time

$t_{rec}$ : min  $t_{cR}$

## Test Configuration for Functional Check



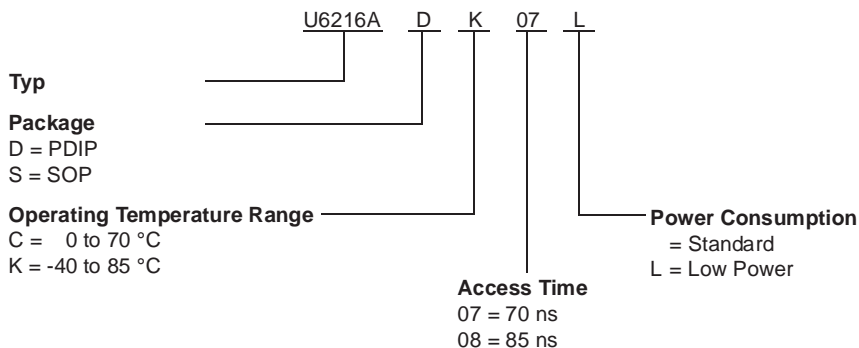
1) In measurement of  $t_{dis(E)}$ ,  $t_{dis(W)}$ ,  $t_{dis(G)}$ ,  $t_t(QX)$  the capacitance is 5 pF.

Capacitance	Conditions	Symbol	Min.	Max.	Unit
Input Capacitance	$V_{CC} = 5.0\text{ V}$ $V_I = V_{SS}$	$C_I$		7	pF
Output Capacitance	$f = 1\text{ MHz}$ $T_a = 25\text{ °C}$	$C_O$		7	pF

All pins not under test must be connected with ground by capacitors.

## IC Code Numbers

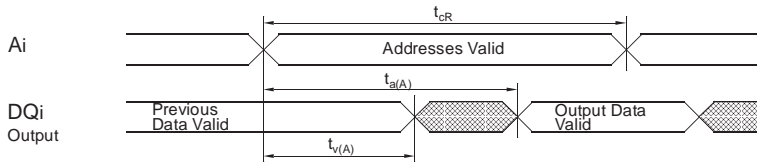
Example



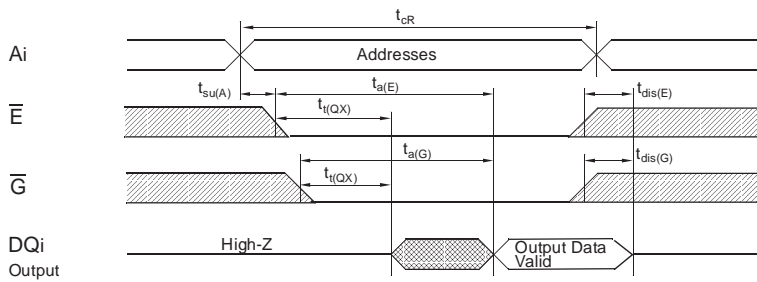
The date of manufacture is given by the 4 last digits of the mark, the first 2 digits indicating the year, and the last 2 digits the calendar week.

# U6216A

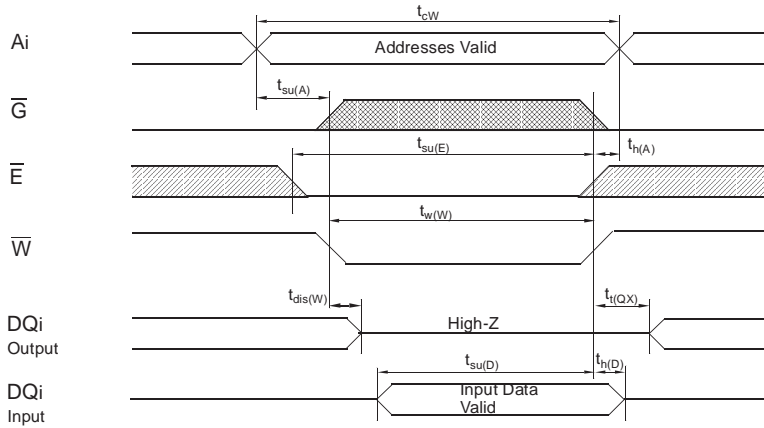
Read Cycle 1 (during Read cycle :  $\overline{E} = \overline{G} = V_{IL}, \overline{W} = V_{IH}$ )



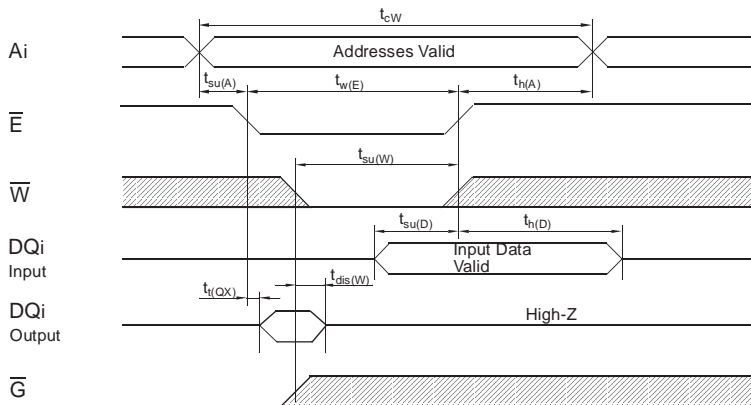
Read Cycle 2 (during Read cycle:  $\overline{W} = V_{IH}$ )



Write Cycle1 ( $\overline{W}$ -controlled)



Write Cycle 2 ( $\overline{E}$ -controlled)



undefined



L- or H-level





Zentrum Mikroelektronik Dresden

## **Memory Products 1998**

### **Standard 2K x 8 SRAM U6216A**

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