2107C FAMILY
4096-BIT DYNAMIC RAM

	2107C-1	2107C-2	2107C	2107C-4
Access Time (ns)	150	200	250	300
Read, Write Cycle (ns)	380	400	430	470
RMW Cycle (ns)	450	500	550	590
Max $I_{DD\ AV}$ (mA)	35	33	30	30

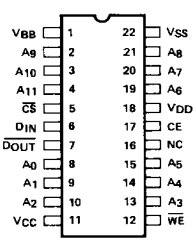
- **Direct Replacement for Industry Standard 22-Pin 4K RAMs**
- **Low Operating Power**
- **Low Standby Power**
- **Only One High Voltage Input Signal-Chip Enable**
- **150 ns Access Time**
- **±10% Tolerance on all Power Supplies**
- **Output is Three-State and TTL Compatible**
- **TTL Compatible — All Address, Data, Write Enable, Chip Select Inputs**
- **Refresh Period 2 ms**

The Intel® 2107C is a 4096-word by 1-bit dynamic n-channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. A new unique dynamic storage cell provides high speed and wide operating margins. The 2107C uses dynamic circuitry which reduces the standby power dissipation.

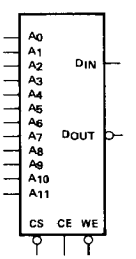
Reading information from the memory is non-destructive. Refreshing is most easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic one or a logic zero.

The 2107C is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than other MOS technologies. The 2107C is a replacement for the 2107A, 2107B and other industry standard 22-pin 4K RAMs.

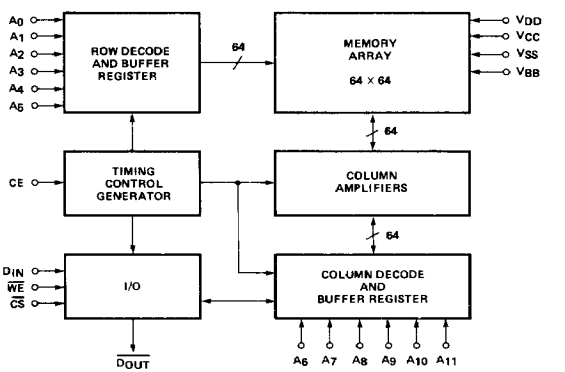
PIN CONFIGURATION
2107C



LOGIC SYMBOL
2107C



BLOCK DIAGRAM



PIN NAMES

A0–A11	ADDRESS INPUTS*	VBB	POWER (–5V)
CE	CHIP ENABLE	VCC	POWER (+5V)
CS	CHIP SELECT	VDD	POWER (+12V)
DIN	DATA INPUT	VSS	GROUND
DOUT	DATA OUTPUT	WE	WRITE ENABLE
NC	NOT CONNECTED		

*Refresh Address A0–A5.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . . -65°C to +150°C

Voltage on any Pin Relative to V_{BB} ($V_{SS} - V_{BB} \geq 4.5$) . . . . . -0.3V to +20V

Power Dissipation 1.00W

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB}[1] = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)			10	µA	V_{IN} = 0V to $V_{IH\ MAX}$ CE = V_{ILC} or V_{IHC}
I_{LC}	Input Load Current, CE			2	µA	V_{IN} = 0V to $V_{IHC\ MAX}$
$\|I_{LO}\|$	Output Leakage Current for high impedance state			10	µA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.5V
I_{DD1}[3]	V_{DD} Supply Current – standby[3]		20	200	µA	CE = -1V to +0.6V
$I_{DD\ AV}$	Average V_{DD} Current – operating		24	35	mA	2107C-1, t_{CYC} = 380
			22	33	mA	2107C-2, t_{CYC} = 400
			20	30	mA	2107C, t_{CYC} = 430
			20	30	mA	2107C-4, t_{CYC} = 470
I_{CC1}[3,4]	V_{CC} Supply Current – standby			10	µA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
I_{BB1}	V_{BB} Supply Current – standby		5	50	µA	CE = -1V to +0.6V
$I_{BB\ AV}$	Average V_{BB} Current – operating		100	400	µA	Min. cycle time, Min. t_{CE}
V_{IL}	Input Low Voltage	-1.0		0.8	V	
V_{IH}	Input High Voltage	2.4		V_{CC}+1	V	
V_{ILC}	CE Input Low Voltage	-1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD}-1		V_{DD}+1	V	
V_{OL}	Output Low Voltage	0.0		0.40	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -2.0 mA

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V or more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}.
4. During CE on V_{CC} supply current is dependent on output loading. V_{CC} is connected to output buffer only.

A.C. Characteristics [1]

$T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

READ, WRITE, AND READ MODIFY/WRITE CYCLE

Symbol	Parameter	2107C-1		2107C-2		2107C		2107C-4		Units	Note
		Min.	Max	Min.	Max.	Min.	Max.	Min.	Max.		
t_{REF}	Time Between Refresh		2		2		2		2	ms	
t_{AC}	Address to CE Set-Up Time	0		0		0		0		ns	2
t_{AH}	Address Hold Time	50		50		100		100		ns	
t_{CC}	CE Off Time	130		130		130		130		ns	
t_T	CE Transition Time		40		40		40		40	ns	
t_{CD}	CE Off to Output Disable Time	30		30		30		30		ns	3

READ CYCLE

Symbol	Parameter	2107C-1		2107C-2		2107C		2107C-4		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{CY}	Cycle Time	380		400		430		470		ns	3
t_{CE}	CE On Time	210	4000	230	4000	260	4000	300	4000	ns	
t_{CO}	CE Output Delay		130		180		230		280	ns	4
t_{ACC}	Address to Output Access		150		200		250		300	ns	5
t_{WL}	CE to $\overline{WE}$	0		0		0		0		ns	
t_{WC}	$\overline{WE}$ to CE On	0		0		0		0		ns	

WRITE CYCLE

Symbol	Parameter	2107C-1		2107C-2		2107C		2107C-4		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{CY}	Cycle Time	380		400		430		470		ns	3
t_{CE}	CE On Time	210	4000	230	4000	260	4000	300	4000	ns	
t_W	$\overline{WE}$ to CE Off	125		125		125		175		ns	
t_{CW}	CE to $\overline{WE}$	150		150		150		200		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set-Up	0		0		0		0		ns	6
t_{DH}	D_{IN} Hold Time	0		0		0		0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	50		50		50		100		ns	
t_{WD}	$\overline{WE}$ to Output Disable Time	15		15		15		15			

Capacitance [7] $T_A = 25°C$

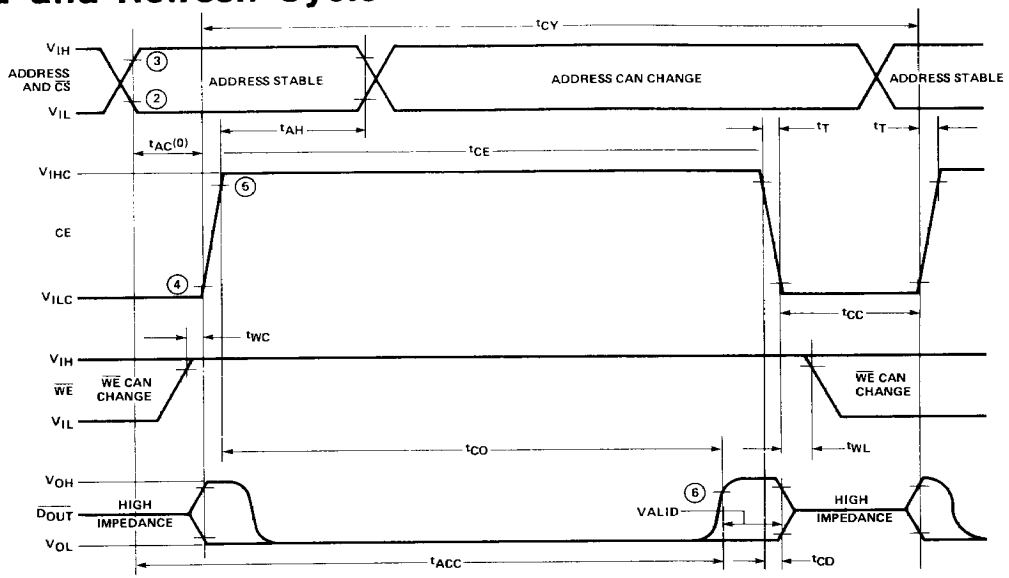
Symbol	Test	Plastic and Ceramic Package		Unit	Conditions
		Typ.	Max.		
C_{AD}	Address Capacitance, $\overline{CS}$, D_{IN}	5	7	pF	$V_{IN} = V_{SS}$
C_{CE}	CE Capacitance	10	15	pF	$V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance	5	7	pF	$V_{OUT} = 0V$
$C_{\overline{WE}}$	$\overline{WE}$ Capacitance	6	8	pF	$V_{IN} = V_{SS}$

NOTES:

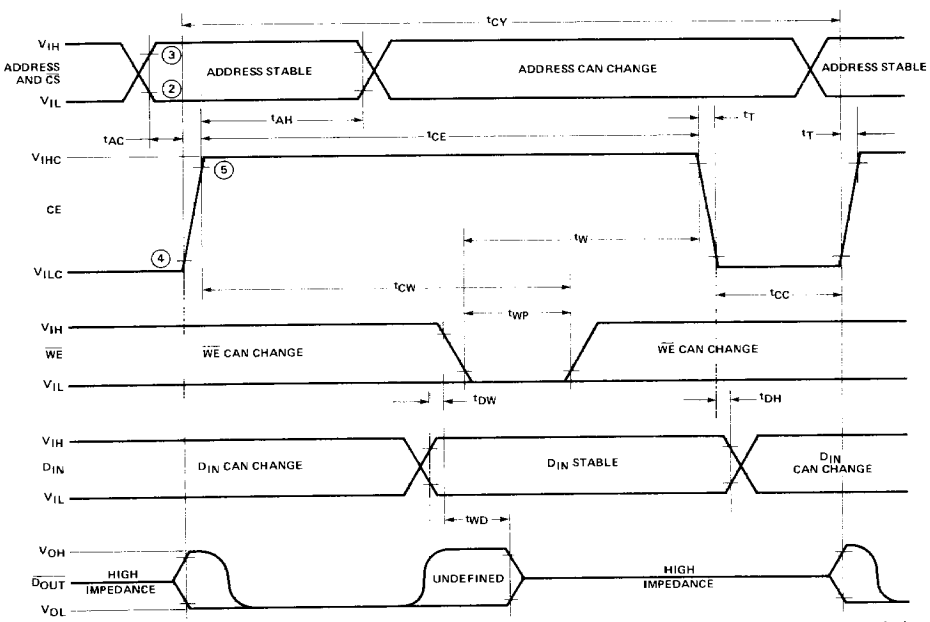
1. After the application of supply voltages or after extended periods of operation without CE, the device must perform a minimum of one initialization cycle (any valid memory cycle or refresh cycle) prior to normal operation.
2. t_{AC} is measured from end of address transition.
3. $t_T = 20$ ns.
4. $C_{LOAD} = 50$ pF, Load = One TTL Gate, Ref = 2.0V.
5. $t_{ACC} = t_{AC} + t_{CO} + 1t_T$.
6. If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.
7. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:

$$C = \frac{I\Delta t}{\Delta V}$$ with the current equal to a constant 20 mA.

Read and Refresh Cycle [1]



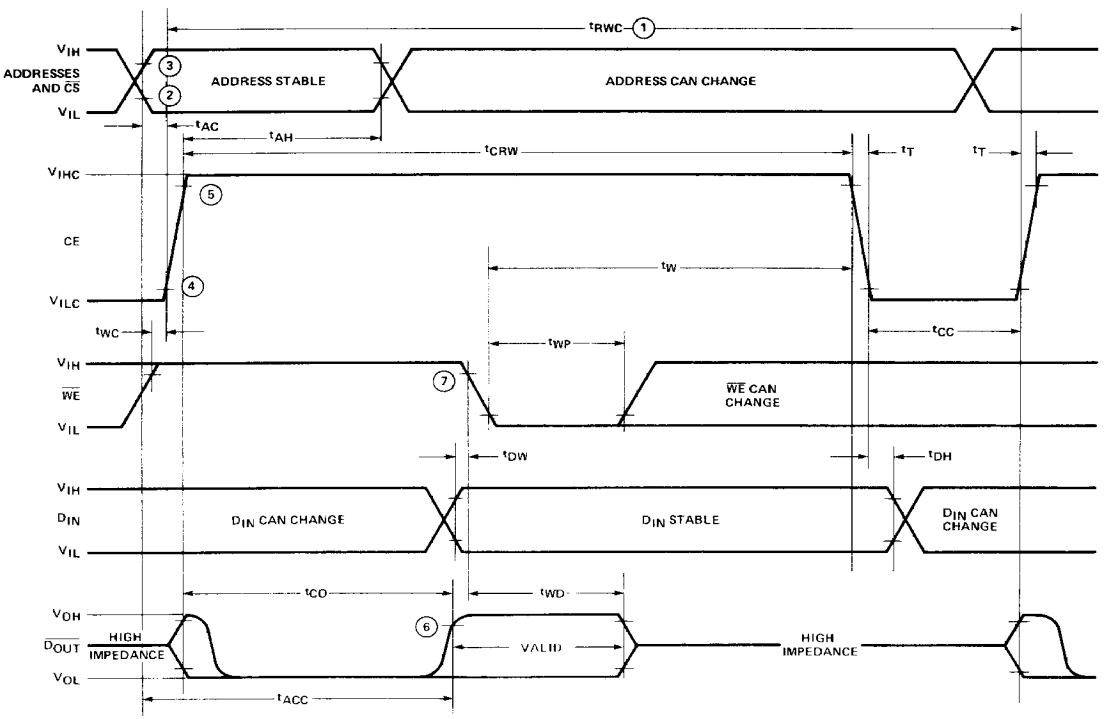
Write Cycle



NOTES:
1. For Refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IN} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} −2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.

Read Modify Write Cycle

Symbol	Parameter	2107C-1		2107C-2		2107C		2107C-4		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RWC}	Read Modify Write (RMW) Cycle	450		500		550		590		ns	1
t_{CRW}	CE Width During RMW	280	4000	330	4000	380	4000	420	4000	ns	
t_{WC}	$\overline{WE}$ to CE On	0		0		0		0		ns	
t_W	$\overline{WE}$ to CE Off	125		125		125		175		ns	
t_{WP}	$\overline{WE}$ Pulse Width	50		50		50		100		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Setup	0		0		0		0		ns	
t_{DH}	D_{IN} Hold Time	0		0		0		0		ns	
t_{CO}	CE to Output Delay		130		180		230		280	ns	
t_{ACC}	Access Time		150		200		250		300	ns	
t_{WD}	$\overline{WE}$ to Output Disable Time	15		15		15		15		ns	



NOTES:
1. t_T of 20 ns.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} –2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$. C_{LOAD} = 50 pF. Load = One TTL Gate.
7. $\overline{WE}$ must be at V_{IH} until end of t_{CO}.