FAIRCHILD
A Schlumberger Company

F6840/F68A40/F68B40 Programmable Timer (PTM)

Microprocessor Product

Description

The F6840 is a programmable subsystem component of the F6800 family designed to provide variable system time intervals.

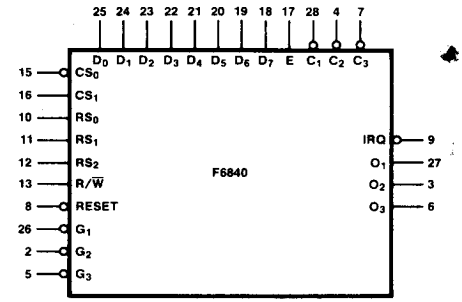
The F6840 has three 16-bit binary counters, three corresponding control registers and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals. The F6840 may be utilized for such tasks as frequency measurements, event counting, interval measuring and similar tasks. The device may be used for square wave generation, gated delay signals, single pulses of controlled duration, and pulse width modulation, as well as system interrupts.

- **Operates From a Single +5V Power Supply**
- **Fully TTL-Compatible**
- **Single System Clock Required (Enable)**
- **Selectable Prescaler on Timer 3 Capable of 4 MHz for the F6840, 6 MHz for the F68A40, and 8 MHz for the F68B40**
- **Programmable Interrupt ($\overline{IRQ}$) Output to MPU**
- **Readable Down Counter Indicates Counts to Go to Time-Out**
- **Selectable Gating for Frequency or Pulse-Width Comparison**
- **$\overline{RESET}$ Input**
- **Three Asynchronous External Clock and Gate/Trigger Inputs Internally Synchronized**
- **Three Maskable Outputs**

Pin Names

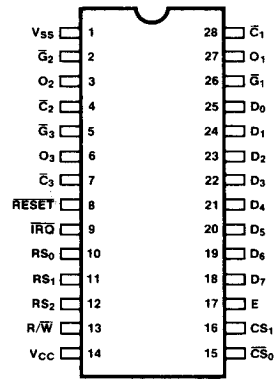
D_0-D_7	Bidirectional Data Lines
$\overline{CS}_0$-CS_1	Chip Select Input
R/$\overline{W}$	Read/Write Input
E	Enable (Systems Clock $\phi 2$) Input
$\overline{IRQ}$	Interrupt Request Output
$\overline{RESET}$	Reset Input
RS_0-RS_2	Register Select Inputs
$\overline{C}_1$-$\overline{C}_3$	Counter Clock Inputs
$\overline{G}_1$-$\overline{G}_3$	Counter Gate Inputs
O_1-O_3	Counter Outputs

Logic Symbol



V_{CC} = Pin 14
V_{SS} = Pin 1

Connection Diagram 28-Pin DIP



(Top View)

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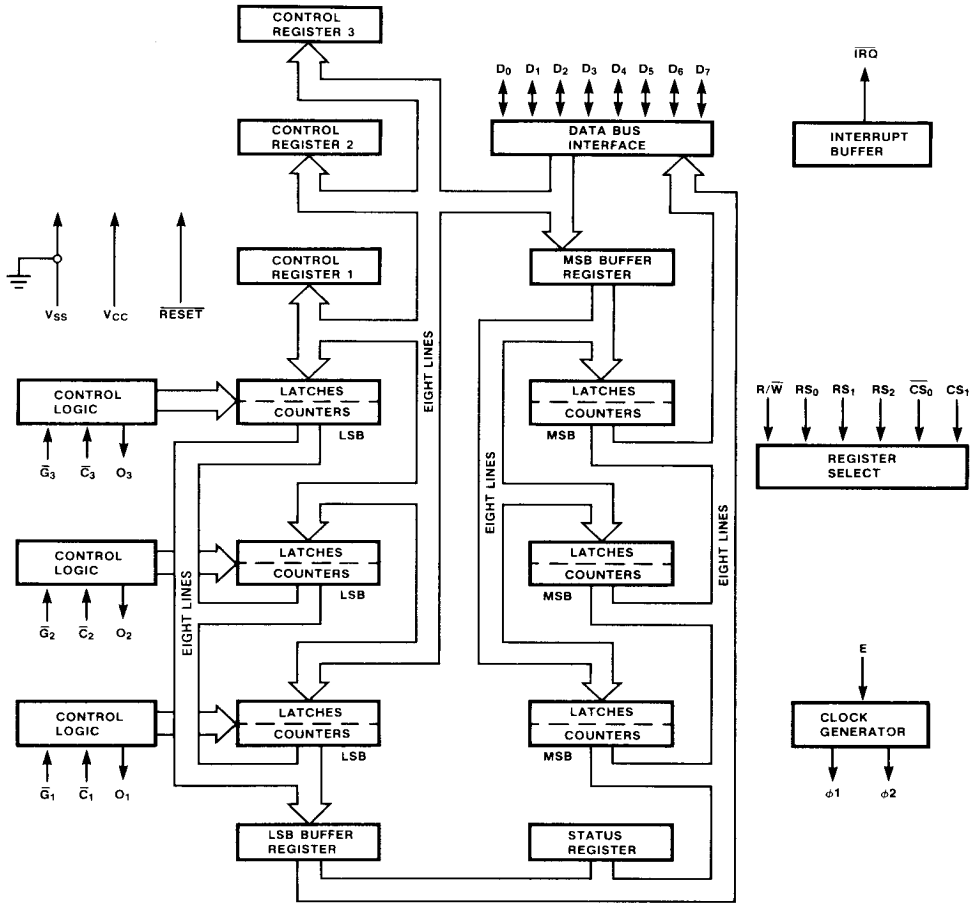
Block Diagram



Functional Description

The three timers in the F6840 may be programmed independently to operate in modes which fit a wide variety of applications. The device is fully bus-compatible with F6800 systems and is accessed by load and store operations from the MPU in much the same manner as a memory device. In a typical application, a timer will be loaded by storing two bytes of data into an associated counter latch. This data then is transferred into the counter during a counter initialization cycle. The counter decrements on each subsequent clock period, which may be an external clock or Enable (System $\phi 2$) until one of several predetermined conditions causes it to halt or recycle. The timers are thus programmable, cyclic in nature, controllable by external inputs or the MPU program, and accessible by the MPU at any time.

Bus Interface

The programmable timer module (PTM) interfaces to the F6800 bus with an 8-bit bidirectional data bus, two Chip Select lines, a Read/Write line, an Enable (System $\phi 2$)

line, an Interrupt Request line, an external $\overline{RESET}$ line, and three Register Select lines. These signals, in conjunction with the F6800 VMA output, permit the MPU to control the PTM. VMA should be utilized in conjunction with the MPU address line into a Chip Select of the PTM.

Bidirectional Data (D_0-D_7)
The bidirectional Data Lines (D_0-D_7) allow the transfer of data between the MPU and the PTM. The data bus output drivers are 3-state devices which remain in the high-impedance (OFF) state except when the MPU performs a PTM read operation (Read/Write and Enable lines HIGH and PTM Chip Selects activated).

Chip Select ($\overline{CS_0}$, CS_1)
These two signals are used to activate the data bus interface and allow transfer of data from the PTM. With $\overline{CS_0}$ = "0" and CS_1 = "1", the device is selected and data transfer will occur.

Read/Write (R/$\overline{W}$)
This signal is generated by the MPU to control the direction of data transfer on the data bus. With the PTM selected, a LOW state on the PTM R/$\overline{W}$ line enables the input buffers and data is transferred from the MPU to the PTM on the trailing edge of the Enable (System $\phi 2$) signal. Alternately (under the same conditions), R/$\overline{W}$ = "1" and Enable HIGH allows data in the PTM to be read by the MPU.

Enable (E, System $\phi 2$)
This signal synchronizes data transfer between the MPU and the PTM. It also performs an equivalent synchronization function on the external Clock, $\overline{RESET}$, and Gate inputs of the PTM.

Interrupt Request ($\overline{IRQ}$)
The active LOW Interrupt Request signal is normally tied directly (or through priority interrupt circuitry) to the $\overline{IRQ}$ input of the MPU. This is an open drain output (no load device on the chip) which permits other similar Interrupt Request lines to be tied together in a wired-OR configuration.

The $\overline{IRQ}$ line is activated if, and only if, the composite interrupt flag (bit 7 of the internal status register) is asserted. The conditions under which the IRQ line is activated are discussed in conjunction with the status register.

External $\overline{RESET}$
A LOW level at this input is clocked into the PTM by the Enable (System $\phi 2$) input. Two Enable pulses are required to synchronize and process the signal. The PTM then recognizes the active LOW or inactive HIGH on the third Enable pulse. If the $\overline{RESET}$ signal is asynchronous, an additional Enable period is required if set-up times are not met. The $\overline{RESET}$ input must be stable HIGH/LOW for the minimum time stated in the *AC Characteristics* table.

Recognition of a LOW level at this input by the PTM causes the following action to occur:
a. All counter latches are preset to their maximal count values.
b. All control register bits are cleared with the exception of $CR1_0$ (internal reset bit), which is set.
c. All counters are preset to the contents of the latches.
d. All counter outputs are reset and all counter clocks are disabled.
e. All status register bits (interrupt flags) are cleared.

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Table 1 Register Selection

Register Select Inputs			Operations	
RS_2	RS_1	RS_0	R/$\overline{W}$ = "0"	R/$\overline{W}$ = "1"
0	0	0	$CR2_0$ = "0" Write Control Register 3 $CR2_0$ = "1" Write Control Register 1	No Operation
0	0	1	Write Control Register 2	Read Status Register
0	1	0	Write MSB Buffer Register	Read Timer 1 Counter
0	1	1	Write Timer 1 Latches	Read LSB Buffer Register
1	0	0	Write MSB Buffer Register	Read Timer 2 Counter
1	0	1	Write Timer 2 Latches	Read LSB Buffer Register
1	1	0	Write MSB Buffer Register	Read Timer 3 Counter
1	1	1	Write Timer 3 Latches	Read LSB Buffer Register

Register Select Lines (RS_0, RS_1, RS_2)
These inputs are used in conjunction with the R/$\overline{W}$ line to select the internal registers, counters and latches as shown in *Table 1*.

It has been stated previously that the PTM is accessed via MPU load and store operations in much the same manner as a memory device. The instructions available with the F6800 family of MPUs which perform operations directly on memory should not be used when the PTM is accessed. These instructions actually fetch a byte from memory, perform an operation, then restore it to the same address location. Since the PTM uses the R/$\overline{W}$ line as an additional register select input, the modified data may not be restored to the same register if these instructions are used.

Control Register
Three write-only registers in the F6840 are used to modify timer operation to suit a variety of applications. Control register 2 has a unique address space (RS_0 = "1", RS_1 = "0", RS_2 = "0") and therefore may be written into any time. The remaining control registers (1 and 3) share the address space selected by a logic "0" on all register select inputs. The least significant bit of control register 2 ($CR2_0$) is used as an additional addressing bit for control registers 1 and 3. Thus, with all Register Selects and R/$\overline{W}$ inputs at logic "0", control register 3 will be written into if $CR2_0$ is a logic "0". Control register 3 can also be written into after a reset LOW condition has occurred, since all control register bits (except $CR1_0$) are cleared. Therefore, one may write in the sequence CR_3, CR_2, CR_1.

The least significant bit of control register 1 is used as an internal reset bit. When this bit is a logic "0", all timers are allowed to operate in the modes prescribed by the remaining bits of the control registers. Writing a "1" into $CR1_0$ causes all counters to be preset with the contents of the corresponding counter latches, all counter clocks to be disabled, and the timer outputs and interrupt flags (status register) to be reset. Counter latches and control registers are undisturbed by an internal reset and may be written into regardless of the state of $CR1_0$.

The least significant bit of control register 3 is used as a selector for a ÷8 prescaler, which is available with timer 3 only. The prescaler, if selected, is effectively placed between the clock input circuitry and the input to counter 3. It therefore can be used with either the internal clock (Enable) or an external clock source.

The functions depicted in the foregoing discussions are tabulated on the first row in *Table 2* for ease of reference.

Control register bits $CR1_0$, $CR2_0$ and $CR3_0$ are unique in that each selects a different function. The remaining bits (1 through 7) of each control register select common functions, with a particular control register affecting only

Table 2 Control Register Bits

$CR1_0$ Internal Reset Bit	$CR2_0$ Control Register Address Bit	$CR3_0$ Timer 3 Clock Control
0 All timers allowed to operate	**0** CR3 may be written	**0** T_3 $\overline{\text{Clock}}$ is not prescaled
1 All timers held in preset state	**1** CR1 may be written	**1** T_3 $\overline{\text{Clock}}$ is prescaled by ÷8
CRX_1*	Timer X $\overline{\text{Clock}}$ Source	
0	TX uses external clock source on $\overline{CX}$ input	
1	TX uses Enable clock	
CRX_2	Timer X Counting Mode Control	
0	TX configured for normal (16-bit) counting mode	
1	TX configured for dual 8-bit counting mode	
CRX_3 CRX_4 CRX_5	Timer X Counter Mode and Interrupt Control (See *Table 3*)	
CRX_6	Timer X Interrupt Enable	
0	Interrupt Flag masked on $\overline{IRQ}$	
1	Interrupt Flag enabled to $\overline{IRQ}$	
CRX_7	Timer X counter Output Enable	
0	TX Output masked on output OX	
1	TX Output enabled on output OX	

*Control Register for timer 1, 2 or 3, Bit 1.

its corresponding timer. For example, bit 1 of control register 1 ($CR1_1$) selects whether an internal or external clock source is to be used with timer 1. Similarly, $CR2_1$ selects the clock source for timer 2, and $CR3_1$ performs this function for timer 3. The function of each bit of control register "X" can therefore be defined as shown in the remaining section of *Table 2*.

Control register bit 2 selects whether the binary information contained in the counter latches (and subsequently loaded into the counter) is to be treated as a single 16-bit word or two 8-bit bytes. In the single 16-bit counter mode ($CR2 = "0"$), the counter will decrement to zero after $N + 1$ enabled ($\overline{G} = "0"$) clock periods, where N is defined as the 16-bit number in the counter latches. With $CRX_2 = "1"$, a similar time-out will occur after $(L + 1) \cdot (M + 1)$ enabled clock periods, where L and M, respectively, refer to the LSB and MSB bytes in the counter latches.

Control register bits 3, 4, and 5 are explained in detail in the Timer Operating Modes section. Bit 6 is an interrupt mask bit which will be explained more fully in conjunction with the status register, and bit 7 is used to enable the corresponding timer output. A summary of control register programming modes is shown in *Table 3*.

Status Register/Interrupt Flags

The F6840 has an internal read-only status register which contains four interrupt flags. (The remaining four bits of the register are not used, and default to "0s" when being read). Bits 0, 1, and 2 are assigned to timers 1, 2, and 3, respectively, as individual flag bits, while bit 7 is a composite interrupt flag. This flag bit will be asserted if any of the individual flag bits is set while bit 6 of the corresponding control register is at a logic "1". The conditions for asserting the composite interrupt flag bit can therefore be expressed as:

$$INT = I_1 \cdot CR1_6 + I_2 \cdot CR2_6 + I_3 \cdot CR3_6$$

where INT = Composite Interrupt Flag (Bit 7)
I_1 = Timer 1 Interrupt Flag (Bit 0)
I_2 = Timer 2 Interrupt Flag (Bit 1)
I_3 = Timer 3 Interrupt Flag (Bit 2)

An interrupt flag is cleared by a timer reset condition; i.e., external $\overline{RESET} = "0"$ or internal reset bit ($CR1_0$) = "1". It will also be cleared by a read timer counter command, provided that the status register has previously been read while the interrupt flag was set. This condition on the read status register — read timer counter (RS-RT) sequence is designed to prevent missing interrupts which might occur after the status register is read, but prior to reading the timer counter.

An individual interrupt flag is also cleared by a write timer latches (W) command or a counter initialization (CI) sequence, provided that W or CI affects the timer corresponding to the individual interrupt flag.

Counter Latch Initialization

Each of the three independent timers consists of a 16-bit addressable counter and 16 bits of addressable latches. The counters are preset to the binary numbers stored in the latches. Counter initialization results in the transfer of the latch contents to the counter. See the notes in *Table 5* regarding the binary number N, L or M placed into the latches and their relationship to the output waveforms and counter time outs.

Since the PTM data bus is 8 bits wide and the counters are 16 bits wide, a temporary register (MSB buffer register) is provided. This write-only register is for the most significant byte of the desired latch data. Three addresses are provided for the MSB buffer register (as indicated in *Table 1*), but they all lead to the same buffer. Data from the MSB buffer will be transferred automatically into the most significant byte of timer X when a write timer X latches command is performed. So it can be seen that the F6840 has been designed to allow transfer of two bytes of data into the counter latches provided that the MSB is transferred first.

In the many applications, the source of the data will be an F6800 MPU. It should be noted that the 16-bit store operations of F6800 family microprocessors (STS and STX) transfer data in the order required by the PTM. A store index register instruction, for example, results in the MSB of the X register being transferred to the selected address, then the LSB of the X register being written into the next higher location. Thus, either the index register or stack pointer may be transferred directly into a selected counter latch with a single instruction.

A logic "0" at the $\overline{RESET}$ input also initializes the counter latches. In this case, all latches will assume a maximum count of $65{,}536_{10}$. It is important to note that an internal reset (bit zero of control register 1 set) has no effect on the counter latches.

Counter Initialization

Counter initialization is defined as the transfer of data from the latches to the counter with subsequent clearing of the individual interrupt flag associated with the counter. Counter initialization always occurs when a reset condition ($\overline{RESET} = "0"$ or $CR1_0 = "1"$ is recognized. It can also occur — depending on timer mode — with a write timer latches command or recognition of a negative transition of the gate input.

Table 3 Control Register Programming

7	6	5	4	3	2	1	0	Register 1	Register 2	Register 3
X	X	X	X	X	X	X	↕	0 All timers operate	Reg #3 may be written	T3 Clk ÷ 1
								1 All timers preset	Reg #1 may be written	T3 Clk ÷ 8

7	6	5	4	3	2	1	0	
X	X	X	X	X	X	↕	X	0 External Clock ($\overline{CX}$ Input) 1 Internal Clock (Enable)

7	6	5	4	3	2	1	0	
X	X	X	X	X	↕	X	X	0 Normal (16-Bit) Count Mode 1 Dual 8-Bit Count Mode

7	6	5	4	3	2	1	0	
X	X	0	0	0	X	X	X	Continuous Operating Mode: $\overline{Gate}$ ↓ or Write to Latches or Reset Causes Counter Initialization
X	X	0	0	1	X	X	X	Frequency Comparison Mode: Interrupt if $\overline{Gate}$ ↓ ⌐¬ ↓ is < Counter Time-Out
X	X	0	1	0	X	X	X	Continuous Operating Mode: $\overline{Gate}$ ↓ or Reset Causes Counter Initialization
X	X	0	1	1	X	X	X	Pulse Width Comparison Mode: Interrupt if $\overline{Gate}$ ↓ ‾‾‾ ↑ is < Counter Time-Out
1	X	1	0	0	X	X	X	Single Shot Mode: $\overline{Gate}$ ↓ or Write to Latches or Reset Causes Counter Initialization
X	X	1	0	1	X	X	X	Frequency Comparison Mode: Interrupt if $\overline{Gate}$ ↓ ⌐¬ ↓ is > Counter Time-Out
1	X	1	1	0	X	X	X	Single Shot Mode: $\overline{Gate}$ ↓ or Reset Causes Counter Initialization
X	X	1	1	1	X	X	X	Pulse Width Comparison Mode: Interrupt if $\overline{Gate}$ ↓ ‾‾‾ ↑ is > Counter Time-Out

7	6	5	4	3	2	1	0	
X	↕	X	X	X	X	X	X	0 Interrupt Flag Masked ($\overline{IRQ}$) 1 Interrupt Flag Enabled ($\overline{IRQ}$)

7	6	5	4	3	2	1	0	
↕	X	X	X	X	X	X	X	0 Timer Output Masked 1 Timer Output Enabled

Note
Reset is Hardware or Software Reset ($\overline{RESET}$ = 0 or CR_{10} = 1).

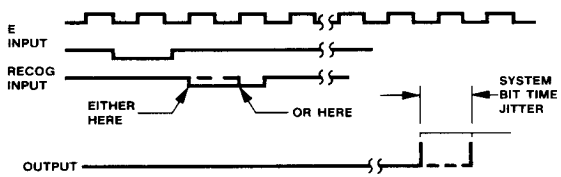
Counter recycling or re-initialization occurs when a negative transition of the clock input is recognized after the counter has reached an all-"0" state. In this case, data is transferred from the latches to the counter.

Asynchronous Input/Output Lines

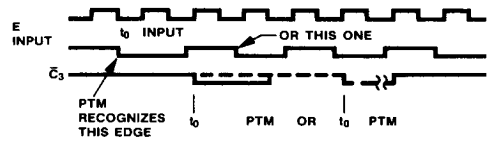
Each of the three timers within the PTM has external clock and gate inputs as well as a counter output line. The inputs are high impedance, TTL-compatible lines and outputs are capable of driving two standard TTL loads.

Clock Inputs ($\overline{C}_1$, $\overline{C}_2$ and $\overline{C}_3$)
Input pins $\overline{C}_1$, $\overline{C}_2$ and $\overline{C}_3$ will accept asynchronous TTL voltage level signals to decrement timers 1, 2 and 3, respectively. The HIGH and LOW levels of the external clocks must each be stable for at least one system clock period plus the sum of the set-up and hold times for the inputs. The asynchronous clock rate can vary from dc to the limit imposed by Enable (System $\phi 2$) set-up and hold time.

The external clock inputs are clocked in by Enable (System $\phi 2$) pulses. Three enable periods are used to synchronize and process the external clock. The fourth Enable pulse decrements the internal counter. This does not affect the input frequency, it merely creates a delay between a clock input transition and internal recognition of that transition by the PTM. All references to $\overline{C}$ inputs in this document relate to internal recognition of the input transition. Note that a clock HIGH or LOW level which does not meet set-up and hold time specifications may require an additional Enable pulse for recognition. When observing recurring events, a lack of synchronization will result in jitter being observed on the output of the PTM when using asynchronous clocks and gate input signals. There are two types of jitter. System jitter is the result of the input signals being out of synchronization with the Enable input (System $\phi 2$), permitting signals with marginal set-up and hold time to be recognized by either the bit time nearest the input transition or the subsequent bit time.



Input jitter can be as great as the time between input signal negative going transitions plus the system jitter, if the first transition is recognized during one system cycle, and not recognized the next cycle, or vice versa.



External clock input $\overline{C}_3$ represents a special case when timer 3 is programmed to utilize its optional ÷8 prescaler mode. The maximum input frequency and allowable duty cycles for this case are specified in the *AC Characteristics* table. The output of the ÷8 prescaler is treated in the same manner as the previously discussed clock inputs. That is, it is clocked into the counter by Enable pulses, is recognized on the fourth Enable pulse (provided set-up and hold time requirements are met), and must produce an output pulse at least as wide as the sum of an enable period, set-up and hold times.

Gate Inputs ($\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$)
Input lines $\overline{G}_1$, $\overline{G}_2$ and $\overline{G}_3$ accept asynchronous TTL-compatible signals which are used as triggers or clock gating functions to timers 1, 2 and 3, respectively. The gating inputs are clocked into the PTM by the Enable (System $\phi 2$) signal in the same manner as the previously discussed Clock inputs. That is, a Gate transition is recognized by the PTM on the fourth Enable pulse (provided set-up and hold time requirements are met), and the HIGH or LOW levels of the Gate input must be stable for at least one system clock period plus the sum of the set-up and hold times. All references to $\overline{G}$ transition in this document relate to internal recognition of the input transition.

The Gate inputs of all timers directly affect the internal 16-bit counter. The operation of $\overline{G}_3$ is therefore independent of the ÷8 prescaler selection.

Timer Outputs (O_1, O_2, O_3)
Timer outputs O_1, O_2 and O_3 are capable of driving up to two TTL loads and produce a defined output waveform for either continuous or single-shot timer modes. Output waveform definition is accomplished by selecting either single 16-bit or dual 8-bit operating modes. The single 16-bit mode will produce a square-wave output in the continuous timer mode and will produce a single pulse in the single-shot timer mode. The dual 8-bit mode will produce a variable duty cycle pulse in both the continuous and single shot timer modes. One bit of each control register (CRX_7) is used to enable the corresponding output. If this bit is cleared, the output will remain LOW (V_{OL}) regardless of the operating mode.

The continuous and single-shot timer modes are the only ones for which output response is defined. Signals appear at the outputs (unless CRX_7 = "0") during frequency and pulse width comparison modes, but the actual waveform is not predictable in typical applications.

Timer Operating Modes

The F6840 has been designed to operate effectively in a wide variety of applications. This is accomplished by using three bits of each control register (CRX_3, CRX_4 and CRX_5) to define different operating modes of the timers. These modes are outlined in *Table 4*.

Table 4 Operating Modes

Control Register			
CRX_3	CRX_4	CRX_5	Timer Operating Mode
0	*	0	Continuous
0	*	1	Single-Shot
1	0	*	Frequency Comparison
1	1	*	Pulse Width Comparison

*Defines additional timer functions

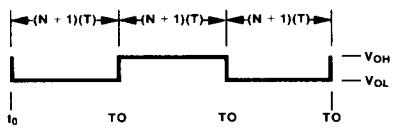
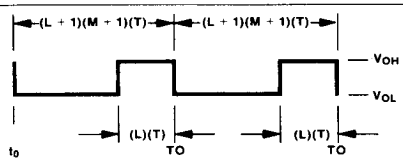
In addition to the four timer modes in *Table 4*, the remaining control register bit is used to modify counter initialization and enabling or interrupt conditions.

Continuous Operating Mode *(Table 5)*
Any of the timers in the PTM may be programmed to operate in a continuous mode by writing "0s" into bits 3 and 5 of the corresponding control register. Assuming that the timer output is enabled (CRX_7 = "1"), either a square wave or a variable duty cycle waveform will be generated at the timer output, OX. The type of output is selected via control register bit 2.

Either a timer reset ($CRX1_0$ = "1" or External $\overline{RESET}$ = "0") condition or internal recognition of a negative transition of the Gate input results in counter initialization. A write timer latches command can be selected as a counter initialization signal by clearing CRX_4.

In the dual 8-bit mode (CRX_2 = "1") [refer to the example in *Figure 1*] the MSB decrements once for every full countdown of the LSB + 1. When the

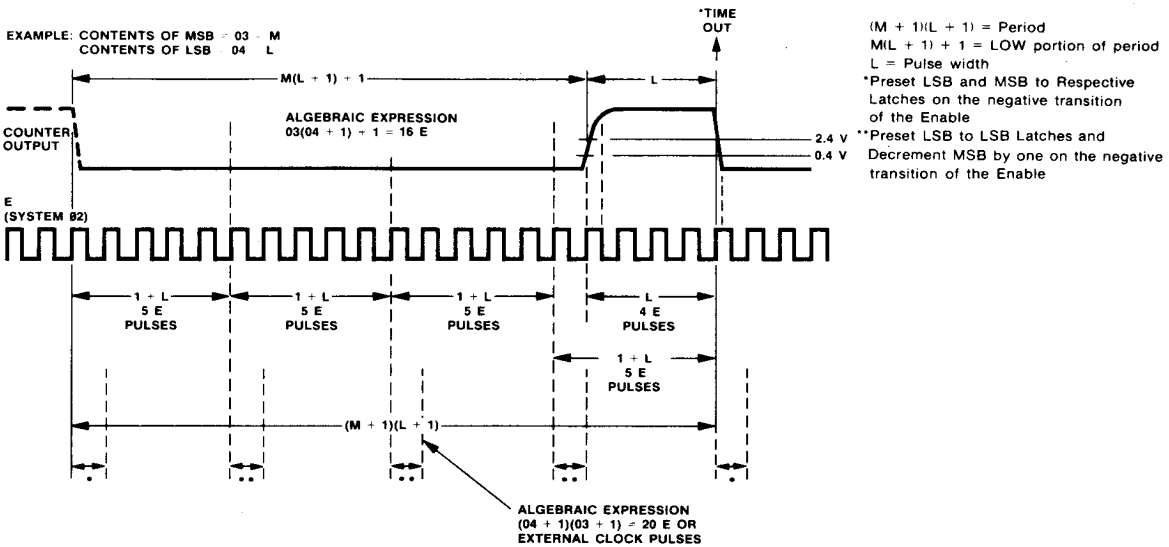
Table 5 Continuous Operating Modes, (CRX_3 = "0", CRX_5 = "0")

Control Register		Initialization/Output Waveforms	
CRX_2	CRX_4	Counter Initialization	*Timer Output (OX) (CRX_7 = "1")
0	0	$\overline{G}\downarrow$ + W + R	
0	1	$\overline{G}\downarrow$ + R	
1	0	$\overline{G}\downarrow$ + W + R	
1	1	$\overline{G}\downarrow$ + R	

$\overline{G}\downarrow$ = Negative transition of Gate input
W = Write Timer Latches Command
R = Timer Reset ($CR1_0$ = "1" or External $\overline{RESET}$ = "0")
N = 16-Bit Number in Counter Latch
L = 8-Bit Number in LSB Counter Latch
M = 8-Bit Number in MSB Counter Latch
T = Clock Input Negative Transitions to Counter
t_0 = Counter Initialization Cycle
TO = Counter Time-Out (All "0" Condition)

*All time intervals shown above assume the Gate ($\overline{G}$) and Clock ($\overline{C}$) signals are synchronized to Enable (System $\phi 2$) with the specified set-up and hold time requirements.

Fig. 1 Timer Output Waveforms Example



LSB = "0", the MSB is unchanged; on the next clock pulse the LSB is reset to the count in the LSB latches and the MSB is decremented by 1 (one). The output, if enabled, remains LOW during and after initialization and will remain LOW until the counter MSB is all "0s". The output will go HIGH at the beginning of the next clock pulse. The output remains HIGH until both the LSB and MSB of the counter are all "0s". At the beginning of the next clock pulse the defined time-out (TO) will occur and the output will go LOW. In the normal 16-bit mode the period of the output of the example in *Figure 1* would span 1546 clock pulses as opposed to the 20 clock pulses using the dual 8-bit mode.

The counter is enabled by an absence of a timer reset condition and a logic "0" at the Gate input. The counter will then decrement on the first clock signal recognized during or after the counter initialization cycle. It continues to decrement on each clock signal so long as $\overline{G}$ remains LOW and no reset condition exists. A counter time-out (the first clock after all counter bits = "0") results in the individual interrupt flag being set and re-initialization of the counter.

A special condition exists for the dual 8-bit mode (CRX_2 = "1") if L = "0". In this case, the counter will revert to a mode similar to the single 16-bit mode, except time-out occurs after M + 1 clock pulses. The output, if enabled, goes LOW during the counter initialization cycle and reverses state at each time-out. The counter remains cyclical (is re-initialized at each time-out) and the individual interrupt flag is set when time-out occurs. If M = L = "0", the internal counters do not change, but the output toggles at a rate of 1/2 the clock frequency.

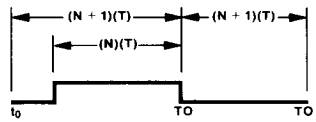
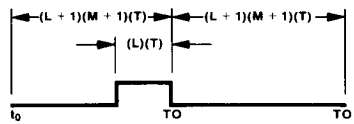
The discussion of the continous mode has assumed that the application requires an output signal. It should be noted that the timer operates in the same manner with the output disabled (CRX_7 = "0"). A read timer counter command is valid regardless of the state of CRX_7.

Single-Shot Timer Mode

This mode is identical to the continuous mode with three exceptions. The first of these is obvious from the name — the output returns to a LOW level after the initial time-out and remains LOW until another counter initialization cycle occurs. The waveforms available are shown in *Table 6*.

As indicated in *Table 6*, the internal counting mechanism remains cyclical in the single-shot mode. Each time-out of the counter results in the setting of an individual interrupt flag and re-initialization of the counter.

Table 6 Single-Shot Operating Modes, (CRX_3 = "0", CRX_7 = "1", CRX_5 = "1")

Control Register		Initialization/Output Waveforms	
CRX_2	CRX_4	Counter Initialization	Timer Output (OX)
0	0	$\overline{G}\downarrow + W + R$	
0	1	$\overline{G}\downarrow + R$	
1	0	$\overline{G}\downarrow + W + R$	
1	1	$\overline{G}\downarrow + R$	

Symbols are as defined in *Table 5*

The second major difference between the single-shot and continuous modes is that the internal counter enable is not dependent on the Gate input level remaining in the LOW state for the single-shot mode.

Another special condition is introduced in the single-shot mode. If L = M = "0" (Dual 8-bit) or N = "0" (Single 16-bit), the output goes LOW on the first clock received during or after counter initialization. The output remains LOW until the operating mode is changed or non-"0" data is written into the counter latches. Time-outs continue to occur at the end of each clock period.

The three differences between single-shot and continuous timer modes can be summarized as attributes of the single-shot mode:

1. Output is enabled for only one pulse until it is reinitialized.
2. Counter Enable is independent of Gate.
3. L = M = "0" or N = "0" disables output.

Aside from these differences, the two modes are identical.

Frequency Comparison or Period Measurement Mode (CRX_3 = "1", CRX_4 = "0")

The frequency comparison mode with CRX_5 = "1" is straightforward. If time-out occurs prior to the first negative transition of the Gate input after a counter initialization cycle, an individual interrupt flag is set. The counter is disabled, and a counter initialization cycle cannot begin until the interrupt flag is cleared and a negative transition on $\overline{G}$ is detected.

Time Interval Modes

The time interval modes are provided for those applications which require more flexibility of interrupt generation and counter initialization. Individual interrupt flags are set in these modes as a function of both counter time-out and transitions of the Gate input. Counter initialization is also affected by interrupt flag status.

The output signal is not defined in any of these modes, but the counter does operate in either single 16-bit or dual 8-bit modes as programmed by CRX_2. Other features of the time interval modes are outlined in *Table 7*.

If CRX_5 = "0", as shown in *Table 7* and *Table 8*, an interrupt is generated if the Gate input returns LOW prior to a time-out. If counter time-out occurs first, the counter is recycled and continues to decrement. A bit is set within the timer on the initial time-out which precludes further individual interrupt generation until a new counter initialization cycle has been completed. When this internal bit is set, a negative transition of the Gate input starts a new counter initialization cycle. (The condition of $\overline{G}\downarrow \cdot \overline{1} \cdot TO$ is satisfied, since a time-out has occurred and no individual interrupt has been generated.)

Any of the timers within the PTM may be programmed to compare the period of a pulse (giving the frequency after calculations) at the Gate input with the time period required for counter time-out. A negative transition of the Gate input enables the counter and starts a counter

Table 7 Timer Interval Modes, CRX_3 = "1"

CRX_4	CRX_5	Application	Condition for Setting Individual Interrupt Flag
0	0	Frequency Comparison	Interrupt Generated if Gate Input Period (1/F) is less than Counter Time-Out (TO)
0	1	Frequency Comparison	Interrupt Generated if Gate Input Period (1/F) is greater than Counter Time-Out (TO)
1	0	Pulse Width Comparison	Interrupt Generated if Gate Input "Down Time" is less than Counter Time-Out (TO)
1	1	Pulse Width Comparison	Interrupt Generated if Gate Input "Down Time" is greater than Counter Time-Out (TO)

Table 8 Frequency Comparison Mode, CRX_3 = "1", CRX_4 = "0"

Control Register Bit 5 (CRX_5)	Counter Initialization	Counter Enable Flip-Flop Set (CE)	Counter Enable Flip-Flop Reset (CE)	Interrupt Flag Set (1)
0	$\overline{G}\downarrow \cdot \overline{I} \cdot (\overline{CE} + TO \cdot CE) + R$	$\overline{G}\downarrow \cdot \overline{W} \cdot \overline{R} \cdot \overline{I}$	$W + R + I$	$\overline{G}\downarrow$ Before TO
1	$\overline{G}\downarrow \cdot \overline{I} + R$	$\overline{G}\downarrow \cdot \overline{W} \cdot \overline{R} \cdot \overline{I}$	$W + R + I$	TO Before $G\downarrow$

$\overline{I}$ represents the interrupt for a given timer.

Table 9 Pulse Width Comparison Mode, CRX_3 = "1", CRX_4 = "1"

Control Register Bit 5 (CRX_5)	Counter Initialization	Counter Enable Flip-Flop Set (CE)	Counter Enable Flip-Flop Reset (CE)	Interrupt Flag Set (I)
0	$\overline{G}\downarrow \cdot \overline{I} + R$	$\overline{G}\downarrow \cdot \overline{W} \cdot \overline{R} \cdot \overline{I}$	$W + R + I + G$	$\overline{G}\uparrow$ Before TO
1	$\overline{G}\downarrow \cdot \overline{I} + R$	$\overline{G}\downarrow \cdot \overline{W} \cdot \overline{R} \cdot \overline{I}$	$W + R + I + G$	TO Before $\overline{G}\uparrow$

G = Level sensitive recognition of Gate Input

initialization cycle — provided that other conditions as noted in *Table 8* are satisfied. The counter decrements on each clock signal recognized during or after counter initialization until an interrupt is generated, a write timer latches command is issued, or a Timer Reset condition occurs. It can be seen from *Table 8* that an interrupt condition will be generated if CRX_5 = "0" and the period of the pulse (single pulse or separately measured repetitive pulses) at the Gate input is less than the counter time-out period. If CRX_5 = "1", an interrupt is generated if the reverse is true.

Assume now with CRX_5 = "1" that a counter initialization has occurred and that the Gate input has returned LOW prior to counter time out. Since there is no individual interrupt flag generated, this automatically starts a new counter initialization cycle. The process will continue with frequency comparison being performed on each Gate input cycle until the mode is changed, or a cycle is determined to be above the predetermined limit.

Pulse Width Comparison Mode (CRX_3 = "1", CRX_4 = "1")

This mode is similar to the frequency comparison mode except that a positive, rather than negative, transition of the Gate input terminates the count. With CRX_5 = "0", an individual interrupt flag will be generated if the "0" level pulse applied to the Gate input is less than the time period required for counter time-out. With CRX_5 = "1", the interrupt is generated when the reverse condition is true.

As can be seen in *Table 9*, a positive transition of the Gate input disables the counter. With CRX_5 = "0", it is therefore possible to obtain directly the width of any pulse causing an interrupt. Similar data for other time interval modes and conditions can be obtained, if two sections of the PTM are dedicated to the purpose.

Absolute Maximum Ratings

Supply Voltage	-0.3 V, +7.0 V
Input Voltage	-0.3 V, +7.0 V
Operating Temperature Range — T_L to T_H	
F6840P,S/F68A40P,S/F68B40P,S	0° C, +70° C
F6840CP,CS/F68A40CP,CS	-40° C, +85° C
F6840DL	-55° C, +85° C
F6840DM	-55° C, +125° C
Storage Temperature Range	-55° C, +150° C
Thermal Resistance	
Plastic Package	115° C/W
Ceramic Package	60° C/W

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics V_{CC} = 5.0 V ±5%, V_{SS} = 0, $T_A = T_L$ to T_H, unless otherwise noted.

Symbol	Characteristic	Signal	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input HIGH Voltage		2.0			V	
V_{IL}	Input LOW Voltage		-0.4		0.8	V	
I_{IN}	Input Leakage Current			1.0	2.5	μA	V_{IN} = 0 to 5.25 V
I_{TSI}	3-State (OFF State) Input Current	D_0-D_7		2.0	10	μA	V_{IN} = 0.4 to 2.4 V
V_{OH}	Output HIGH Voltage	D_0-D_7 Other Outputs	2.4 2.4			V	I_{Load} = -205 μA, I_{Load} = 200 μA
V_{OL}	Output LOW Voltage	D_0-D_7 O_1-O_3, $\overline{IRQ}$			0.4 0.4	V	I_{Load} = 1.6 mA, I_{Load} = 3.2 mA
I_{LOH}	Output Leakage Current (OFF State)	($\overline{IRQ}$)		1.0	10	μA	V_{OH} = 2.4 V
P_D	Power Dissipation			470	700	mW	
C_{IN}	Input Capacitance	 D_0-D_7 All Other Inputs			 12.5 7.5	 pF	V_{IN} = 0, T_A = 25°C, f = 1.0 MHz
C_{OUT}	Output Capacitance	O_1, O_2, O_3 $\overline{IRQ}$			10 5.0	 pF	V_{IN} = 0, T_A = 25°C, f = 1.0 MHz

Bus Timing Characteristics
Read *(Figure 2)*

Symbol	Characteristic	F6840 Min	F6840 Max	F68A40 Min	F68A40 Max	F68B40 Min	F68B40 Max	Unit
$t_{cyc}E$	Enable Cycle Time	1.0	10	0.666	10	0.5	10	μs
PW_{EH}	Enable Pulse Width, HIGH	0.45	4.5	0.280	4.5	0.22	4.5	μs
PW_{EL}	Enable Pulse Width, LOW	0.43		0.280		0.21		μs
t_{AS}	Set-up Time, Address and R/$\overline{W}$ valid to enable positive transition	160		140		70		ns
t_{DDR}	Data Delay Time		320		220		180	ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input		25		25		25	ns

Write *(Figure 3)*

$t_{cyc}E$	Enable Cycle Time	1.0	10	0.666	10	0.50	10	μs
PW_{EH}	Enable Pulse Width, HIGH	0.45	4.5	0.280	4.5	0.22	4.5	μs
PW_{EL}	Enable Pulse Width, LOW	0.43		0.280		0.21		μs
t_{AS}	Set-up Time, Address and R/$\overline{W}$ valid to enable positive transition	160		140		70		ns
t_{DSW}	Data Set-up Time	195		80		60		ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input		25		25		25	ns

Fig. 2 Bus Read Timing Characteristics
(Read Information from PTM)

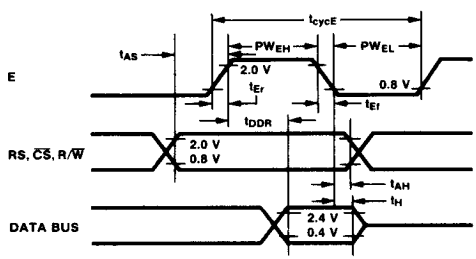
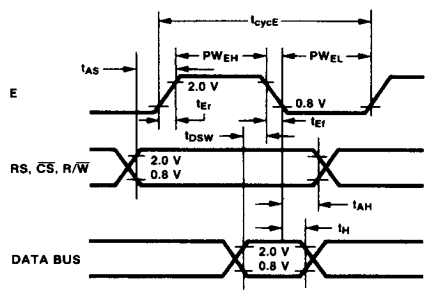


Fig. 3 Bus Write Timing Characteristics
(Write Information into PTM)



AC Characteristics *(Figures 4-8)*

Symbol	Characteristic		F6840 Min	F6840 Max	F68A40 Min	F68A40 Max	F68B40 Min	F68B40 Max	Unit
t_r, t_f	Input Rise and Fall Times	$\overline{C}$,$\overline{G}$ and $\overline{RESET}$		1.0*		0.666*		0.500*	μs
PW_L	Input Pulse Width LOW	$\overline{C}$,$\overline{G}$ and $\overline{RESET}$	$t_{cyc}E$ $+t_{su}$ $+t_{hd}$		$t_{cyc}E$ $+t_{su}$ $+t_{hd}$		$t_{cyc}E$ $+t_{su}$ $+t_{hd}$		ns
PW_H	Input Pulse Width HIGH	$\overline{C}$,$\overline{G}$	$t_{cyc}E$ $+t_{su}$ $+t_{hd}$		$t_{cyc}E$ $+t_{su}$ $+t_{hd}$		$t_{cyc}E$ $+t_{su}$ $+t_{hd}$		ns
t_{su}	Input Set-up Time (Synchronous Mode)	$\overline{C}$,$\overline{G}$ and $\overline{RESET}$ $\overline{C3}$ (÷8 Prescaler Mode only)	200		120		75		ns
t_{hd}	Input Hold Time (Synchronous Mode)	$\overline{C}$,$\overline{G}$ and $\overline{RESET}$ $\overline{C3}$ (÷8 Prescaler Mode only)	50		50		50		ns
	Output Delay, 01-03								
t_{co}	(V_{OH} = 2.4 V, Load B)	TTL		700		460		340	ns
t_{cm}	(V_{OH} = 2.4 V, Load D)	MOS		450		450		340	ns
t_{cmos}	(V_{OH} = 0.7 V_{DD}, Load D)	CMOS		2.0		1.35		1.0	μs
t_{IR}	Interrupt Release Time			1.2		0.9		0.7	μs

*t_r and $t_f \leq 1 \times$ Pulse Width or 1.0 μs, whichever is smaller.

Fig. 4 Input Pulse Width Low

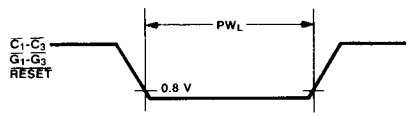


Fig. 5 Input Pulse Width High

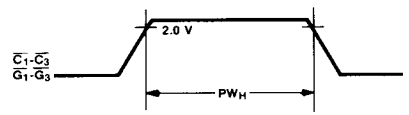


Fig. 6 Input Set-up and Hold Times

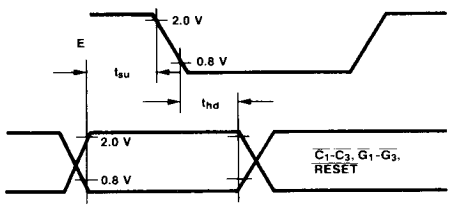


Fig. 7 Output Delay

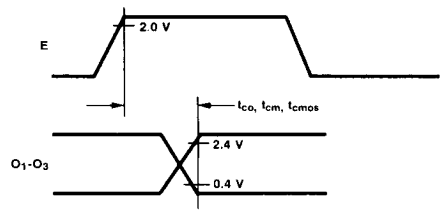


Fig. 8 $\overline{IRQ}$ Release Time

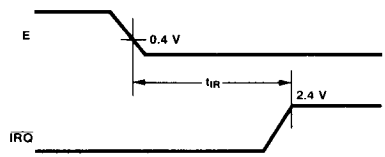
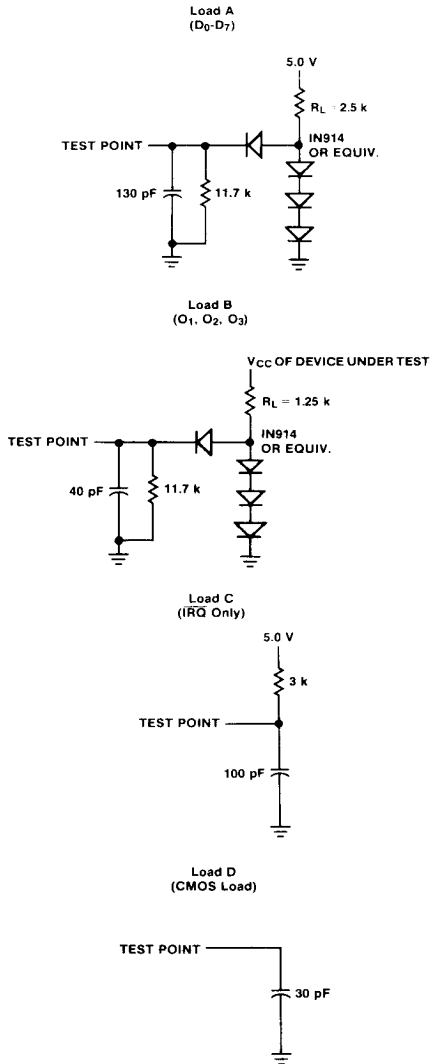


Fig. 9 Bus Timing Test Loads



Ordering Information

Speed	Order Code	Temperature Range
1.0 MHz	F6840P,S	0° C to +70° C
	F6840CP,CS	-40° C to +85° C
	F6840DL	-55° C to +85° C
	F6840DM	-55° C to +125° C
1.5 MHz	F68A40P,S	0° C to +70° C
2.0 MHz	F68B40P,S	0° C to +70° C

P = Plastic package, S = Ceramic package

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