Integrated Device Technology, Inc.

CMOS STATIC RAMS 256K (64K x 4-BIT)

Separate Data Inputs and Outputs

PRELIMINARY
IDT 71281S/L
IDT 71282S/L

FEATURES:

- Separate data inputs and outputs
- IDT71281S/L: outputs track inputs during write mode
- IDT71282S/L: high impedance outputs during write mode
- High speed (equal access and cycle time)
  - Military: 25/35/45/55/70ns (max.)
  - Commercial: 20/25/35/45/55ns (max.)
- Low power consumption
  - IDT71281/2S
    Active: 400mW (typ.)
    Standby: 400µw (typ.)
  - IDT71281/2L
    Active: 350mW (typ.)
    Standby: 100µw (typ.)
- Battery backup operation – 2V data retention (L version only)
- High-density 28-pin DIP, and 28-pin SOIC
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71281/IDT71282 are 262,144-bit high-speed static RAMs organized as 64K x 4. They are fabricated using IDT's high-performance, high-reliability technology – CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

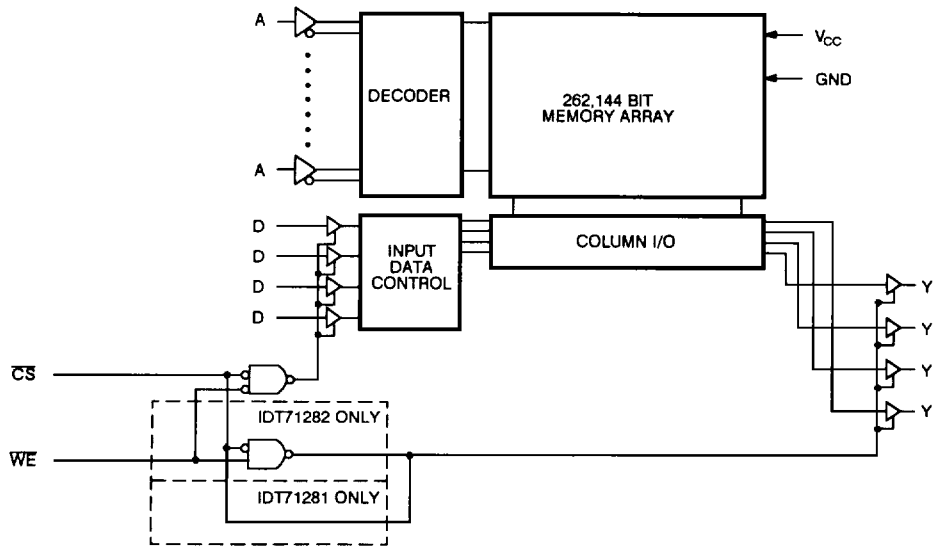
Access times as fast as 25ns are available with typical power consumption of only 350mW. These circuits also offer a reduced power standby mode (I_{SB}). When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, this standby mode. The ultra-low-power standby mode capability provides significant system-level power and cooling savings. The low-power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 100µW operating off a 2V battery.

All inputs and outputs of the IDT71281/IDT71282 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT71281/IDT71282 are packaged in 28-pin sidebraze and plastic DIPs, and SOICs providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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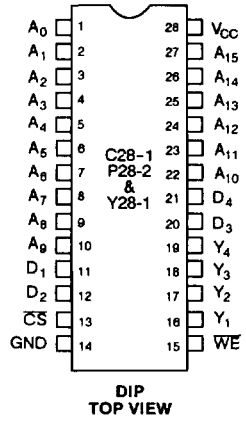
PIN CONFIGURATIONS

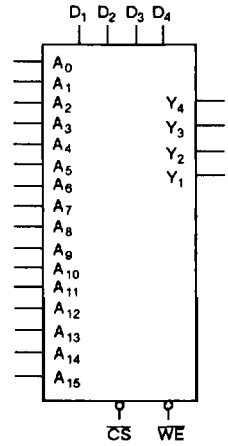


DIP
TOP VIEW

PIN NAMES

A_0-A_{15}	Address Inputs	D_1-D_4	$DATA_{IN}$
$\overline{CS}$	Chip Select	Y_1-Y_4	$DATA_{OUT}$
$\overline{WE}$	Write Enable	GND	Ground
V_{CC}	Power		

LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS (for all speeds)

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT71281/2S MIN.	IDT71281/2S TYP.(1)	IDT71281/2S MAX.	IDT71281/2L MIN.	IDT71281/2L TYP.(1)	IDT71281/2L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	POWER	FUNCTION	71281/2S20 71281/2L20		71281/2S25(2) 71281/2L25(2)		71281/2S35 71281/2L35		71281/2S45 71281/2L45		71281/2S55 71281/2L55		71281/2S70 71281/2L70		UNIT
				COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(2)	S	READ	70	–	60	70	50	60	50	60	50	60	–	60	mA
			WRITE(4)	140	–	130	140	120	130	120	130	120	130	–	130	
		L	READ	50	–	40	50	30	40	30	40	30	40	–	40	
			WRITE(4)	130	–	120	130	110	120	110	120	110	120	–	120	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	S	READ	170	–	160	170	150	160	150	160	150	160	–	160	mA
			WRITE(4)	180	–	170	180	160	170	160	170	160	170	–	170	
		L	READ	150	–	140	150	130	140	130	140	130	140	–	140	
			WRITE(4)	160	–	150	160	140	150	140	150	140	150	–	150	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH} V_{CC} = Max., Outputs Open f = f_{MAX}(2)	S		35	–	35	35	35	35	35	35	35	35	–	35	mA
		L		20	–	20	20	20	20	20	20	20	20	–	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC} V_{CC} = Max., f = 0(2)	S		30	–	30	35	30	35	30	35	30	35	–	35	mA
		L		1.5	–	1.5	4.5	1.5	4.5	1.5	4.5	1.5	4.5	–	4.5	

NOTES:

1. All values are maximum guaranteed values.
2. Preliminary data for military devices only.
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
4. Write cycle current specifications are included to aid in the design of extremely sensitve applications. It should be noted that, in most systems, the ratio of read cycles to write cycles is extremely high. When calculating total current consumption, the designer should weight these figures by the percentage of "On" time as well as the anticipated ratio of read to write cycles (usually greater than 90%).

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

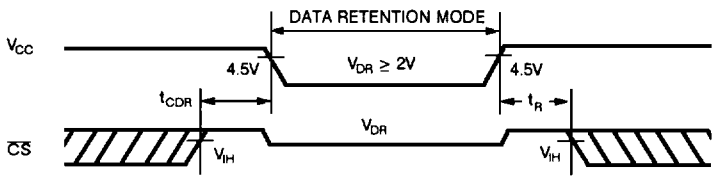
SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	MIL.	–	50	75	2000	3000	µA
			COM'L.	–	50	75	500	750	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:

1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

4

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

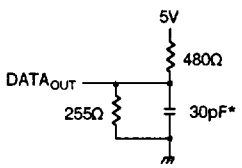


Figure 1. Output Load

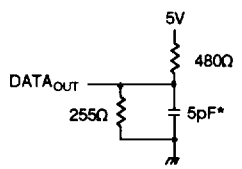


Figure 2. Output Load (for t_{CLZ}, t_{CHZ}, t_{OW} and t_{WHZ})

* Including scope and jig.

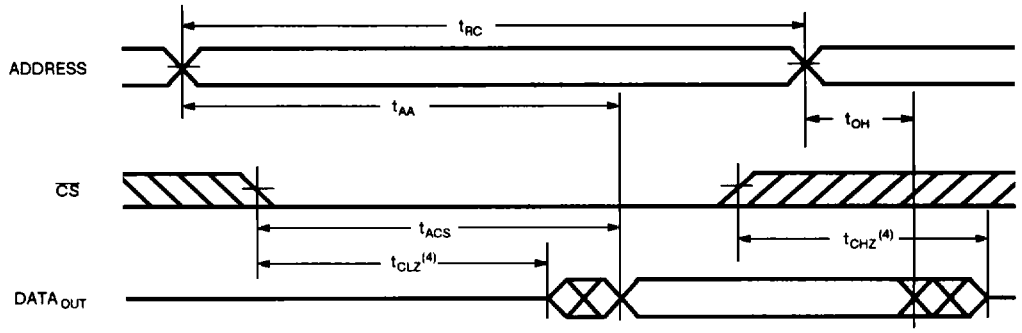
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	71281/2S20[1] 71281/2L20[1] MIN.	MAX.	71281/2S25[5] 71281/2L25[5] MIN.	MAX.	71281/2S35 71281/2L35 MIN.	MAX.	71281/2S45 71281/2L45 MIN.	MAX.	71281/2S55 71281/2L55 MIN.	MAX.	71281/2S70[2] 71281/2L70[2] MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	20	–	25	–	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	35	–	45	–	55	–	70	ns
t_{ACS}	Chip Select Access Time[3]	–	20	–	25	–	35	–	45	–	55	–	70	ns
t_{CLZ}	Chip Select to Output in Low Z[4]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Select to Output in High Z[4]	–	10	–	13	–	15	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time[4]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[4]	–	20	–	25	–	35	–	45	–	55	–	70	ns

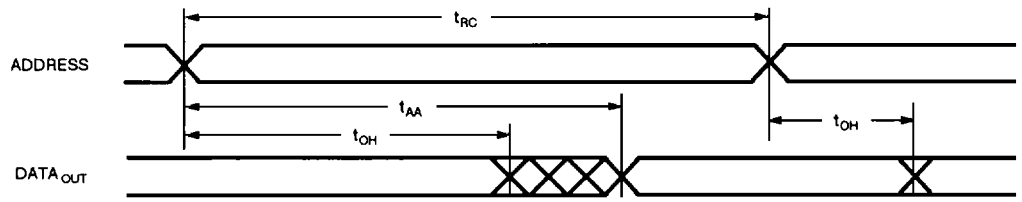
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.
5. Preliminary data for military devices only.

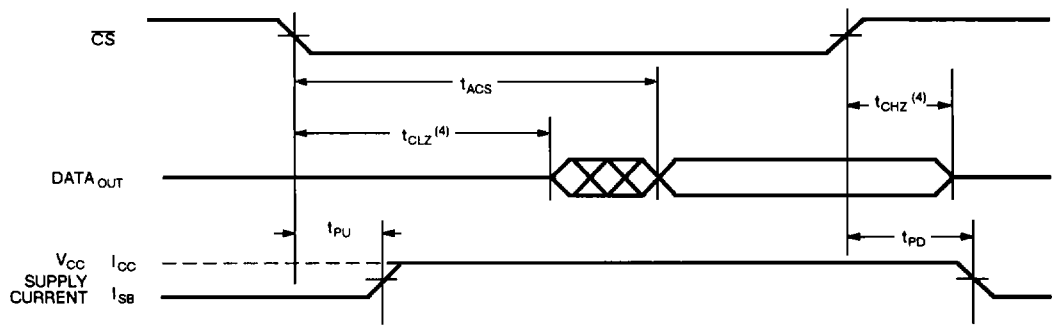
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2]



TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3]



NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state.

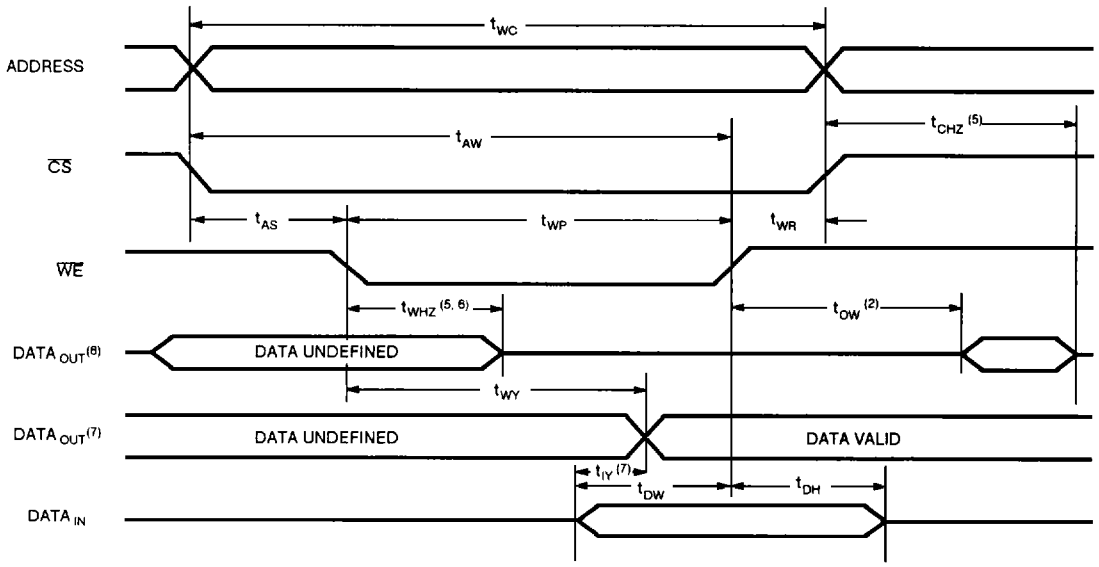
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	71281/2S20[1] 71281/2L20[1] MIN.	MAX.	71281/2S25[7] 71281/2L25[7] MIN.	MAX.	71281/2S35 71281/2L35 MIN.	MAX.	71281/2S45 71281/2L45 MIN.	MAX.	71281/2S55 71281/2L55 MIN.	MAX.	71281/2S70[2] 71281/2L70[2] MIN.	MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{CW}	Chip Select to End of Write [3]	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output in High Z [4, 6]	–	13	–	13	–	15	–	20	–	25	–	30	ns
t_{DW}	Data Valid to End of Write	15	–	15	–	20	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write [4, 6]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{IY}	Data Valid to Output Valid [4, 5]	–	20	–	20	–	30	–	35	–	40	–	45	ns
t_{WY}	Write Enable to Output Valid [4, 5]	–	20	–	20	–	30	–	35	–	40	–	45	ns

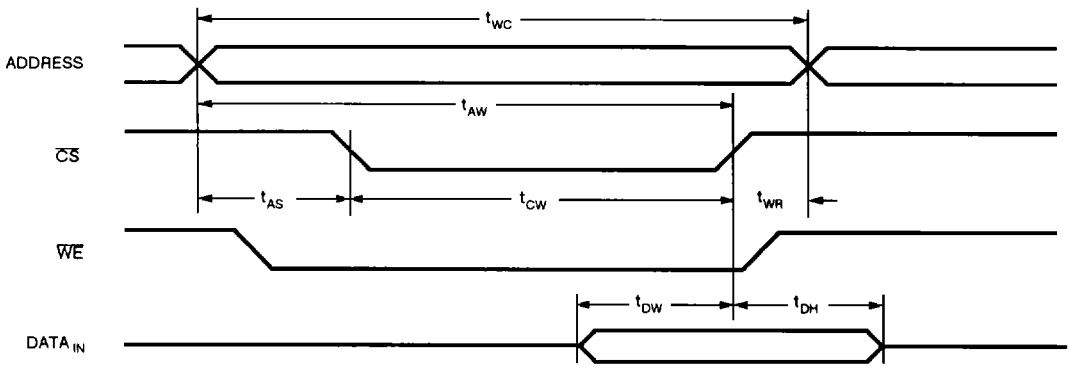
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.
5. For IDT71281S/L only.
6. For IDT71282S/L only.
7. Preliminary data for military devices only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3]



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 4]



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$, and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state (IDT71282 only).
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
6. IDT71282 only.
7. IDT71281 only.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write (1)	L	L	D_{IN}	Active
Write (2)	L	L	High Z	Active

NOTES:
1. For IDT71281 only.
2. For IDT71282 only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

ORDERING INFORMATION