NEC
NEC Electronics Inc.

μPD4265
65,536 x 1-BIT
DYNAMIC CMOS RAM

Revision 1

Description

The NEC μPD4265 is a 65,536-word by 1-bit dynamic CMOS Random Access Memory (RAM) designed to operate from a single +5 V power supply. The negative voltage substrate bias is generated internally providing automatic and transparent operation.
The unique construction of the μPD4265 allows for an extremely low standby power device that incorporates three user-selected, self-refresh standby modes. The device can accomplish $\overline{RAS}$-only refresh. Also, by utilizing the pin 1 refresh function, it can perform automatic pulsed refresh or hidden auto pulsed refresh which makes use of the internal refresh address generator.

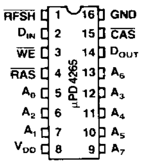
Features

- ☐ 65,536-word x 1-bit organization
- ☐ High memory density: 16-pin plastic DIP
- ☐ Single +5V ± 10% power supply
- ☐ Control on pin 1 for automatic and self refresh
- ☐ Multiplexed address inputs
- ☐ Fully TTL-compatible including clocks
- ☐ Three-state output
- ☐ Read, write, RMW, $\overline{RAS}$-only refresh, page mode, latched pulse, pulse and self-refresh capabilities
- ☐ $\overline{CAS}$-controlled output allows hidden refresh
- ☐ 2 performance ranges:

Device	t_{RAC}	t_{CAC}	t_{RC}	Power
μPD4265C-20	200ns	100ns	335ns	193mW
μPD4265C-25	250ns	125ns	410ns	165mW

- ☐ Cycle time: R/W, 335ns min
- ☐ Low power dissipation
  - – 35mA max (operating)
  - – 1.0mA max (standby, $\overline{RAS} = \overline{CAS} = V_{IH}$)
  - – 0.5mA max (standby, $\overline{RAS} = \overline{CAS} = V_{DD}$)
  - – 200μA max (self-refresh 1, T_A = 0°C to +70°C)
  - – 100μA max (self-refresh 2, T_A = 0°C to +45°C)
  - – 50μA max (self-refresh 3, T_A = 0°C to +25°C)
  (According to Figure 1.)
- ☐ 128 refresh cycles

Pin Configuration



Pin Identification

Pin No.	Pin Symbol	Function
1	$\overline{RFSH}$	Refresh
2	D_{IN}	Data-in
3	$\overline{WE}$	Write Enable
4	$\overline{RAS}$	Row Address Strobe
5–7, 9–13	$A_0 - A_7$	Address Inputs
5–7, 10–13	$A_0 - A_6$	Refresh Addresses
8	V_{DD}	+5V Power Supply
14	D_{OUT}	Data-out
15	$\overline{CAS}$	Column Address Strobe
16	GND	Ground

Absolute Maximum Ratings*

Voltage on any Pin Relative to Ground, $V_{I/O}$	−1.0V to +7.0V
Operating Temperature, T_{OPT} (Ambient)	0°C to +70°C
Storage Temperature, T_{STG} (Ambient)	−55°C to +125°C
Short-circuit Output Current, I_{OS}	50mA
Power Dissipation, P_D	1W

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C; f = 1MHz

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Address, Data-in	C_{I1}			5	pF	
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{RFSH}$	C_{I2}			8	pF	
Output	C_O			7	pF	

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DC Characteristics

T_A = 0°C to +70°C; V_{DD} = 5V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	All Voltages Referenced to Ground
High-level Input Voltage	V_{IH}	2.4		5.5	V	
Low-level Input Voltage	V_{IL}	−1.0		0.8	V	
V_{DD} Supply Current Standby	I_{DD2}			1.0	mA	$\overline{RAS} = \overline{CAS} = V_{IH}$
Standby (Output-enable)	I_{DD5}			1.0	mA	$\overline{RAS} = V_{IH}$
Standby	I_{DD6}			0.5	mA	$\overline{RAS} = \overline{CAS} = V_{DD}$
Self-refresh 1 (T_A = 0°C to +70°C)	I_{DD8}			200	μA	$\overline{RAS} = \overline{CAS} = V_{IH}$; $\overline{WE} = V_{IH}$
Self-refresh 2 (T_A = 0°C to +45°C)	I_{DD9}			100	μA	$\overline{RAS} = \overline{CAS} = V_{IH}$; $\overline{WE} = V_{IL}$
Self-refresh 3	I_{DD10}			①		$\overline{CAS}$ = GND; $\overline{RAS} = V_{IH}$; $\overline{WE} = V_{DD}$/GND
Input Leakage Current	$I_{I(L)}$	−10		10	μA	
Output Leakage Current	$I_{O(L)}$	−10		10	μA	
Output Low Voltage	V_{OL}	0		0.4	V	I_{OL} = 4.2mA
Output High Voltage	V_{OH}	2.4		V_{DD}		I_{OH} = −5mA

Note: ① According to Figure 1.

AC Characteristics

T_A = 0°C to +70°C; V_{DD} = 5V ± 10%

Read, Write, RMW, $\overline{RAS}$-only Refresh Cycles

Parameter	Symbol	4265-20 Min	4265-20 Max	4265-25 Min	4265-25 Max	Unit	Test Conditions
V_{DD} Operating Current	I_{DD1}		35		30	mA	
V_{DD} RAS-only Refresh Current	I_{DD3}		30		25	mA	
V_{DD} Page Current	I_{DD4}		20		17	mA	
Random Read or Write Cycle Time	t_{RC}	335		410		ns	
Read, Write Cycle Time	t_{RWC}	370		465		ns	
Access Time from $\overline{RAS}$	t_{RAC}		200		250	ns	
Access Time from $\overline{CAS}$	t_{CAC}		100		125	ns	
Output Buffer Turn-off Delay	t_{OFF}	0	50	0	60	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	60	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	120		150		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	200	10000	250	10000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	100		125		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	100	10000	125	10000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	200		250		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	30	100	35	125	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	0		0		ns	
CAS Precharge Time, (Nonpage Cycles)	t_{CPN}	30		35		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	0		0		ns	
Row Address Set-up Time	t_{ASR}	0		0		ns	
Row Address Hold Time	t_{RAH}	20		25		ns	
Column Address Set-up Time	t_{ASC}	0		0		ns	
Column Address Hold Time	t_{CAH}	55		65		ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	155		190		ns	
Read Command Set-up Time	t_{RCS}	0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	25		30		ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	
Write Command Hold Time	t_{WCH}	55		65		ns	

AC Characteristics (Cont.)

T_A = 0°C to +70°C; V_{DD} = 5V ± 10%

Read, Write, RMW, $\overline{RAS}$-only Refresh Cycles

Parameter	Symbol	4265-20 Min	4265-20 Max	4265-25 Min	4265-25 Max	Unit	Test Conditions
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	155		190		ns	
Write Command Pulse Width	t_{WP}	55		65		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	55		65		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	55		65		ns	
Data-in Set-up Time	t_{DS}	0		0		ns	
Data-in Hold Time	t_{DH}	55		65		ns	
Data-in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	155		190		ns	
Refresh Period	t_{REF}		2		2	ns	
$\overline{WE}$ Command Set-up Time	t_{WCS}	−10		−10		ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	80		100		ns	
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	180		235		ns	

Page Mode Cycle

Parameter	Symbol	4265-20 Min	4265-20 Max	4265-25 Min	4265-25 Max	Unit	Test Conditions
Read or Write Cycle Time	t_{PC}	190		260		ns	
Read Modify Write Cycle Time	t_{CPM}	230		280		ns	
$\overline{CAS}$ Precharge Time	t_{CP}	80		100		ns	
$\overline{RAS}$ Pulse Width	t_{RPM}	200	10000	250	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	100	10000	125	10000	ns	

Pulse Refresh Cycle (Latched Pulse Refresh)

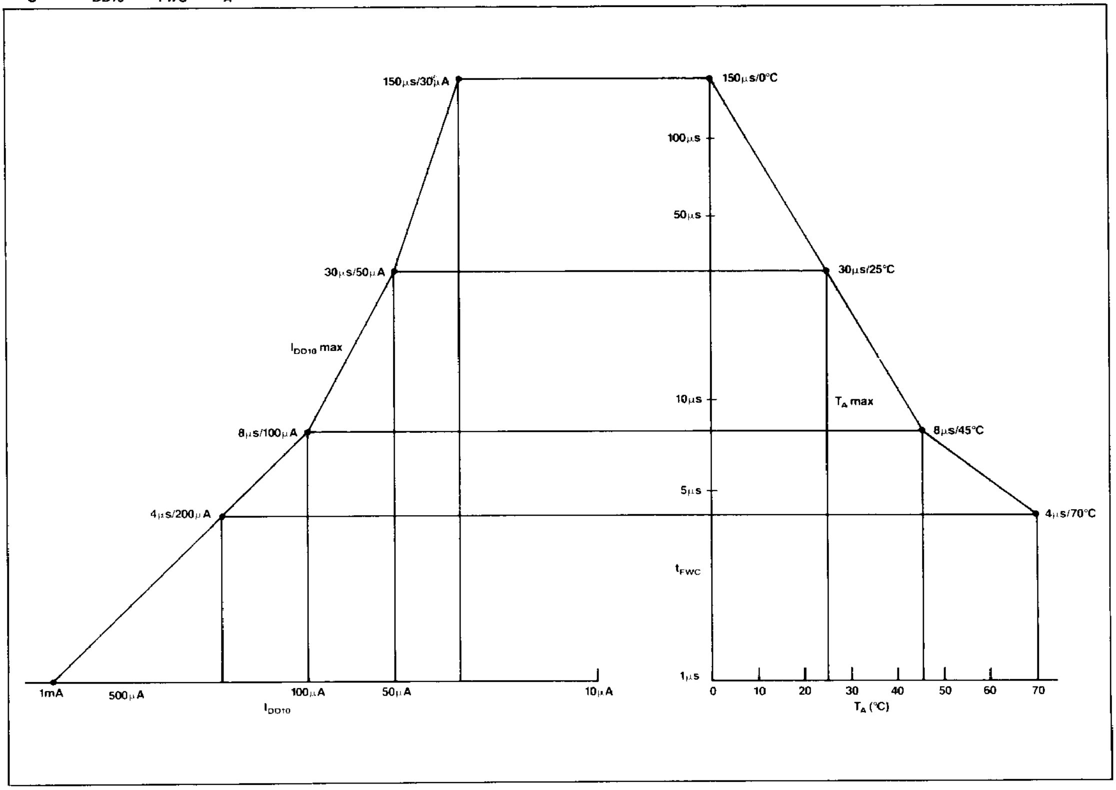
Parameter	Symbol	4265-20 Min	4265-20 Max	4265-25 Min	4265-25 Max	Unit	Test Conditions
V_{DD} Pulse Refresh Current	I_{DD7}		25		20	mA	
Pulse Refresh Cycle Time	t_{FC}	335		410		ns	
$\overline{RAS}$ to $\overline{RFSH}$ Delay	t_{RFD}	120		150		ns	
$\overline{RFSH}$ Pulse Width	t_{FAS}	80	1000	80	1000	ns	
$\overline{RFSH}$ Precharge Time	t_{FP}	120		120		ns	
$\overline{RFSH}$ to $\overline{RAS}$ Delay	t_{FSR}	30		30		ns	
$\overline{RFSH}$ before $\overline{RAS}$ Set-up Time	t_{FBR}	365		445		ns	
$\overline{RAS}$ to $\overline{RFSH}$ Delay (Latched Pulse)	t_{FRD}	80		80		ns	
$\overline{RAS}$ to $\overline{RFSH}$ Set-up (Latched Pulse)	t_{RFS}	455		560		ns	

Self-refresh Cycle

Parameter	Symbol	4265-20 Min	4265-20 Max	4265-25 Min	4265-25 Max	Unit	Test Conditions
$\overline{RAS}$ to $\overline{RFSH}$ Delay	t_{RFD}	120		150		ns	
$\overline{RFSH}$ Pulse Width	t_{FAS}	8000		8000		ns	
$\overline{RFSH}$ to $\overline{RAS}$ Delay	t_{FRS}	365		445		ns	
$\overline{RAS}$ Hold Time	t_{FRH}	8000		8000		ns	
$\overline{RAS}$ to $\overline{RFSH}$ Set-up Time	t_{RSF}	0		0		ns	
$\overline{RFSH}$ to $\overline{CAS}$ Delay	t_{FCD}	0	1000	0	1000	ns	
$\overline{RFSH}$ to $\overline{WE}$ Delay	t_{FWD}	0	1000	0	1000	ns	
$\overline{RFSH}$ to $\overline{CAS}$ Set-up Time	t_{FCS}	0		0		ns	
$\overline{RFSH}$ to $\overline{WE}$ Set-up Time	t_{FWS}	0		0		ns	
$\overline{CAS}$ to $\overline{WE}$ Set-up Time	t_{FWCS}	0		0		ns	
$\overline{WE}$ Pulse Width	t_{FWP}	1		1		μs	
$\overline{WE}$ Pulse Cycle Time	t_{FWC}		①		①	μs	

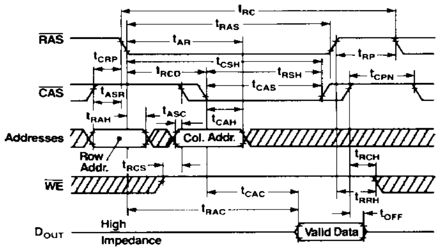
Note: ① According to Figure 1.

Figure 1. I_{DD10} vs. t_{FWC} vs. T_A

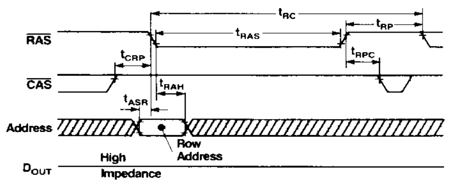


Timing Waveforms

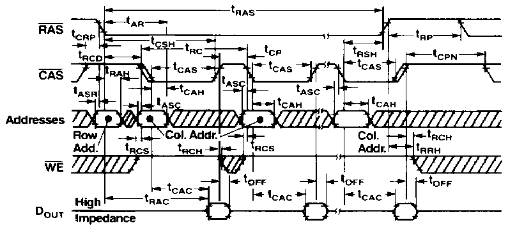
Read Cycle



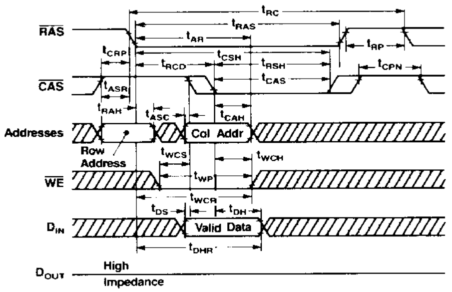
$\overline{RAS}$-only Refresh Cycle



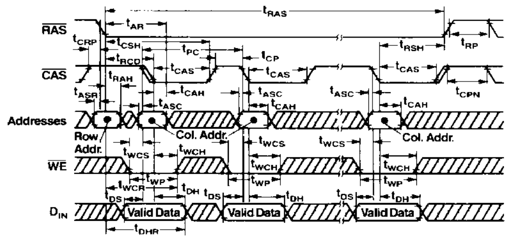
Page Mode Read Cycle



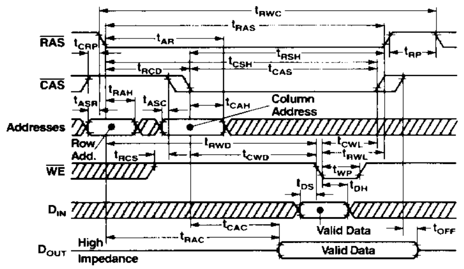
Write Cycle (Early Write)



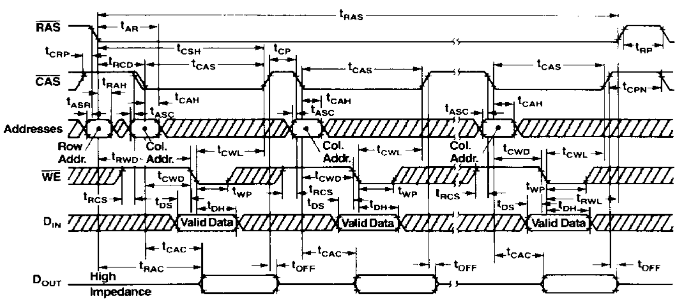
Page Mode Write Cycle (Early Write)



Read-Write/Read-Modify-Write Cycles

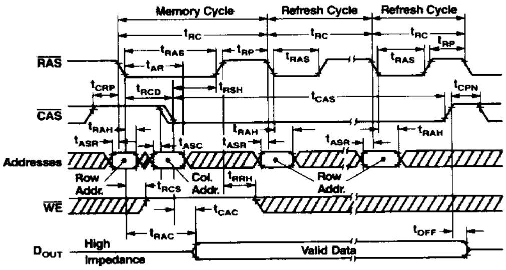


Page Mode Read-Write/Read-Modify-Write Cycles

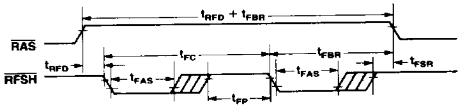


Timing Waveforms (Cont.)

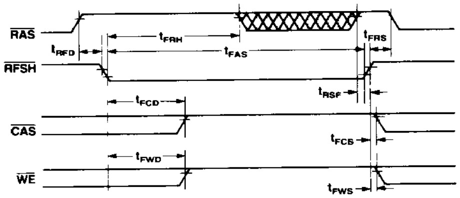
Hidden Refresh Cycle



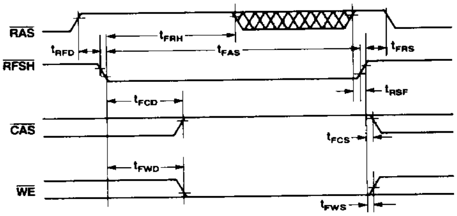
Pulse Refresh Cycle



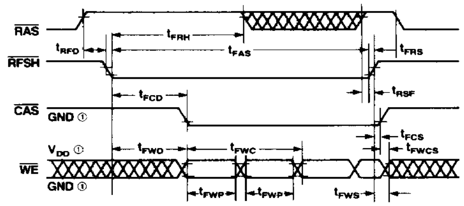
Self-refresh Cycle 1



Self-refresh Cycle 2

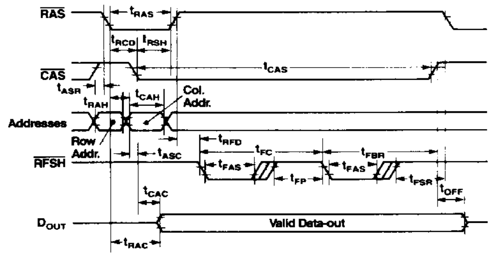


Self-refresh Cycle 3

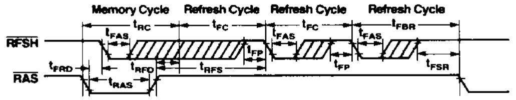


Note: ① Needs CMOS level.

Hidden Automatic Pulse Refresh Cycle



Latched Pulse Refresh Cycle



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