FUJITSU

CMOS 1,048,576 BIT UV ERASABLE READ ONLY MEMORY (EPROM)

MBM27C1001-15
MBM27C1001-20
MBM27C1001-25

April 1988
Edition 2.0

CMOS 1,048,576 BIT UV ERASABLE READ ONLY MEMORY (EPROM)

The Fujitsu MBM27C1001 EPROM is a high speed read-only static memory that is UV-erasable and reprogrammable. The device contains 1,048,576 programmable or reprogrammable bits organized in a 131,072-byte/8-bit format. The MBM27C1001 is housed in a 32-pin DIP and 36-pad LCC with a transparent lid; when the lid is properly exposed to an ultraviolet light source, a previously programmed bit pattern is erased in approximately 15-to-21 minutes. A new bit pattern can then be written into memory.

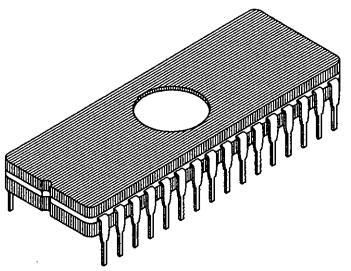
The MBM27C1001 EPROM is fabricated using CMOS double poly-silicon gate technology with stacked single-transistor gate cells. The MBM27C1001 is an excellent choice for system development work and in other applications where program changes are frequently necessary. Once programmed, the device requires only a single +5V power supply; the current requirements are exceptionally low in both the active and standby modes of operation.

- 131,072-byte/8-bit organization with on-chip decoding
- Single-byte or four-byte programming capability with Quick Pro™ algorithm
- Static operation (no clocks required)
- Upward compatible with 256K/512K EPROMS
- Fast access time:
  MBM27C1001-15 = 150 ns (max)
  MBM27C1001-20 = 200 ns (max)
  MBM27C1001-25 = 250 nx (max)
- Easy and simple memory expansion via @pin
- Three-state output for wired-OR capability
- TTL-compatible inputs/outputs
- Single =5V (+10%) power supply with low current drain:
  Active operation = 30 mA (max) for 200ns/250ns
  40 mA (max) for 150ns
  Standby operation = 0.1 mA (max)
- Programming voltage: +12.5V
- JEDEC-approved pin assignments
- 32-pin CERDIP

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage with respect to ground	V_{CC}	-0.6 to + 7.0	V
Programming Voltage with respect to ground	V_{PP}	-0.6 to + 14.0	V
Input/Output Voltage (except for A_9 with respect to ground)	V_{IN_1}	-0.6 to V_{CC} + 0.3	V
Programming Voltage with respect to ground	V_{IN_2}	-0.6 to + 13.5	V
Temperature under Bias	T_{BIAS}	-25 to + 85	°C
Storage Temperature Range	T_{STG}	-65 to + 125	°C

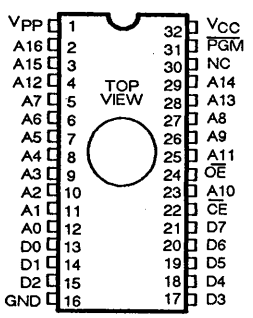
NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



CERAMIC PACKAGE
DIP-32C-C01

LCC-36C-F01 See Page 11

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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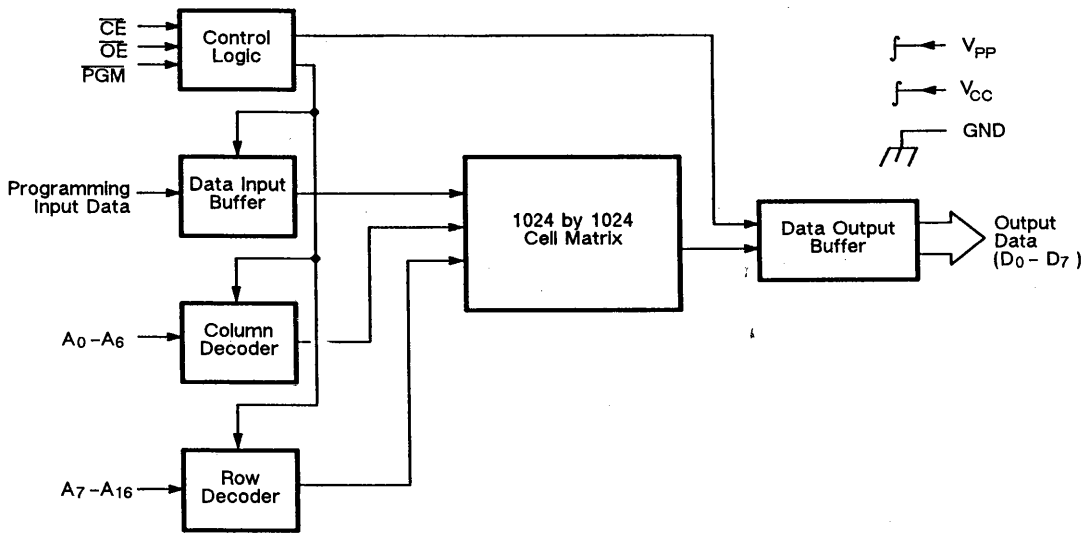
Fig. 1 — BLOCK DIAGRAM



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CAPACITANCE (T_A = 25 °C, f = 1MHz)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Capacitance (V_{IN} = 0V)	C_{IN}			12	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}			12	pF

PIN DESCRIPTION

Symbol	Pin No. *	Function
V_{PP}	1	+12.5V programming voltage.
$A_0 - A_{16}$	2-12, 23 25-29	Address lines.
$O_0 - O_7$	13-15, 17-21	Three-state output data lines.
GND	16	Circuit ground.
$\overline{CE}$	22	When active Low, the device is enabled for data read.
$\overline{OE}$	24	Output enable. When $\overline{OE}$ and $\overline{CE}$ are active low and the $\overline{PGM}$ strobe is active High; all output lines ($D_0 - D_7$) are enabled.
NC	30	No connection.
$\overline{PGM}$	31	When active Low, programming data from the input buffer is written into a specified address of memory.
V_{CC}	32	+5V power supply

* This numbers are applied to DIP package.

FUNCTIONS AND PIN CONNECTIONS

OPERATING MODE	$A_0 - A_8$	A_9	$A_{10} - A_{16}$	Data	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{CC}	V_{PP}	GND
Standby	X	X	X	Hi - Z	V_{IH}	X	X	5V	5V	0V
Read	A_{IN}	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	5V	5V	0V
Output Disable	A_{IN}	A_{IN}	A_{IN}	Hi-Z	V_{IL}	V_{IH} X	X V_{IL}	5V	5V	0V
Electronic Signature	Note 1	12V	X	CODE	V_{IL}	V_{IL}	V_{IH}	5V	5V	0V
Single Byte Program	A_{IN}	A_{IN}	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	6V	12.5V	0V
Single Byte Verify	A_{IN}	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	6V	12.5V	0V
Single Byte Program Inhibit	A_{IN}	A_{IN}	A_{IN}	Hi-Z	V_{IL}	V_{IH}	V_{IH}	6V	12.5V	0V
Four Byte Data Input	Note 2	A_{IN}	A_{IN}	D_{IN}	V_{IH}	V_{IH}	V_{IH}	6V	12.5V	0V
Four Byte Program	X	A_{IN}	A_{IN}	Hi-Z	V_{IH}	V_{IL}	V_{IL}	6V	12.5V	0V
Four Byte Verify	Note 2	A_{IN}	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	6V	12.5V	0V
Four Byte Program Inhibit	A_{IN}	A_{IN}	A_{IN}	Hi-Z	V_{IL}	V_{IH}	V_{IH}	6V	12.5V	0V

Legend:
X = Don't care

Notes:

1. A_0 is toggling address. A_1 is V_{IL}.
2. A_0 and A_1 can be either V_{IL} or V_{IH}

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{PP}	V_{CC} -0.6	V_{CC}	V_{CC} +0.6	V
Input High Level	V_{IH}	2.0		V_{CC} +0.3	V
Input Low Level	V_{IL}	-0.1		0.8	V
Supply Voltage	GND		0		V
Operating Temperature	T_A	0		70	°C

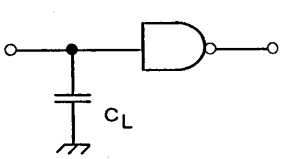
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Input Leakage Current	I_{LI}	V_{IN} = V_{CC} = 5.5V			10	µA
Output Leakage Current	I_{LO}	V_{IN} = V_{CC} = 5.5V			10	µA
V_{CC} Standby Current	I_{SB_1}	$\overline{CE}$=V_{IH}			1	mA
V_{CC} Standby Current	I_{SB_2}	$\overline{CE}$=V_{CC}±0.3V		1	100	µA
V_{CC} Active Current	I_{CC_1}	$\overline{CE}$=V_{IL}, I_{OUT} =0mA			30	mA
V_{CC} Operation Current 150ns	I_{CC_2}	$\overline{CE}$=V_{IL}: f =min, I_{OUT} =0mA			40	mA
V_{CC} Operation Current 200ns/250ns					30	
V_{PP} Supply Current	I_{PP}	V_{PP} = V_{CC} ±0.6V		1	100	µA
Output Low Level	V_{OL}	I_{OL} =2.1mA			0.45	V
Output High Level	V_{OH_1}	I_{OH} = -400 µ A	2.4			V
Output High Level	V_{OH_2}	I_{OH} = -100 µ A	V_{CC} -0.7			V

Fig. 2 — AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input pulse levels:	0.45V to 2.4V (0.3V to 2.8V programming)
Input Rise/Fall Times:	≤20ns
Input Reference Levels:	0.8V to 2.0V (0.6V to 2.4V programming)
Output Reference Levels:	0.8V to 2.0V
Output Load:	1 TTL gate and C_L =100pF



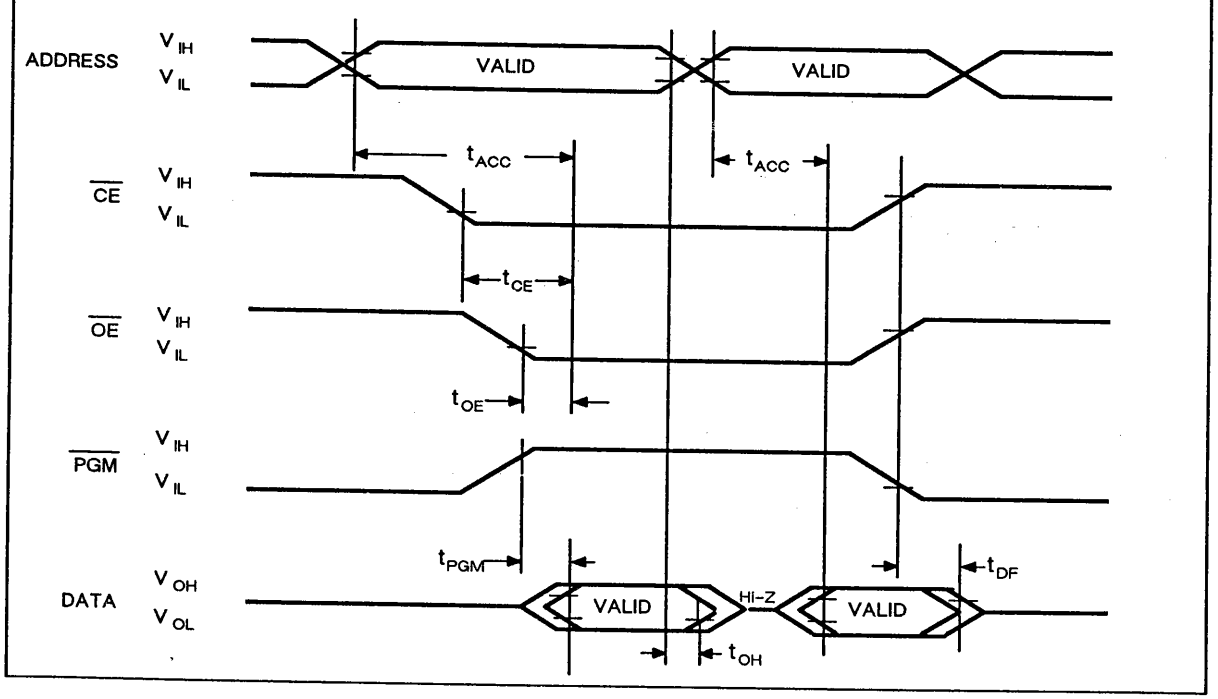
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM27C1001-15 Values		MBM27C1001-20 Values		MBM27C1001-25 Values		Unit
		Min	Max	Min	Max	Min	Max	
Address Access Time	t_{ACC}		150		200		250	ns
$\overline{CE}$ to Output Delay Time	t_{CE}		150		200		250	ns
$\overline{OE}$ to Output Delay Time	t_{OE}		70	0	70	0	100	ns
$\overline{PGM}$ to Output Delay Time	t_{PGM}		70	0	70	0	100	ns
$\overline{CE}$ or $\overline{OE}$ to Output Float Delay (Note)	t_{DF}		60		60		60	ns
Address to Output Hold Time	t_{OH}	0		0		0		ns

NOTE: Output Float is defined as the point where data is no longer driven.

READ WAVEFORM



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PROGRAMMING / ERASING INFORMATION

PROGRAMMING

Single-Byte Programming. When +12.5V(±0.3) volts is applied to V_{PP}, +6(±0.25) volts is applied to V_{CC}, $\overline{CE}$ and $\overline{PGM}$ = V_{IH}, and $\overline{OE}$ = V_{IH}, the programming mode is initiated. Next, the proper address is input and the data pattern is applied to the input buffer (Figure 1). When both address and data are stable, a 0.5-millisecond negative pulse is applied to the $\overline{PGM}$ pin. Upon verification of written data an over pulse (three times the initial pulse width times the number of pulses used to accomplish a write) should be applied to complete the programming of one byte. Refer to the PROGRAMMING FLOWCHART that follows for step-by-step programming procedures.

Four-Byte Programming. When compared to single-byte programming, the four-byte programming method reduces the programming time by about 75% one quarter. Voltages applied to VPP and VCC are the same as those for single-byte programming; however, some logic levels differ--refer to "Four Byte Programming" in the Truth Table. In conjunction with the $\overline{OE}$ pin, address pins A0 and A1 are used to latch four bytes of data. When both address and data are stable, a 0.5 millisecond negative pulse is applied to the $\overline{PGM}$ pin. Upon verification of written data an over pulse (three times the initial pulse width times the number of pulses used to accomplish a write,) should be applied to complete the programming of four bytes. Refer to the PROGRAMMING FLOWCHART for step-by-step programming procedures.

Caution

The width of one programming pulse must not exceed 40-millisecond; thus, a continuous TTL low-level voltage should not be applied to the $\overline{PGM}$ pin. Also, a 0.1-microfarad capacitor must be connected between V_{PP} and ground to prevent excessive voltage transients. Neglecting either of these precautions may cause device failure.

Electronic Signature/Programming Algorithm. When the MBM27C1001 is shipped from the factory, all memory cells (1,048,576 bits) are set to the High state (logic 1). During the programming procedure, affected bit cells are set to the Low (logic 0) state.

The MBM27C1001 is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. Manufacturer and device codes are electronically stored in each device; these codes can be read at the output port (D0-D7) for the purpose of matching the device with the Quick Pro™ algorithm. The Electronic Signature Code List is shown preceding the ELECTRICAL CHARACTERISTICS.

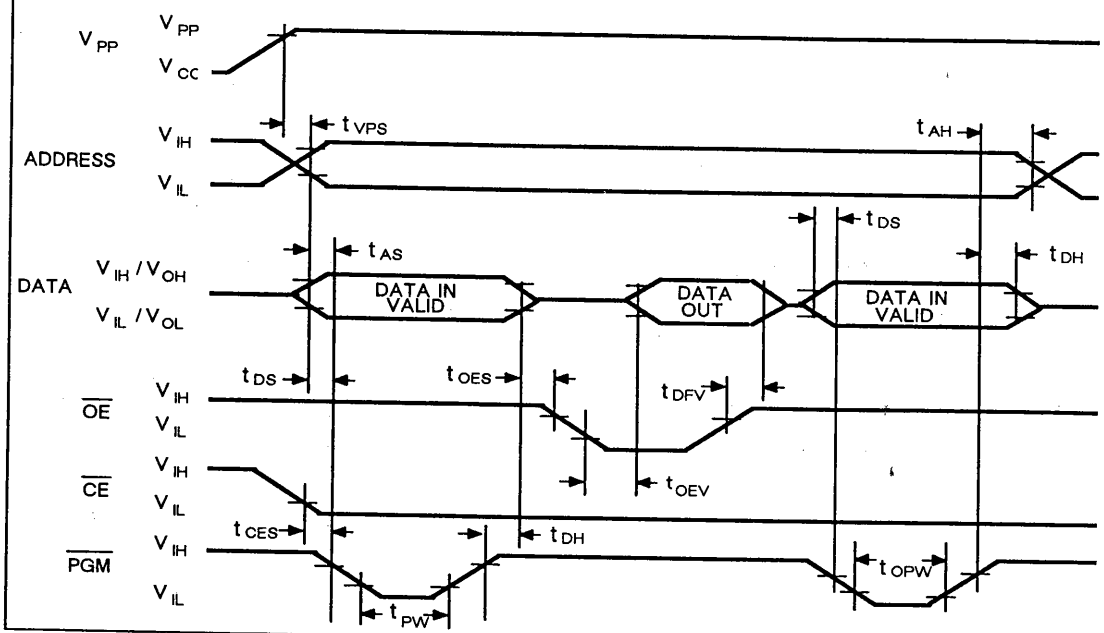
ERASING

In order to clear all memory cells of programmed contents, the MBM27C1001 must be exposed to an ultraviolet light source. To completely erase the memory (restore all cells to a logic 1 state), a dosage of 15Wsec/cm^2 is required. The required exposure can be obtained by using a UV-lamp with a wavelength of 2537 Angstroms and with an intensity of 12mW/cm^2. Remove all filters from the lamp and clean the transparent lid of the MBM 27C1001 with a non-abrasive cleaner. Hold the MBM 27C1001 approximately one inch from the light source for 15-to-21 minutes. (Note. The MBM 27C1001 and other similar devices can be erased by light sources with longer wavelengths: however, the erasing time is much greater. Nonetheless, exposure to fluorescents or sunlight will severely degrade and eventually erase the memory. When used in a lighted environment, it is recommended that the transparent window be covered with an opaque label.)

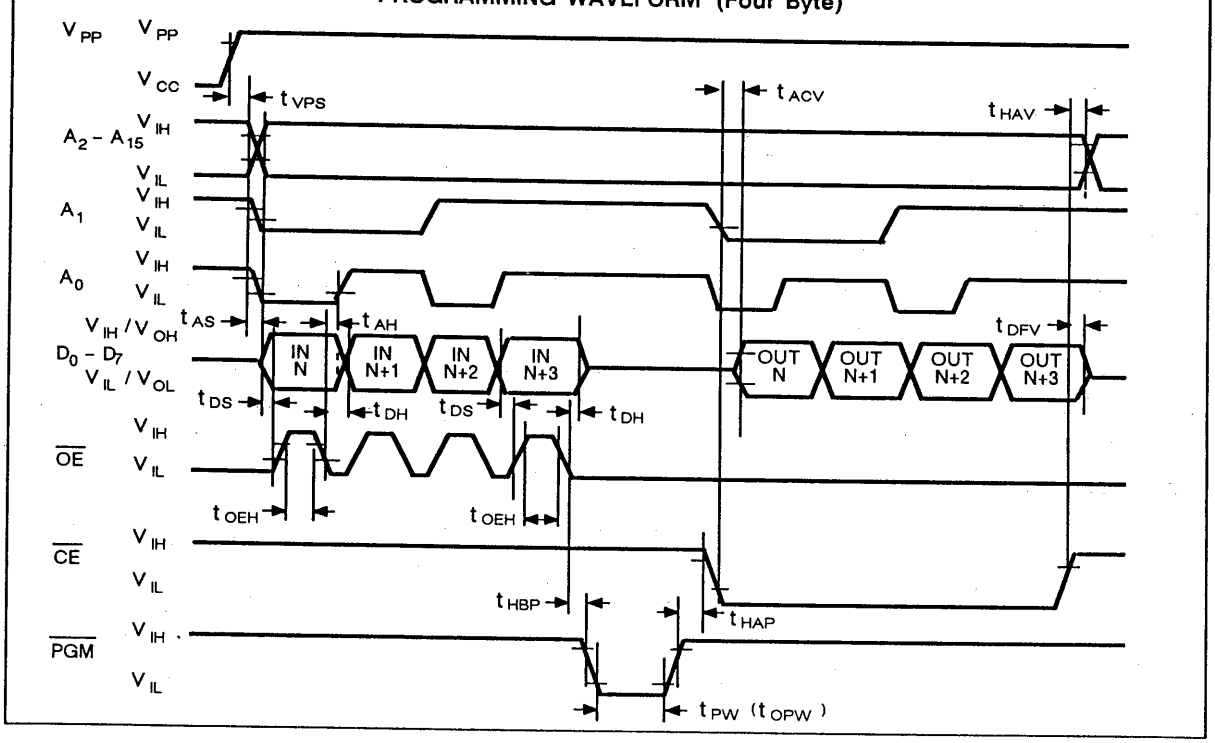
ELECTRONIC SIGNATURE CODE LIST

Definition	AO	A1 TO A6	A9	A7 to A16	D0	D1	D2	D3	D4	D5	D6	D7	HEX
Manufacture	VIL	VIL	12(±0.5)V	Don't Care	0	0	1	0	0	0	0	0	#04
Device	VIH	VIL	12(±0.5)V	Don't Care	0	1	1	0	0	1	1	1	#E6

PROGRAMMING WAVEFORM (Single Byte)



PROGRAMMING WAVEFORM (Four Byte)



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DC CHARACTERISTICS (Programming Mode)

(T_A= 25 °C ± 5°C, V_{CC}[1] = 6V ± 0.25V, V_{PP}[2] = 12.5V ± 0.3V)

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Input Leakage Current	I_{LI}	VIN = 6.25V/0V			10	µA
Input High Level	V_{IH}		2.4		V_{CC}+0.3	V
Input Low Level	V_{IL}		-0.1		0.6	V
V_{CC} Supply Current	I_{CC}				30	mA
V_{PP} Supply Current	I_{PP1}	$\overline{CE}$=$\overline{PGM}$=V_{IL} ; $\overline{OE}$=V_{IH}			30	mA
V_{PP} Supply Current	I_{PP2}	$\overline{CE}$=V_{IH} ; $\overline{OE}$=$\overline{PGM}$=V_{IL}			100	mA
V_{PP} Supply Current	I_{PP3}	$\overline{PGM}$=V_{IH}			5	mA
Output Low Level	V_{OL}	IOL=2.1mA			0.45	V
Output High Level	V_{OH}	IOH=-400 µA	2.4			V

NOTE *1 V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.

*2 V_{PP} must not be greater than 13.5 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 12.5 volts. Also, during $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, V_{PP} must not be switched from V_{CC} to V_{PP} volts or vice versa.

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AC CHARACTERISTICS
(Single Byte Programming)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
V_{PP} Setup Time	t_{VPS}	2			µS
Address Setup Time	t_{AS}	2			µS
Data Setup Time	t_{DS}	2			µS
$\overline{CE}$ Setup Time	t_{CES}	2			µS
$\overline{OE}$ Setup time	t_{OES}	2			µS
Address Hold Time	t_{AH}	2			µS
Data Hold Time	t_{DH}	2			µS
$\overline{OE}$ to Output Valid	t_{OEV}			500	ns
$\overline{OE}$ to Output Float	t_{DFV}			150	ns
Programming Pulse Width	t_{PW}	0.475	0.50	0.525	ms
Over Programming Pulse Number	N	1		25	times
Over Programming Pulse Width (Note)	t_{OPW}	1.4	1.5	39.4	ms

NOTE: t_{OPW} = 1.5 x Nms ± 5%

AC CHARACTERISTICS
(Four Byte Programming)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
V_{PP} Setup Time	t_{VPS}	2			µS
Address Setup Time	t_{AS}	2			µS
Data Setup Time	t_{DS}	2			µS
Address Hold Time	t_{AH}	2			µS
Data Hold Time	t_{DH}	2			µS
$\overline{OE}$ High Hold Time	t_{OEH}	2			µS
Hold Time Before Programming	t_{HBP}	2			µS
Hold Time After Program	t_{HAP}	2			µS
Address Access Time at Verify	t_{ACV}			500	ns
$\overline{CE}$ to Output Float at Verify	t_{DFV}			150	ns
Hold Time After Verify	t_{HAV}	0			µS
Programming Pulse Width	t_{PW}	0.475	0.50	0.525	ms
Over Programming Pulse Number	N	1		25	times
Over Programming Pulse Width (Note)	t_{OPW}	1.4	1.5	39.4	ms

NOTE: $t_{OPW} = 1.5 \times Nms \pm 5\%$

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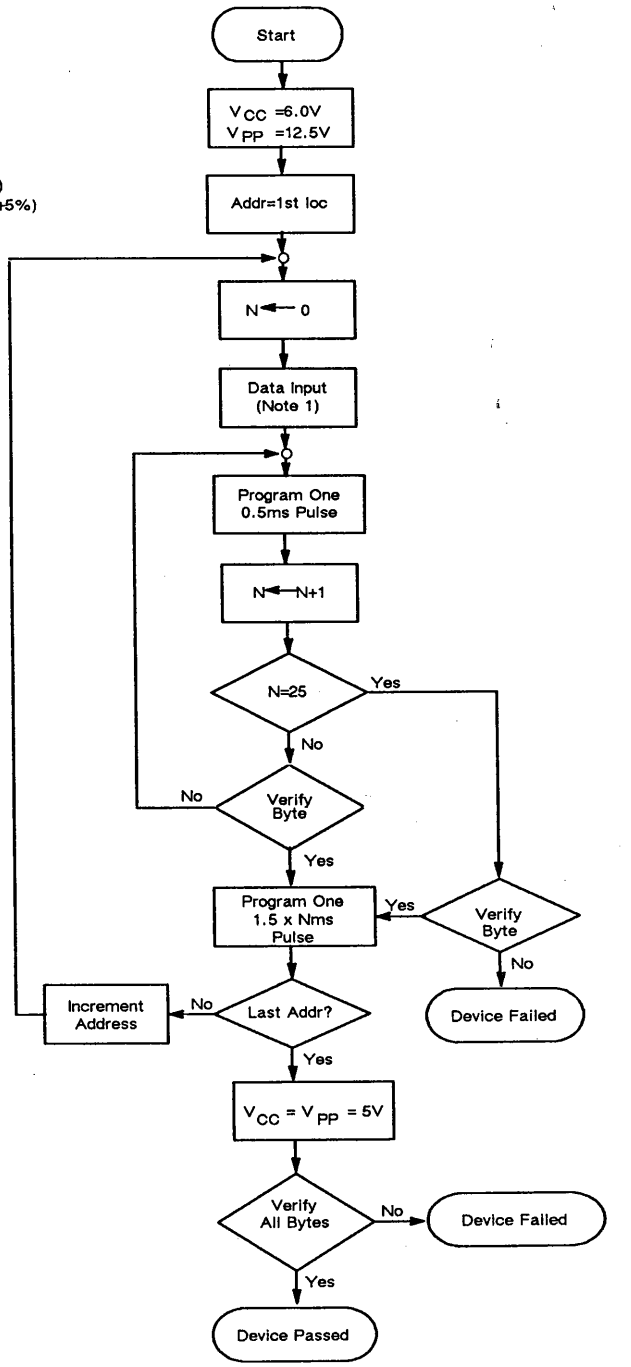
PROGRAMMING / ERASING INFORMATION (Cont'd)

PROGRAMMING FLOWCHART FOR QUICK PRO ™

Notes:
1. 1-byte or 4-bytes
2. Conditions:
   V_{CC} =6V(±0.25)
   V_{PP} =12.5(±0.3)V
   t_{PW} =0.5ms (+5%)
   t_{OPW} =1.5 x Nms (+5%)



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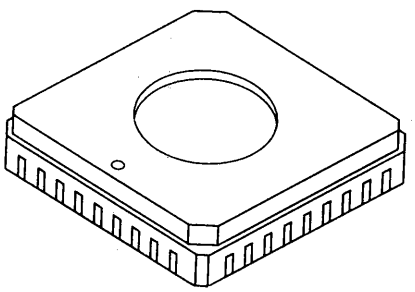
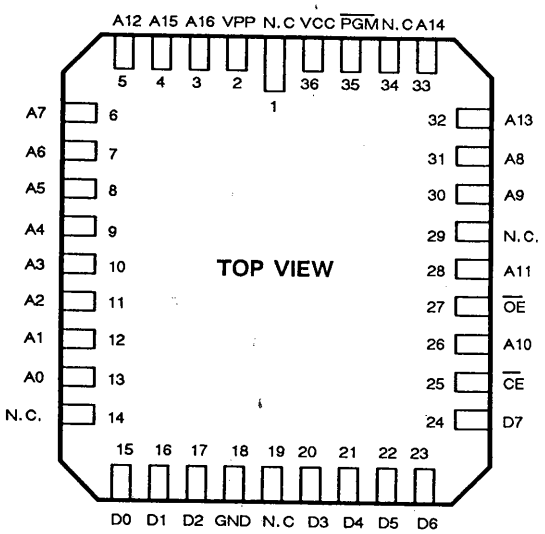
PACKAGE DIMENSIONS

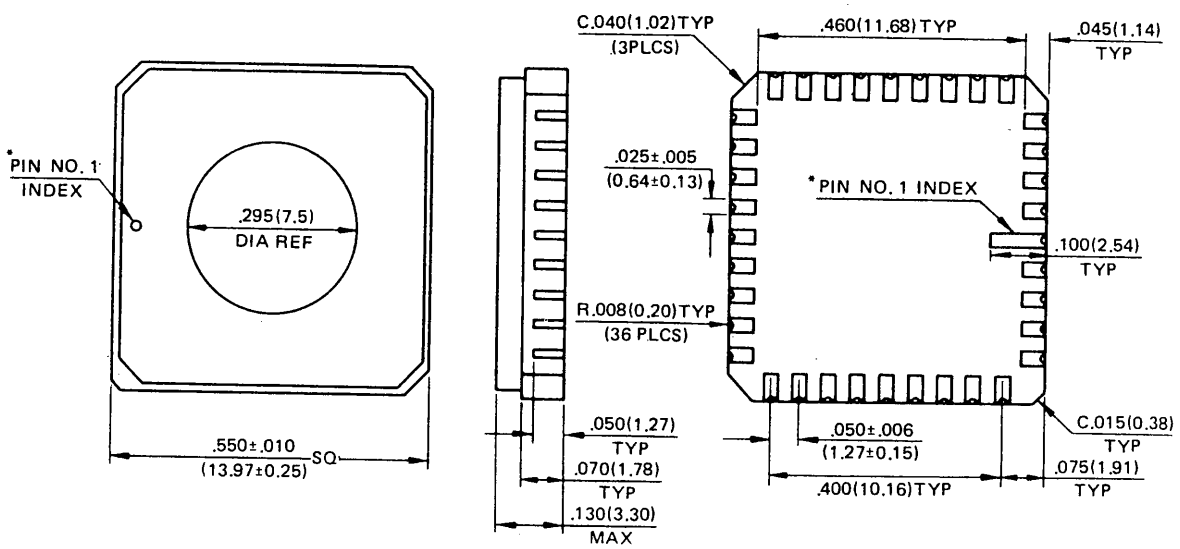


LCC-36C-F01

PIN ASSIGNMENT



32-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(Case No.: LCC-36C-F01)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimension in
inches (millimeters)

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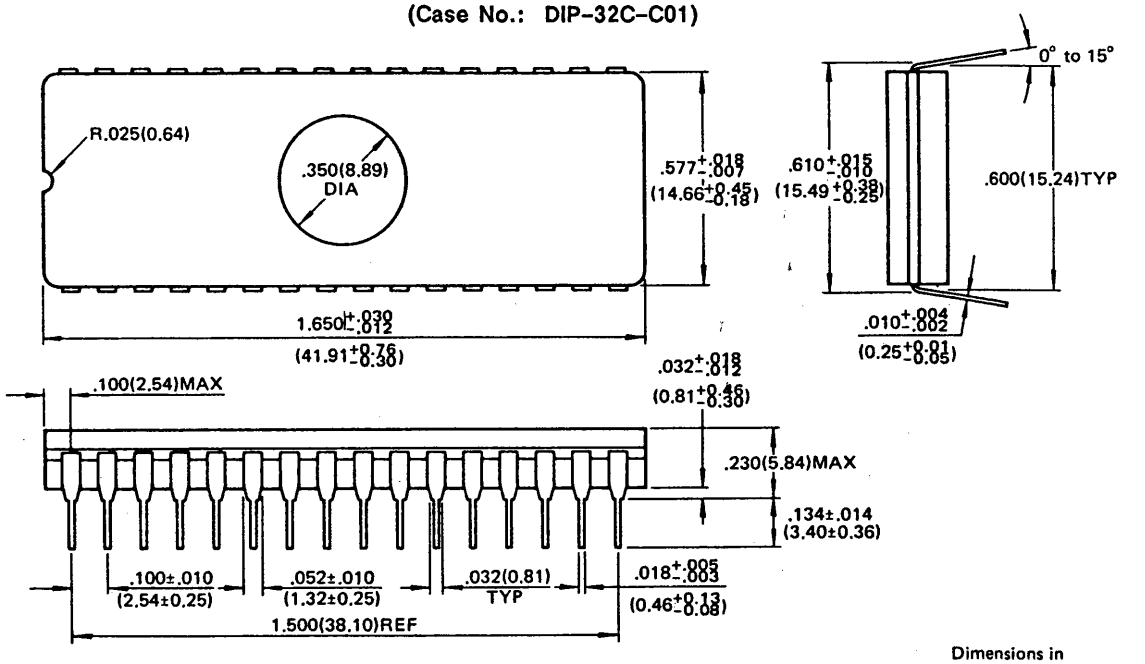
PACKAGE DIMENSIONS

32-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(Case No.: DIP-32C-C01)



Dimensions in inches (millimeters).

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