Lead-Free Package Options Available!

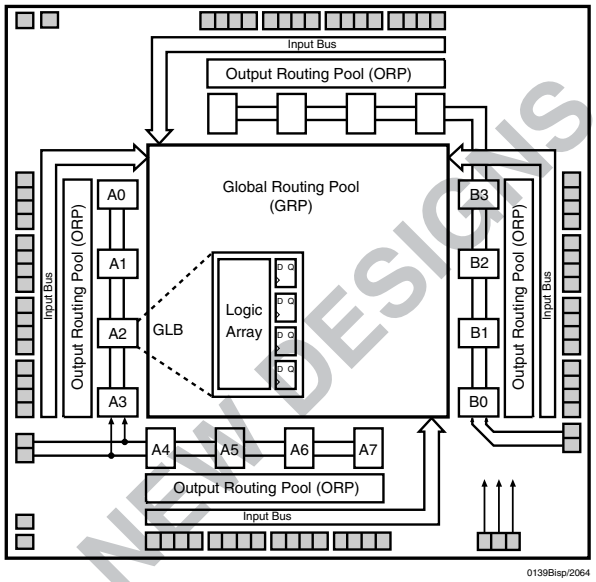
ispLSI® 2064/A

In-System Programmable High Density PLD

Features

- **ENHANCEMENTS**
  - — ispLSI 2064A is Fully Form and Function Compatible to the ispLSI 2064, with Identical Timing Specifcations and Packaging
  - — ispLSI 2064A is Built on an Advanced 0.35 Micron E²CMOS® Technology
- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - — 2000 PLD Gates
  - — 64 I/O Pins, Four Dedicated Inputs
  - — 64 Registers
  - — High Speed Global Interconnect
  - — Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - — Small Logic Block Size for Random Logic
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - — f_{max} = 125 MHz Maximum Operating Frequency
  - — t_{pd} = 7.5 ns Propagation Delay
  - — TTL Compatible Inputs and Outputs
  - — Electrically Erasable and Reprogrammable
  - — Non-Volatile
  - — 100% Tested at Time of Manufacture
  - — Unused Product Term Shutdown Saves Power
- **IN-SYSTEM PROGRAMMABLE**
  - — In-System Programmable (ISP™) 5V Only
  - — Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality
  - — Reprogram Soldered Devices for Faster Prototyping
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - — Complete Programmable Device Can Combine Glue Logic and Structured Designs
  - — Enhanced Pin Locking Capability
  - — Three Dedicated Clock Input Pins
  - — Synchronous and Asynchronous Clocks
  - — Programmable Output Slew Rate Control to Minimize Switching Noise
  - — Flexible Pin Placement
  - — Optimized Global Routing Pool Provides Global Interconnectivity
  - — Lead-Free Package Options

Functional Block Diagram



Description

The ispLSI 2064 and 2064A are High Density Programmable Logic Devices. The devices contain 64 Registers, 64 Universal I/O pins, four Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The 2064 and 2064A feature 5V in-system programmability and in-system diagnostic capabilities. The ispLSI 2064 and 2064A offer non-volatile reprogrammability of the logic, as well as the interconnect, to provide truly reconfigurable systems.

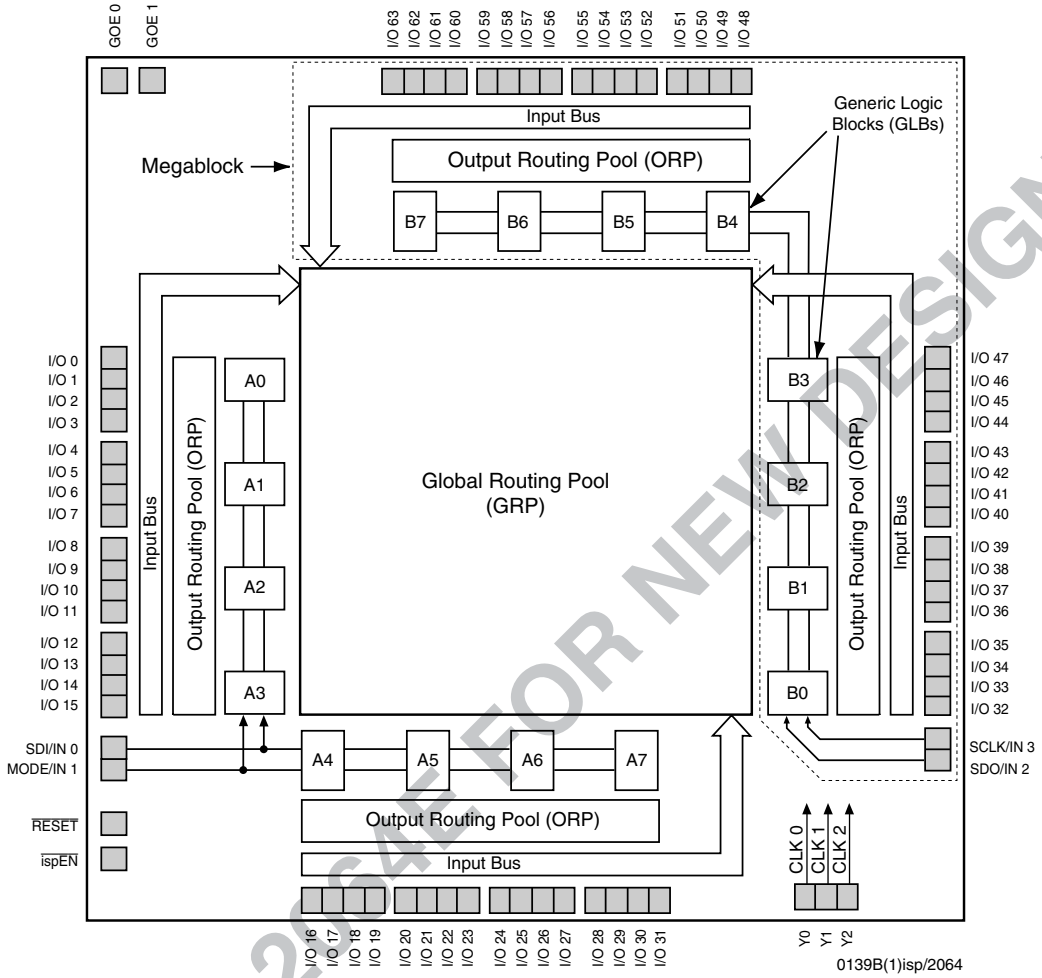
The basic unit of logic on these devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1…B7 (Figure 1). There are a total of 16 GLBs in the ispLSI 2064 and 2064A devices. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 268-8000; 1-800-LATTICE; FAX (503) 268-8556; http://www.latticesemi.com

August 2006

Functional Block Diagram

Figure 1. ispLSI 2064/A Functional Block Diagram



The devices also have 64 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (Figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by two ORPs. Each ispLSI 2064 and 2064A device contains two Megablocks.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 2064 and 2064A devices are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Absolute Maximum Ratings [1]

Supply Voltage V_{cc} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ..... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial T_A = 0°C to + 70°C	4.75	5.25	V
		Industrial T_A = -40°C to + 85°C	4.5	5.5	V
V_{IL}	Input Low Voltage		0	0.8	V
V_{IH}	Input High Voltage		2.0	V_{cc}+1	V

Table 2 - 0005/2064

Capacitance (TA=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	V_{CC} = 5.0V, V_{IN} = 2.0V
C_2	I/O Capacitance	9	pf	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V
C_3	Clock Capacitance	15	pf	V_{CC} = 5.0V, V_Y = 2.0V

Table 2-0006/2064

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
Erase/Reprogram Cycles	10000	–	Cycles

Table 2-0008/2064

Switching Test Conditions

Input Pulse Levels	GND to 3.0V	
Input Rise and Fall Time 10% to 90%	-125	≤ 2 ns
	Others	≤ 3 ns
Input Timing Reference Levels	1.5V	
Output Timing Reference Levels	1.5V	
Output Load	See Figure 2	

Table 2-0003/2064

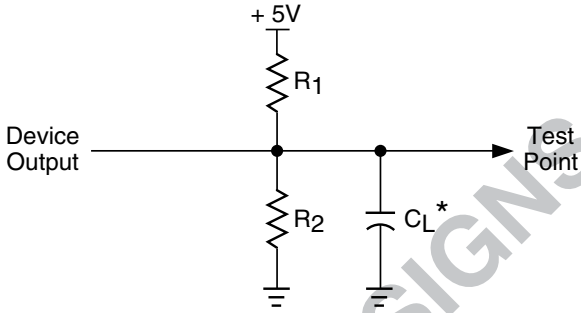
3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see Figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH}-0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL}+0.5V	470Ω	390Ω	5pF

Table 2-0004/2064

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
$I_{IL\text{-}isp}$	$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
$I_{IL\text{-}PU}$	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V	Commercial	–	95	175	mA
		f_{CLOCK} = 1 MHz	Industrial	–	95	–	mA

Table 2-0007/2064

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using four 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-125		-100		-80		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	7.5	–	10.0	–	15.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	10.0	–	13.0	–	18.5	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	125	–	100	–	81.0	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	100	–	77.0	–	57.0	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle	125	–	111	–	100	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	5.0	–	6.5	–	9.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	4.0	–	5.0	–	6.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	6.0	–	8.0	–	11.0	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	4.5	–	6.0	–	8.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	10.0	–	13.5	–	17.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	5.0	–	6.5	–	10.0	–	ns
t_{ptoeen}	B	14	Product Term OE, Enable	–	12.0	–	15.0	–	18.0	ns
$t_{ptoedis}$	C	15	Product Term OE, Disable	–	12.0	–	15.0	–	18.0	ns
t_{goeen}	B	16	Global OE, Enable	–	7.0	–	9.0	–	12.0	ns
t_{goedis}	C	17	Global OE, Disable	–	7.0	–	9.0	–	12.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	4.0	–	4.5	–	5.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	4.0	–	4.5	–	5.0	–	ns

Table 2 - 0030B/2064-130

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

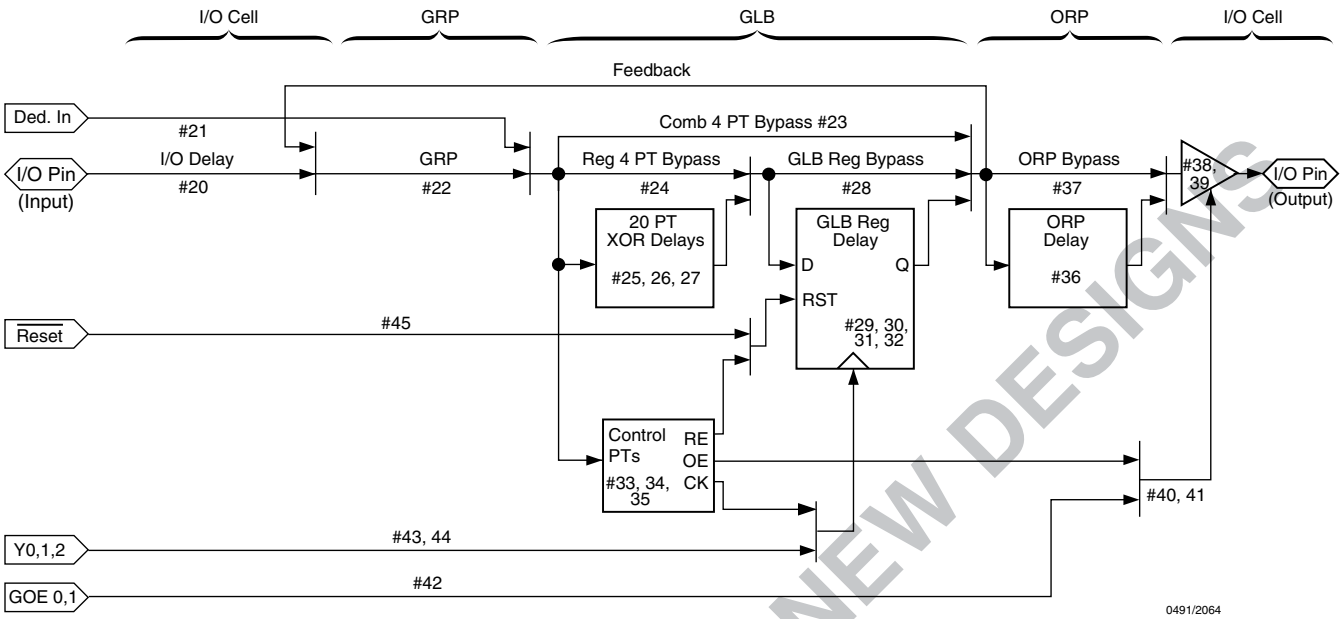
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-125		-100		-80		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t_{io}	20	Input Buffer Delay	–	0.2	–	0.5	–	1.8	ns
t_{din}	21	Dedicated Input Delay	–	1.5	–	2.2	–	4.4	ns
GRP									
t_{grp}	22	GRP Delay	–	1.3	–	1.7	–	2.6	ns
GLB									
t_{4ptbp}	23	4 Product Term Bypass Comb. Path Delay	–	4.5	–	5.8	–	8.1	ns
t_{4ptbp}	24	4 Product Term Bypass Reg. Path Delay	–	5.0	–	5.8	–	6.8	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	–	5.7	–	6.8	–	8.0	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	–	6.0	–	7.3	–	8.8	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	–	6.5	–	8.0	–	9.8	ns
t_{gbp}	28	GLB Register Bypass Delay	–	0.5	–	0.5	–	1.3	ns
t_{gsu}	29	GLB Register Setup Time before Clock	0.8	–	1.2	–	1.4	–	ns
t_{gh}	30	GLB Register Hold Time after Clock	3.0	–	4.0	–	6.0	–	ns
t_{gco}	31	GLB Register Clock to Output Delay	–	0.2	–	0.3	–	0.4	ns
t_{gro}	32	GLB Register Reset to Output Delay	–	1.1	–	1.3	–	1.6	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	–	4.8	–	6.1	–	8.6	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	–	7.3	–	8.6	–	9.0	ns
t_{ptck}	35	GLB Product Term Clock Delay	3.3	5.6	4.1	7.1	5.6	10.2	ns
ORP									
t_{orp}	36	ORP Delay	–	0.8	–	1.4	–	2.0	ns
t_{orpbp}	37	ORP Bypass Delay	–	0.3	–	0.4	–	0.5	ns
Outputs									
t_{ob}	38	Output Buffer Delay	–	1.2	–	1.6	–	2.0	ns
t_{sl}	39	Output Slew Limited Delay Adder	–	10.0	–	10.0	–	10.0	ns
t_{oen}	40	I/O Cell OE to Output Enabled	–	3.2	–	4.2	–	4.6	ns
t_{odis}	41	I/O Cell OE to Output Disabled	–	3.2	–	4.2	–	4.6	ns
t_{goe}	42	Global Output Enable	–	3.8	–	4.8	–	7.4	ns
Clocks									
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	2.3	2.3	2.7	2.7	3.6	3.6	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.3	2.3	2.7	2.7	3.6	3.6	ns
Global Reset									
t_{gr}	45	Global Reset to GLB	–	6.9	–	9.2	–	11.4	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Table 2- 0036C/2064-130

ispLSI 2064/A Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu = Logic + Reg su - Clock (min)
= (**t**io + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**io + **t**grp + **t**ptck(min))
= (#20 + #22 + #26) + (#29) - (#20 + #22 + #35)
3.5 ns = (0.2 + 1.3 + 6.0) + (0.8) - (0.2 + 1.3 + 3.3)

th = Clock (max) + Reg h - Logic
= (**t**io + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**io + **t**grp + **t**20ptxor)
= (#20 + #22 + #35) + (#30) - (#20 + #22 + #26)
2.6 ns = (0.2 + 1.3 + 5.6) + (3.0) - (0.2 + 1.3 + 6.0)

tco = Clock (max) + Reg co + Output
= (**t**io + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#20 + #22 + #35) + (#31) + (#36 + #38)
9.4 ns = (0.2 + 1.3 + 5.6) + (0.2) + (0.8 + 1.2)

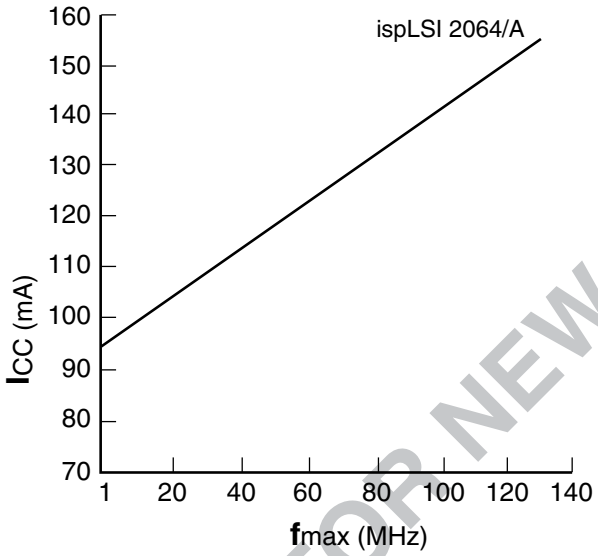
Table 2- 0042A-2064

Note: Calculations are based upon timing specifications for the ispLSI 2064/A-125L.

Power Consumption

Power consumption in the ispLSI 2064 and 2064A devices depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 4 shows the relationship between power and operating speed.

Figure 4. Typical Device Power Consumption vs fmax



Notes: Configuration of Four 16-bit Counters
Typical Current at 5V, 25° C

I_{CC} can be estimated for the ispLSI 2064/A using the following equation:

I_{CC}(mA) = 38 + (# of PTs * 0.33) + (# of nets * Max freq * 0.007)

Where:
- # of PTs = Number of Product Terms used in design
- # of nets = Number of Signals used in device
- Max freq = Highest Clock Frequency to the device (in MHz)

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127A/2064A

Pin Description

NAME	PLCC PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 3	26, 27, 28, 29,	Input/Output Pins — These are the general purpose I/O pins used by the logic array.
I/O 4 - I/O 7	30, 31, 32, 33,	
I/O 8 - I/O 11	34, 35, 36, 37,	
I/O 12 - I/O 15	38, 39, 40, 41,	
I/O 16 - I/O 19	45, 46, 47, 48,	
I/O 20 - I/O 23	49, 50, 51, 52,	
I/O 24 - I/O 27	53, 54, 55, 56,	
I/O 28 - I/O 31	57, 58, 59, 60,	
I/O 32 - I/O 35	68, 69, 70, 71,	
I/O 36 - I/O 39	72, 73, 74, 75,	
I/O 40 - I/O 43	76, 77, 78, 79,	
I/O 44 - I/O 47	80, 81, 82, 83,	
I/O 48 - I/O 51	3, 4, 5, 6,	
I/O 52 - I/O 55	7, 8, 9, 10,	
I/O 56 - I/O 59	11, 12, 13, 14,	
I/O 60 - I/O 63	15, 16, 17, 18	
GOE 0, GOE 1	67, 84	Global Output Enable input pins.
Y0, Y1, Y2	20, 66, 63	Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs in the device.
$\overline{\text{RESET}}$	24	Active Low (0) Reset pin which resets all registers in the device.
$\overline{\text{ispEN}}$	23	Input — Dedicated in-system programming enable pin. This pin is brought low to enable the programming mode. When low, the MODE, SDI, SDO and SCLK controls become active.
SDI/ IN 0[2]	25	Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the ISP state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated pin input.
MODE/ IN 1[2]	42	Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the ISP state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
SDO/IN 2[2]	44	Output/Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
SCLK/IN 3[2]	61	Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
GND	1, 22, 43, 64	Ground (GND)
VCC	21, 65	Vcc
NC[1]	2, 19, 62	No Connect

1. NC pins are not to be connected to any active signals, VCC or GND.
2. Pins have dual function capability.

Table 2-0002A-08isp/2064

Pin Description

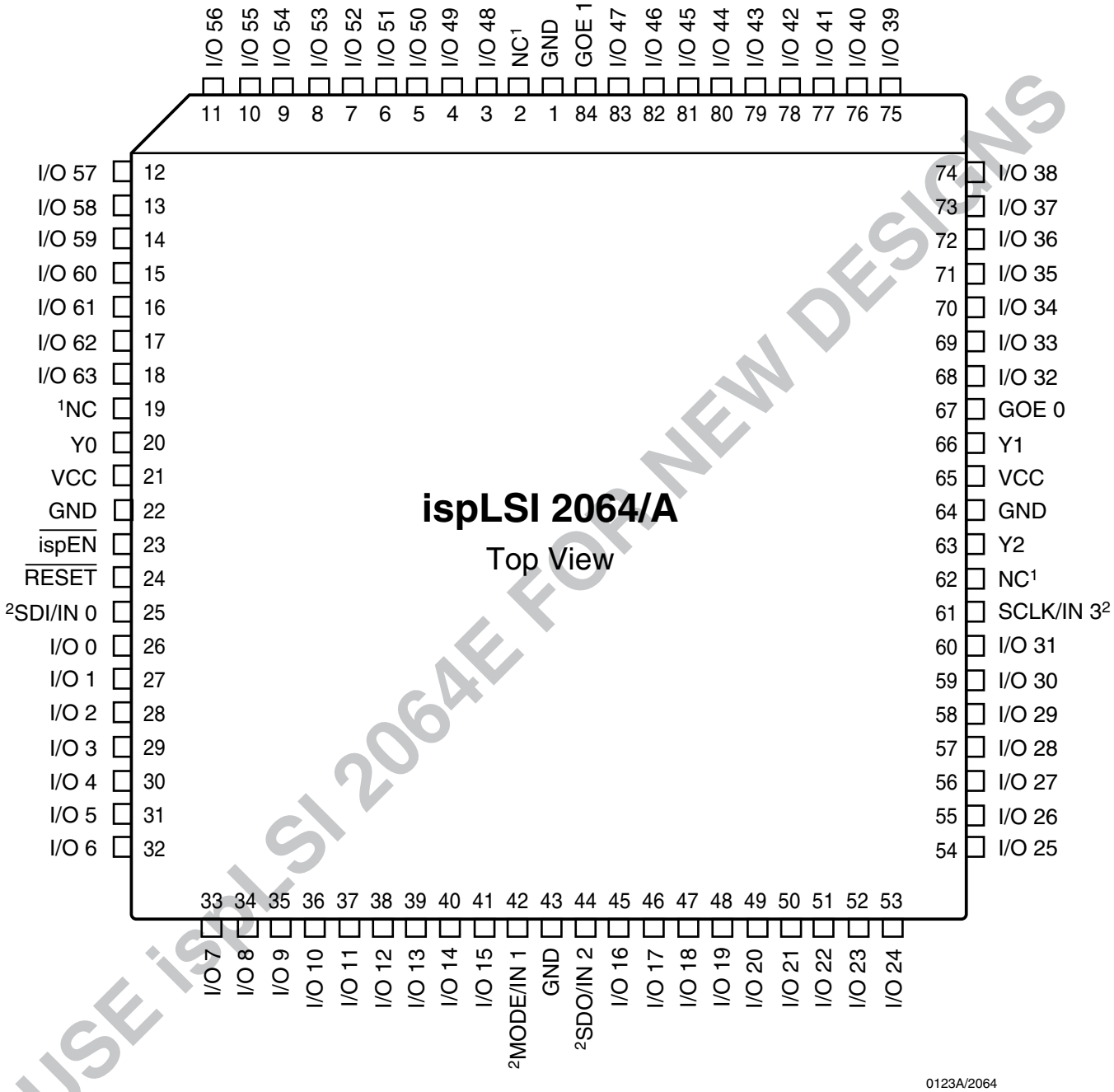
NAME	TQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47 I/O 48 - I/O 51 I/O 52 - I/O 55 I/O 56 - I/O 59 I/O 60 - I/O 63	17, 18, 19, 20, 21, 22, 23, 28, 29, 30, 31, 32, 33, 34, 35, 36, 40, 41, 42, 43, 44, 45, 46, 47, 48, 53, 54, 55, 56, 57, 58, 59, 67, 68, 69, 70, 71, 72, 73, 78, 79, 80, 81, 82, 83, 84, 85, 86, 90, 91, 92, 93, 94, 95, 96, 97, 98, 3, 4, 5, 6, 7, 8, 9	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE 0, GOE 1	66, 87	Global Output Enable input pins.
Y0, Y1, Y2	11, 65, 62	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
$\overline{\text{RESET}}$	15	Active Low (0) Reset pin which resets all of the registers in the device.
$\overline{\text{ispEN}}$	14	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK controls become active.
SDI/IN 0[2]	16	Input – This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the ISP state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
MODE/IN 1[2]	37	Input – This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the ISP state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
SDO/IN 2[2]	39	Output/Input – This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
SCLK/IN 3[2]	60	Input – This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
GND	13, 38, 63, 88	Ground (GND)
VCC	12, 64	V_{CC}
NC[1]	1, 2, 10, 24, 25, 26, 27, 49, 50, 51, 52, 61, 74, 75, 76, 77, 89, 99, 100	No Connect.

Table 2-0002-2064b.eps

1. NC pins are not to be connected to any active signals, VCC or GND.
2. Pins have dual function capability.

Pin Configuration

ispLSI 2064/A 84-Pin PLCC Pinout Diagram

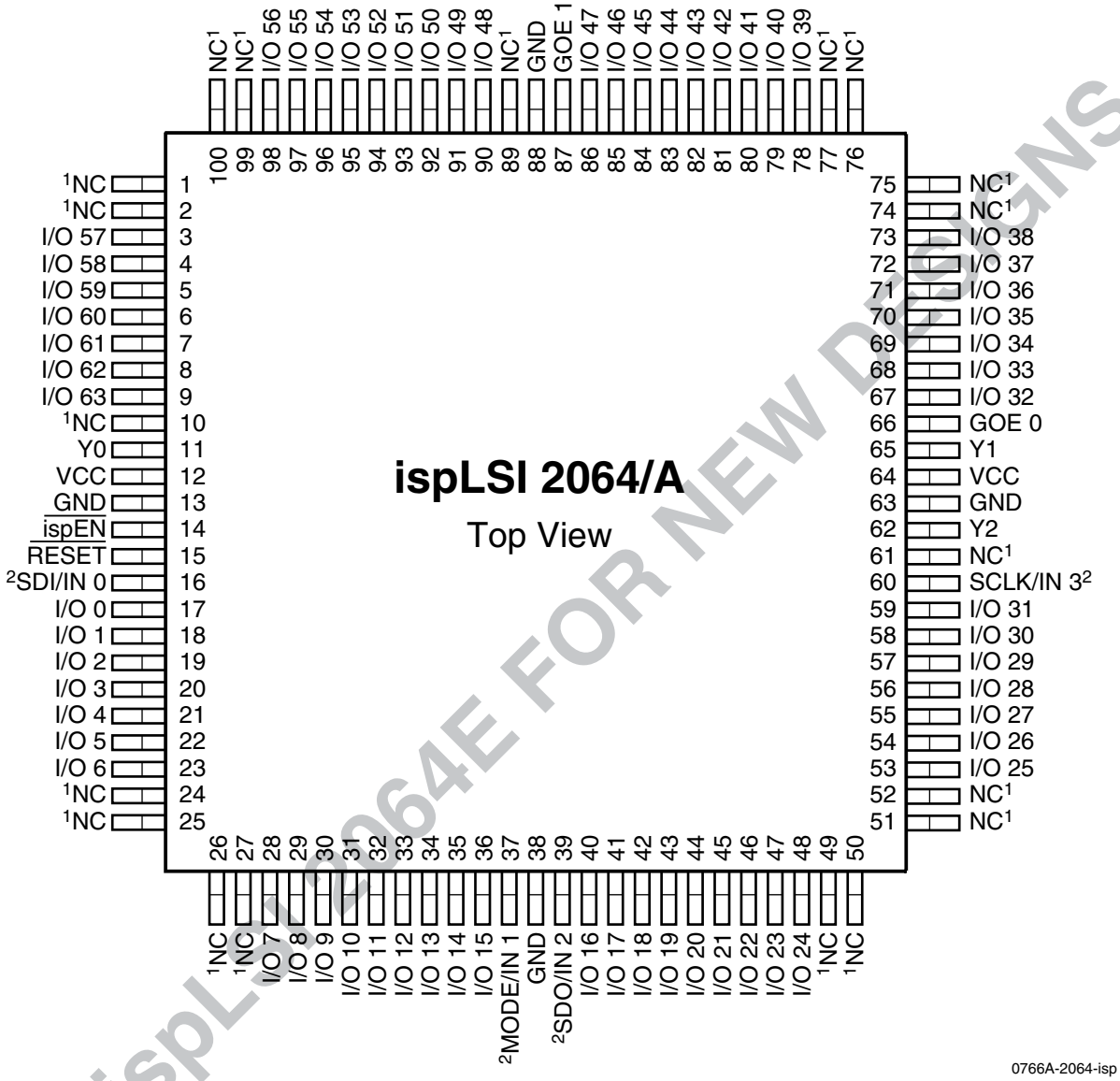


0123A/2064

1. NC pins are not to be connected to any active signals, VCC or GND.
2. Pins have dual function capability.

Pin Configuration

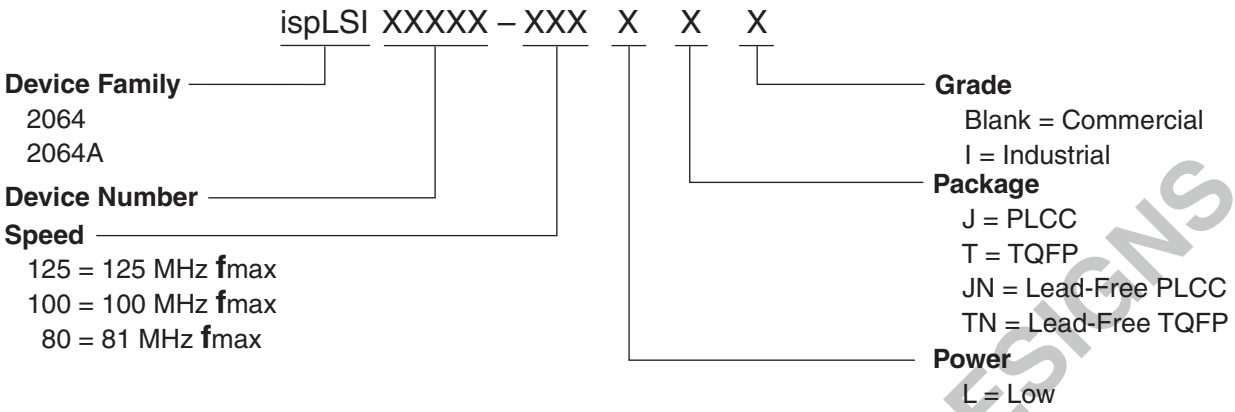
ispLSI 2064/A 100-Pin TQFP Pinout Diagram



0766A-2064-isp

1. NC pins are not to be connected to any active signals, VCC or GND.
2. Pins have dual function capability.

Part Number Description



ispLSI 2064/A Ordering Information

Conventional Packaging

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	125	7.5	ispLSI 2064A-125LJ84	84-Pin PLCC
	125	7.5	ispLSI 2064A-125LT100	100-Pin TQFP
	100	10	ispLSI 2064A-100LJ84	84-Pin PLCC
	100	10	ispLSI 2064A-100LT100	100-Pin TQFP
	81	15	ispLSI 2064A-80LJ84	84-Pin PLCC
	81	15	ispLSI 2064A-80LT100	100-Pin TQFP
	125	7.5	ispLSI 2064-125LJ	84-Pin PLCC
	125	7.5	ispLSI 2064-125LT	100-Pin TQFP
	100	10	ispLSI 2064-100LJ	84-Pin PLCC
	100	10	ispLSI 2064-100LT	100-Pin TQFP
	81	15	ispLSI 2064-80LJ	84-Pin PLCC
	81	15	ispLSI 2064-80LT	100-Pin TQFP

Table 2-0041A/2064A

INDUSTRIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	81	15	ispLSI 2064A-80LJ84I	84-Pin PLCC
	81	15	ispLSI 2064A-80LT100I	100-Pin TQFP
	81	15	ispLSI 2064-80LJI	84-Pin PLCC
	81	15	ispLSI 2064-80LTI	100-Pin TQFP

Table 2-0041B/2064A

ispLSI 2064/A Ordering Information (Cont.)

Lead-Free Packaging

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	125	7.5	ispLSI 2064A-125LJN84[1]	Lead-Free 84-Pin PLCC
	125	7.5	ispLSI 2064A-125LTN100	Lead-Free 100-Pin TQFP
	100	10	ispLSI 2064A-100LJN84[1]	Lead-Free 84-Pin PLCC
	100	10	ispLSI 2064A-100LTN100	Lead-Free 100-Pin TQFP
	81	15	ispLSI 2064A-80LJN84[1]	Lead-Free 84-Pin PLCC
	81	15	ispLSI 2064A-80LTN100	Lead-Free 100-Pin TQFP

1. 84-PLCC lead-free package is MSL4. Refer to “Handling Moisture Sensitive Packages” document on www.latticesemi.com.

INDUSTRIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	81	15	ispLSI 2064A-80LJN84I[1]	Lead-Free 84-Pin PLCC
	81	15	ispLSI 2064A-80LTN100I	Lead-Free 100-Pin TQFP

1. 84-PLCC lead-free package is MSL4. Refer to “Handling Moisture Sensitive Packages” document on www.latticesemi.com.

Revision History

Date	Version	Change Summary
—	09	Previous Lattice release.
August 2006	10	Updated for lead-free package options.