MM5260 1024-bit fully decoded dynamic random access memory

general description

The MM5260 fully decoded dynamic 1024 word x 1-bit word read/write random access memory is a monolithic MOS integrated circuit using silicon gate low threshold technology to achieve bipolar compatibility on all I/O lines except the precharge and read/write lines. This provides an efficient approach to memory design using this systems oriented device. The MM5260 is used for main memory applications where large bit storage and improved operating performance are important. A TRI-STATE™ output is utilized to allow wired "OR" capability and common I/O data busing in memory applications.

features

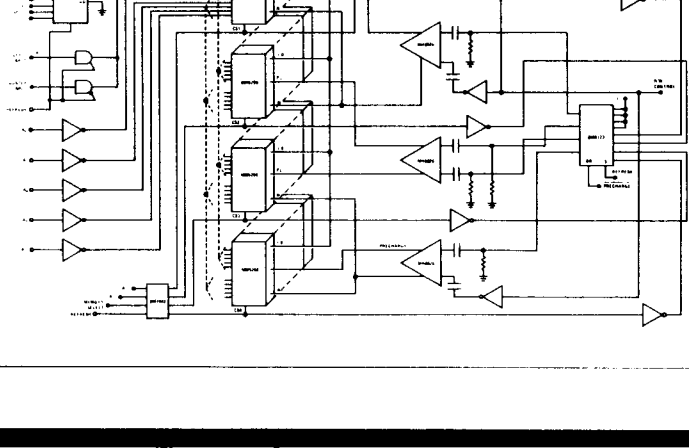
- Fast access time 350 ns
- Fast cycle time 450 ns read cycle min
  600 ns write cycle min
- Low overhead circuit count Fully decoded
- Systems-oriented design Bipolar compatib
  (address lines, ch
  enable data I/
  Common data I/O li
  TRI-STATE outp
- Refresh cycle 2.0 r
- Easy memory expansion Chip enab
- Device protection All I/O lines ha
  protection again
  static char
- Standard power supplies +5V, -12
- Low power dissipation 400 m
- Small package size 16 pin dual-in-line packa

applications

- High speed mainframe memory
- Mass memory storage

typical application

Main Memory Module Storing 4096 16-Bit Words



absolute maximum ratings

All Input or Output Voltages with Respect to Most Positive Supply Voltage V_{SS}	+0.3V to −20V
Power Dissipation	600 mW
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

dc operating characteristics

T_A within operating temperature range, V_{SS} = +5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage (Address input, chip enable and data input)					
Logic "0" (V_{IH})		V_{SS} − 2.0			V
Logic "1" (V_{IL})				V_{SS} − 4.0	V
Input voltage (Precharge and Read/Write)					
Logic "0" (V_{IH})		V_{SS} − 1.5			V
Logic "1" (V_{IL})				V_{SS} − 15	V
Output Voltage Data Output					
Logic "0" (V_{OH})	I_L = 200 μA Source	2.4			V
Logic "1" (V_{OL})	I_L = 1.6 mA Sink			0.4	V
Average Supply Current (I_{DD}) t cycle = 450 ns and t_{pc} = 300 ns			20		mA

ac operating characteristics

T_A within operating temperature range, V_{SS} = +5V ±5V%, V_{DD} = −12V ±5%, unless otherwise noted.

Read Cycle (T_{RC})		450			ns
Write Cycle (T_{WC})		600			ns
Read/Write Cycle (T_{RWC})		(600 + T_D See Note 1)			ns
Access Time (T_A)			350		ns
Address to Chip Enable (T_{AC}) Note 2		0		50	ns
Address to Precharge Delay (T_{APL}) Note 2		0		50	ns
Address to Write Pulse Delay (T_{AWD})		350			ns
Write Pulse Width (T_{WP})		250			ns
Precharge Off Time (T_{PP})		150			ns
Read Write to Precharge Delay (T_{WRP})		50			ns
Refresh Interval (T_{REF})				2	ms
Address to Precharge Trailing Edge (T_{APT})		350			ns

capacitance characteristics

Address Capacitance (C_A)	V_{IN} = V_{SS}	f = 1 MHz All unused inputs are at AC Ground		5	pF
Chip Enable Capacitance (C_{CE})	V_{IN} = V_{SS}			5	pF
Precharge Capacitance (C_{PC})	V_{IN} = V_{SS}			25	pF
Read/Write Capacitance (C_{RW})	V_{IN} = V_{SS}			10	pF
Data Input/Output Capacitance ($C_{IN\ OUT}$)	V_{IN} = V_{SS}			7	pF

Note 1: T_D = Output data to input data delay in read-modify write cycle.

Note 2: Characteristic max limits to achieve T_A specifications. An increase in these times will cause T_A to increase directly.

Channel Matching

Channel matching and crosstalk efficiency are largely dependent on board layout. The layout of National's dual amplifier evaluation boards are optimized to produce maximum channel matching and isolation. Typical channel matching for the CLC417 is shown in Figure 3.

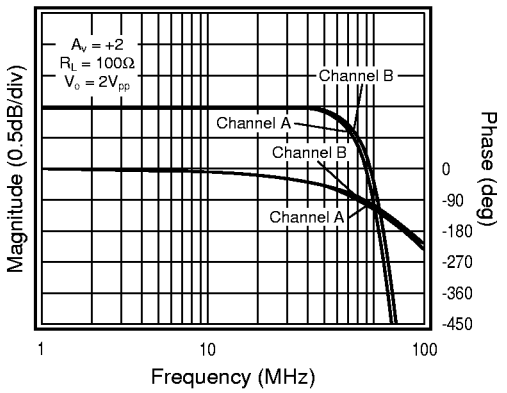


Figure 3: Channel Matching

The CLC417's channel-to-channel isolation is better than 70dB for input frequencies of 4MHz. Input referred crosstalk vs. frequency is illustrated in Figure 4.

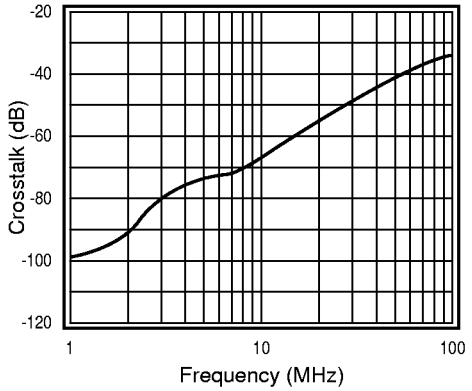


Figure 4: Input Referred Crosstalk vs. Frequency

Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load applications, a small series resistor at the output of the CLC417 will improve stability. The ***R_S vs. Capacitive Load*** plot, in the ***Typical Performance*** section, gives the recommended series resistance value for optimum flatness at various capacitive loads.

Power Dissipation

The power dissipation of an amplifier can be described in two conditions:

- Quiescent Power Dissipation - P_Q (No Load Condition)
- Total Power Dissipation - P_T (with Load Condition)

The following steps can be taken to determine the power consumption for each CLC417 amplifier:

1. Determine the quiescent power
   $P_Q = (V_{CC} - V_{EE}) \cdot I_{CC}$
2. Determine the RMS power at the output stage
   $P_O = (V_{CC} - V_{load})\ (I_{load})$, where V_{load} and I_{load} are the RMS voltage and current across the external load.
3. Determine the total RMS power
   $P_T = P_Q + P_O$

Add the total RMS powers for both channels to determine the power dissipated by the dual.

The maximum power that the package can dissipate at a given temperature is illustrated in the ***Power Derating*** curves in the ***Typical Performance*** section. The power derating curve for any package can be derived by utilizing the following equation:

$$P = \frac{(175° - Tamb)}{\theta_{JA}}$$

where: T_{amb} = Ambient temperature (°C)
θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W)

Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. National provides evaluation boards for the CLC417 (CLC730038 - DIP, CLC730036 - SOIC) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization.

Supply bypassing is required for best performance. The bypass capacitors provide a low impedance return current path at the supply pins. They also provide high frequency filtering on the power supply traces. Other layout factors play a major role in high frequency performance. The following are recommended as a basis for high frequency layout:

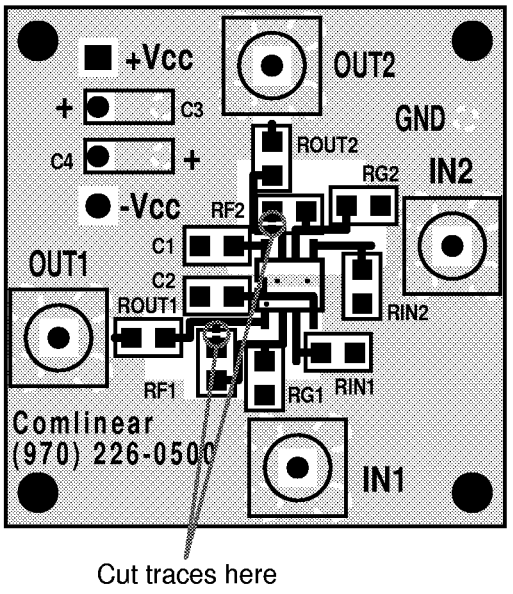
1. Include 6.8µF tantalum and 0.1µF ceramic capacitors on both supplies.
2. Place the 6.8µF capacitors within 0.75 inches of the power pins.
3. Place the 0.1µF capacitors less than 0.1 inches from the power pins.
4. Remove the ground plane near the input and output pins to reduce parasitic capacitance.
5. Minimize all trace lengths to reduce series inductances.

Additional information is included in the evaluation board literature.

Special Evaluation Board Considerations

To optimize off-isolation of the CLC417, cut the R_f trace on both the 730038 and 730036 evaluation boards. This cut minimizes capacitive feedthrough between the input and output. Figure 5 indicates the alterations recommended to improve off-isolation.

730036 Top



730038 Bottom

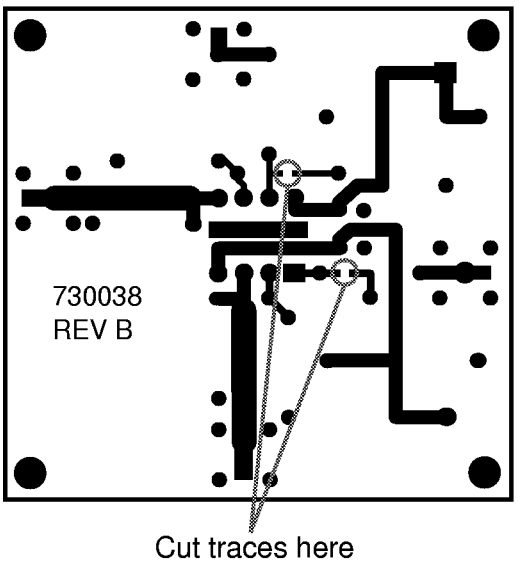


Figure 5: Optional Evaluation Board Alterations

SPICE Models

SPICE models provide a means to evaluate amplifier designs. Free SPICE models are available for National's monolithic amplifiers that:

- Support Berkeley SPICE 2G and its many derivatives
- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The ***readme*** file that accompanies the diskette lists released models, and provides a list of modeled parameters. The application note OA-18, Simulation SPICE Models for National's Op Amps, contains schematics and a reproduction of the ***readme*** file.

Applications Circuits

Video Cable Driver

The CLC417 was designed to produce exceptional video performance at all three closed-loop gains. A typical cable driving configuration is shown in Figure 6. In this example, the amplifier is configured with a gain of 2.

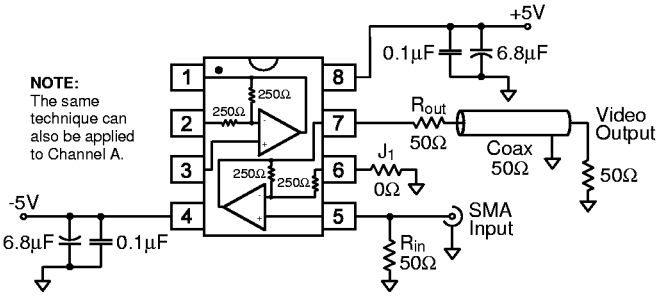


Figure 6: Typical Cable Driver

Single to Differential Line Driver

The topology in Figure 7 accomplishes a single-ended to differential conversion with no external components. With this configuration, the value of Vin is limited to the common mode input range of the CLC417.

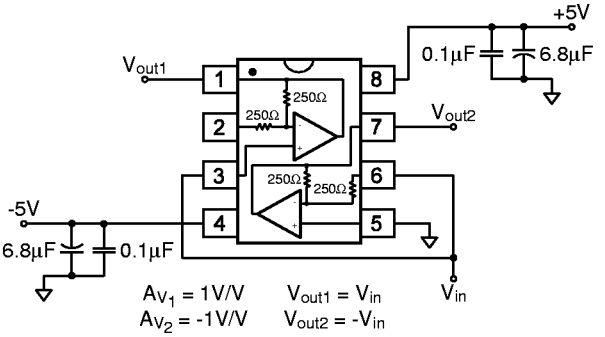


Figure 7: Single to Differential Line Driver