TMS 2147H JL, NL, FPL
FAST 4096-WORD BY 1-BIT STATIC RAM

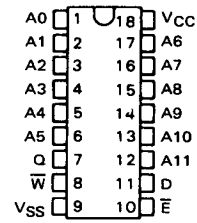
FEBRUARY 1981 – REVISED MAY 1982

- 4096 X 1 Organization
- Single +5 V Supply (±10% Tolerance)
- High-Density 300-mil (7.62 mm) Packages
- Fully Static Operation (No Clocks, No Refresh, No Timing Strobe)
- Fast . . . 4 Performance Ranges:

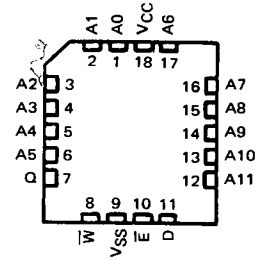
	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 2147H-3	35 ns	35 ns
TMS 2147H-4	45 ns	45 ns
TMS 2147H-5	55 ns	55 ns
TMS 2147H-7	70 ns	70 ns

- Inputs and Outputs TTL Compatible
- Common I/O Capability
- 3-State Outputs and Chip Enable Control for OR-Tie Capability
- Automatic Chip Enable/Power Down Operation
- Reliable SMOS (Scaled-MOS) N-Channel Technology
- Direct Performance Upgrade for Industry Standard 2147

TMS 2147H
18-PIN PLASTIC AND CERAMIC DUAL-IN-LINE PACKAGES
(TOP VIEW)



18-PIN PLASTIC CHIP CARRIER PACKAGE
(TOP VIEW)



PIN NAMES

A0-A11	Addresses
D	Data In
Q	Data Out
$\overline{E}$	Chip Enable/Power Down
V_{CC}	+5 V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

These high-speed static random-access memories are organized as 4096 words of 1 bit. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. Automatic chip enable/power down allows devices to be placed in the reduced-power mode whenever deselected.

All inputs and outputs are fully compatible with Series 74, 74S or 74LS TTL. No pull-up resistors are required. These 4K static RAM series are manufactured using TI's reliable state-of-the-art SMOS (scaled MOS) N-channel silicon-gate technology to optimize the cost/performance relationship.

The TMS 2147H is offered in 18-pin dual-in-line plastic (NL suffix) and ceramic (JL suffix) packages designed for insertion in mounting-hole rows on 300-mil (7.62 mm) centers. An 18-pin plastic chip carrier (FP suffix) is also available. The series is guaranteed for operation from 0°C to 70°C.

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operation

addresses (A0-A11)

The 12 address inputs select one of the 4096 storage locations in the RAM. The address inputs must be stable for the duration of a write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip enable/power down ($\overline{E}$)

The chip enable/power down terminal, which can be driven directly by standard TTL circuits, affects the data-in and data-out terminals and the internal functioning of the chip itself. Whenever the chip enable/power down is low (enabled), the device is operational, input and output terminals are enabled, and data can be read or written. When the chip enable/power down terminal is high (disabled), the device is deselected and put into a reduced-power standby mode. Data is retained during standby.

write-enable ($\overline{W}$)

The read or write mode is selected through the write-enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ must be high when changing addresses to prevent erroneously writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

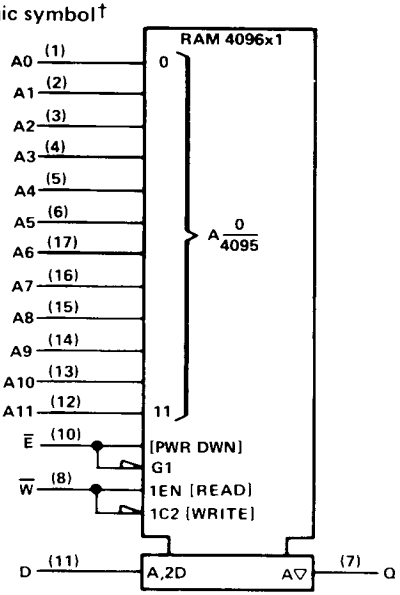
data-in (D)

Data can be written into a selected device when the write-enable input is low. The data-in terminal can be driven directly from standard TTL circuits.

data-out (Q)

The three-state output buffer provides direct TTL compatibility. The output is in the high-impedance state when chip enable/power down ($\overline{E}$) is high or whenever a write operation is being performed, facilitating device operation in common I/O systems. Data-out is the same polarity as data-in.

logic symbol†



FUNCTION TABLE

INPUTS		OUTPUT	MODE
$\overline{E}$	$\overline{W}$	Q	
H	X	Hi-Z	POWER DOWN
L	L	Hi-Z	WRITE
L	H	DATA OUT	READ

† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 289.

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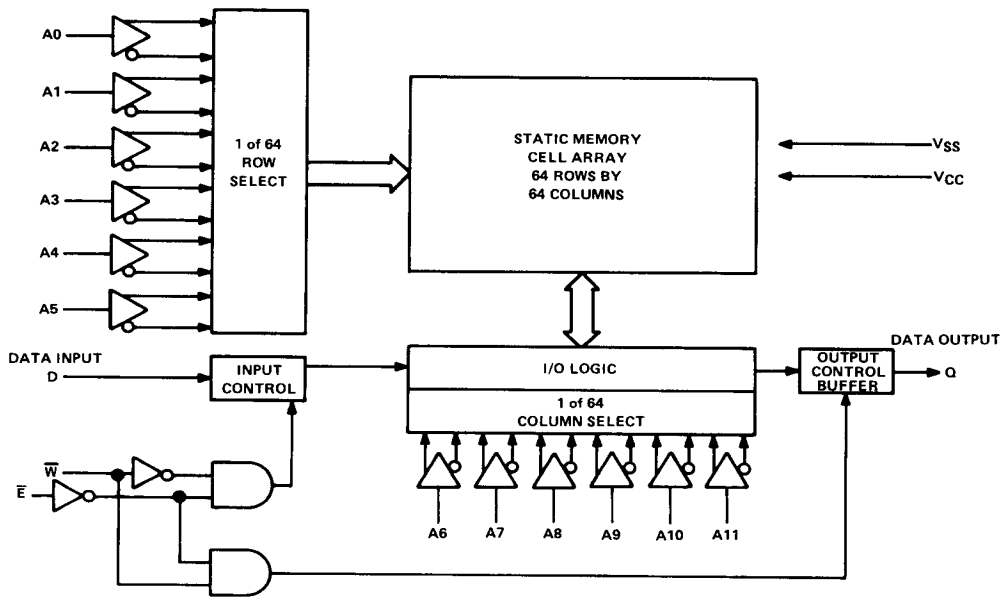
functional block diagram



absolute maximum ratings over operating ambient temperature† range (unless otherwise noted)‡

Supply voltage, V_{CC} (see Note 1)	−1.5 V to 7 V
Input voltage (any input) (see Note 1)	−1.5 V to 7 V
Continuous power dissipation	1 W
Operating ambient temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2		6	V
Low-level input voltage, V_{IL}	−1§		0.8	V
Operating ambient temperature†, T_A	0		70	°C

† The ambient temperature conditions assume air moving perpendicular to the longitudinal axis and parallel to the seating plane of the device at a velocity of 400 ft/min (122 m/min) with the device under test soldered to a 4 X 6 X 0.062-inch (102 X 152 X 1.6-mm) double-sided 2-ounce copper-clad circuit board (plating thickness 0.07 mm).

‡ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

§ The algebraic convention, where the more negative limit is designated as minimum, is used in this data sheet for logic voltage levels only.

NOTE 1: Voltage values are with respect to the ground terminal.

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electrical characteristics over recommended operating ambient temperature† range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −4 mA, V_{CC} = 4.5 V	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA, V_{CC} = 4.5 V			0.4	V
I_I	Input current	V_I = 0 V to 5.5 V			10	μA
I_{OZ}	Off-state output current	$\overline{E}$ at 2 V, V_O = 0 V to 4.5 V, V_{CC} = 5.5 V			±50	μA
I_{CC1}	Standby supply current from V_{CC}	$\overline{E}$ at V_{IH}		18	30	mA
I_{CC2}	Operating supply current from V_{CC}	$\overline{E}$ at V_{IL}, I_O = 0 mA, T_A = 0°C (worst case)		90	120	mA
		$\overline{E}$ at V_{IL}, I_O = 0 mA, T_A = 70°C			100	mA
I_{PO}	Peak power-on current (see Note 2)	V_{CC} = GND to V_{CC} min, $\overline{E}$ at lower of V_{CC} or V_{IH} min			70	mA
C_i	Input capacitance	V_I = 0 V, f = 1 MHz			5	pF
C_O	Output capacitance	V_O = 0 V, f = 1 MHz			6	pF

ac test conditions

Input pulse levels	GND to 3 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output timing reference level (2147H-3)	1.5 V
Output timing reference high level (2147H-4, -5, -7)	2 V
Output timing reference, low level (2147H-4, -5, -7)	0.8 V
Output loading	See Figure 1

timing requirements over recommended supply voltage range and operating ambient temperature† range

PARAMETER		TMS 2147H-3		TMS 2147H-4		TMS 2147H-5		TMS 2147H-7		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	35		45		55		70		ns
$t_{c(wr)}$	Write cycle time	35		45		55		70		ns
$t_{w(W)}$	Write pulse width	20		25		25		40		ns
$t_{su(A)}$	Address setup time	0		0		0		0		ns
$t_{su(E)}$	Chip enable setup time	35		45		45		55		ns
$t_{su(D)}$	Data setup time	20		25		25		30		ns
$t_{h(D)}$	Data hold time	10		10		10		10		ns
$t_{h(A)}$	Address hold time	0		0		10		15		ns
t_{AVWH}	Address valid to write enable high	35		45		45		55		ns

† The ambient temperature conditions assume air moving at a velocity of 400 ft/min (122 m/min).

‡ All typical values are at V_{CC} = 5, T_A = 25°C.

NOTE 2: I_{PO} exceeds I_{CC1} maximum during power on. A pull-up resistor to V_{CC} on the $\overline{E}$ input is required to keep the device deselecte otherwise, power-on current approaches I_{CC2}.

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switching characteristics over recommended supply voltage range and operating ambient temperature† range

PARAMETER		TEST CONDITIONS	TMS 2147H-3		TMS 2147H-4		TMS 2147H-5		TMS 2147H-7		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	R_L = 510 Ω, C_L = 30 pF, See Figure 1		35		45		55		70	ns
$t_{a(E)}$	Access time from chip enable			35		45		55		70	ns
$t_{v(A)}$	Output data valid after address change		5		5		5		5		ns
$t_{dis(W)}$	Output disable time from write enable‡			20		25		25		35	ns
$t_{en(W)}$	Output enable time from write enable‡		0		0		0		0		ns
$t_{dis(E)}$	Output disable time from chip enable‡			30		30		30		40	ns
$t_{en(E)}$	Output enable time from chip enable‡		5		5		10		10		ns
t_{pwrdn}	Power down time from chip select			20		20		20		30	ns

† The ambient temperature conditions assume air moving at a velocity of 400 ft/min (122 m/min).
‡Transition is measured ±500 mV from steady state voltage with specified loading in Figure 1.

PARAMETER MEASUREMENT INFORMATION

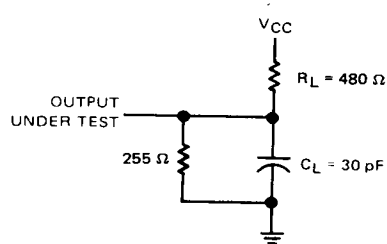
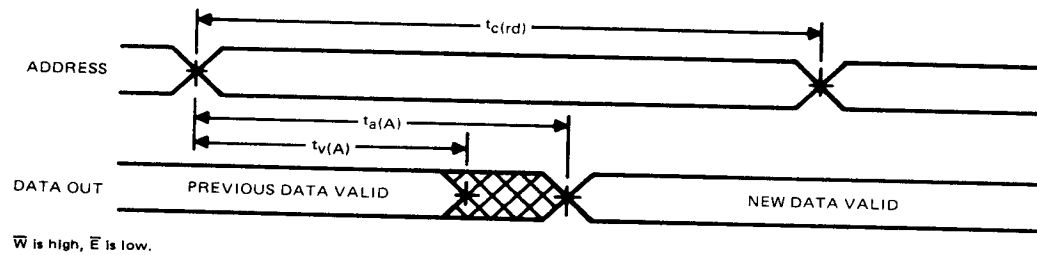


FIGURE 1 – LOAD CIRCUIT

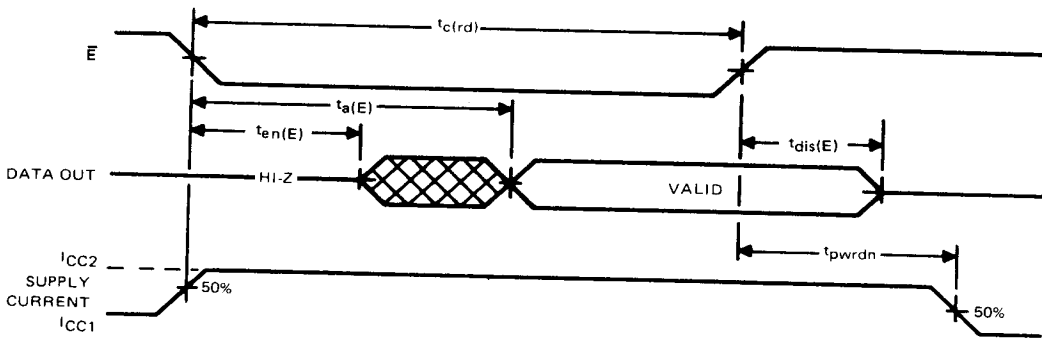
read cycle timing

from address



$\overline{W}$ is high, $\overline{E}$ is low.

from chip select



$\overline{W}$ is high, address is valid prior to or simultaneously with the high-to-low transition of $\overline{E}$.

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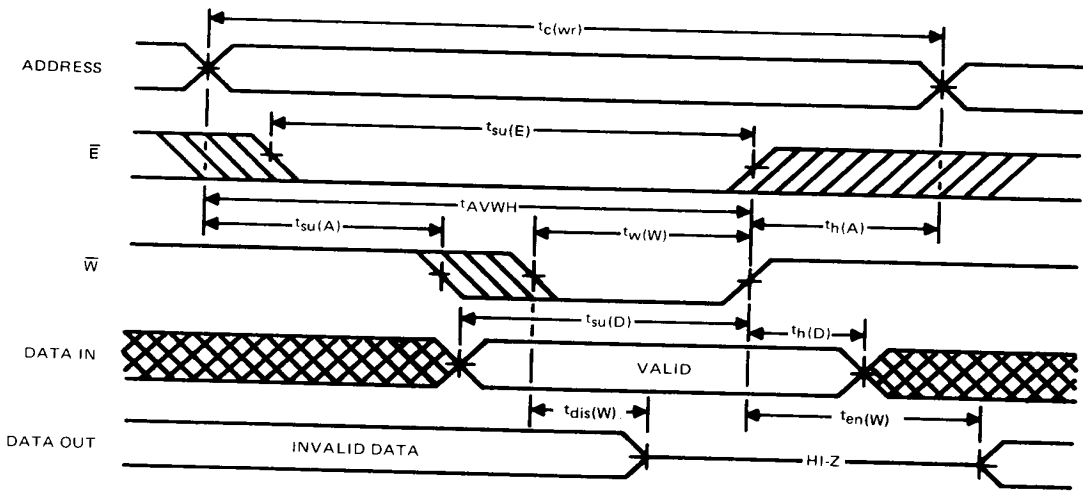
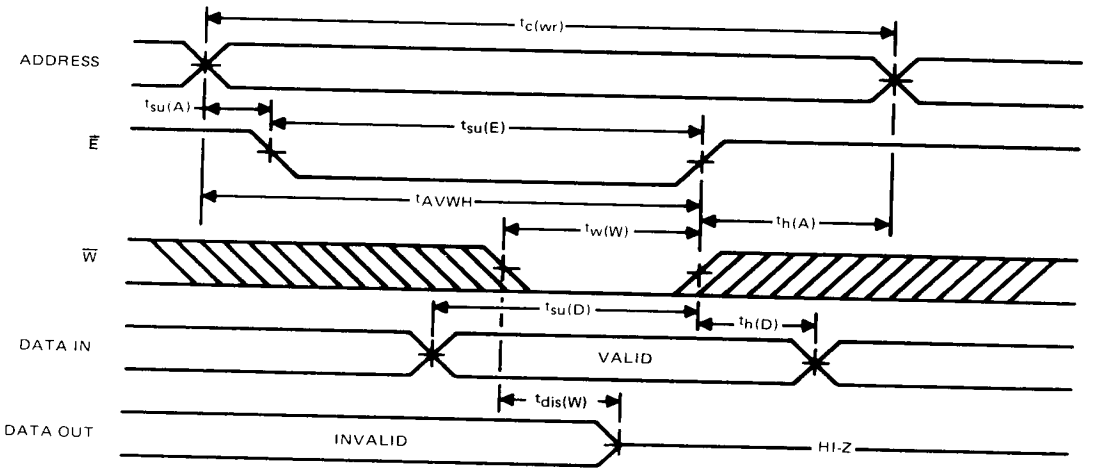
write cycle timing

controlled by write enable†



controlled by chip enable†



†$\overline{E}$ or $\overline{W}$ must be high during address transitions.
NOTE: If $\overline{E}$ goes high simultaneously with $\overline{W}$ going high, the output remains in the high-impedance state.

TYPICAL CHARACTERISTICS

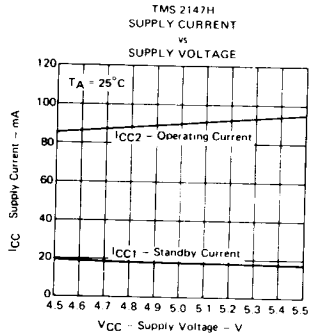


FIGURE 2

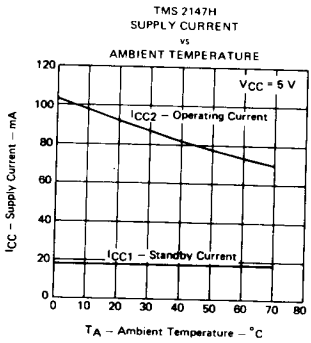


FIGURE 3

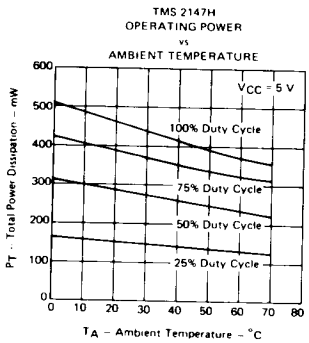


FIGURE 4

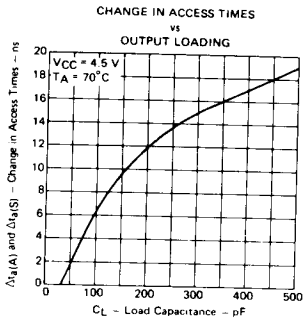


FIGURE 5

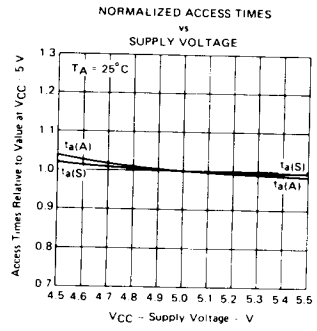


FIGURE 6

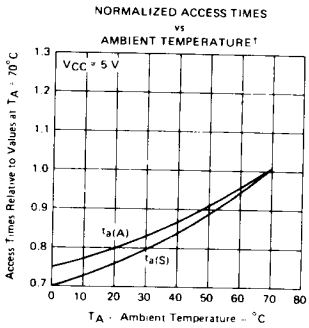


FIGURE 7

† The ambient temperature conditions assume air moving at a velocity of 400 feet per minute.

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