FUJITSU
MICROELECTRONICS

MOS 4096-BIT STATIC RANDOM ACCESS MEMORY

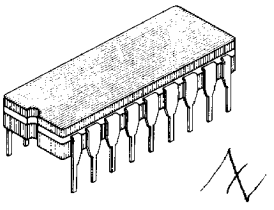
MBM2147H-70
MBM2147H-55
MBM2147H-45
MBM2147H-35

DESCRIPTION

The Fujitsu MBM2147H is a 4096 words by 1 bit static random access memory fabricated using N-channel silicon gate MOS technology. Separate input/output pins are provided. All devices are fully compatabile with TTL logic families in all respects: inputs, outputs and the use of a single +5V DC supply. For ease of use, chip select ($\overline{CS}$) permits the selection of an individual package when outputs are OR-tied, and automatically powers down the MBM2147H. All devices offer the advantage of low power dissipation, low cost and high performance.

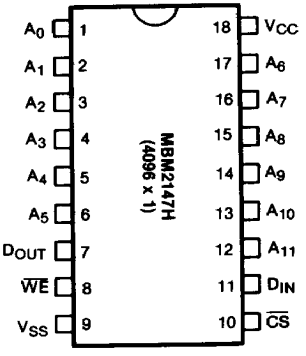
FEATURES

- **Organization: 4096 words X 1 bit**
- **Static operation, no clocks or refresh required**
- **Fast Access Time:**
  - **MBM2147H-70: 70 ns Max**
  - **MBM2147H-55: 55 ns Max**
  - **MBM2147H-45: 45 ns Max**
  - **MBM2147H-35: 35 ns Max**
- **Single +5V DC supply voltage**
- **TTL compatible input/output**
- **3-state output with OR-tie capability**
- **Chip select with automatic power down**
- **Standard 18 pin DIP package**
- **Pin compatible with Intel 2147/2147H**

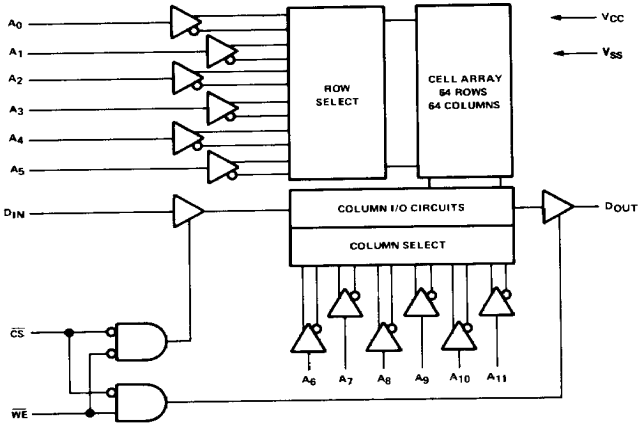


CERDIP PACKAGE
DIP-18C-C01

PIN ASSIGNMENT



MBM2147H BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage On Any Pin with respect to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−3.5 to +7	V
DC Output Current	I_O	20	mA
Temperature Under Bias	T_A	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.2	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
Input Low Voltage	V_{IL}	−3.0	—	0.8	V	
Input High Voltage	V_{IH}	2.0	—	6.0	V	

CAPACITANCE

(T_A = 25°C; f = 1MHz

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	5	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	—	6	pF

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (V_{IN} = V_{SS} to V_{CC}, V_{CC} = Max		I_{LI}	—	10	μA
Output Leakage Current ($\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{CC}, V_{CC} = Max.)		I_{LO}	—	50	μA
Power Supply Current (V_{CC} = Max, $\overline{CS}$ = V_{IL}, I_{OUT} = 0mA)	H-70	I_{CC}	—	160	mA
	H-55/H-45/H-35		—	180	
Output Low Voltage (I_{OL} = 8mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4mA)		V_{OH}	2.4	—	V
Standby Current, (V_{CC} = Max, $\overline{CS}$ = V_{IH}, I_{OUT} = 0mA)	H-70	I_{SB}	—	20	mA
	H-55/H-45/H-35		—	30	
Peak Power-On Current (V_{CC} = V_{SS} to V_{CC} Min, $\overline{CS}$ = Lower of V_{CC} or V_{IN} Min.)	H-70	I_{DO}	—	50	mA
	H-55/H-45/H-35			70	
Output Short Circuit Current		I_{OS}	−200	+200	mA

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AC CHARACTERISTICS

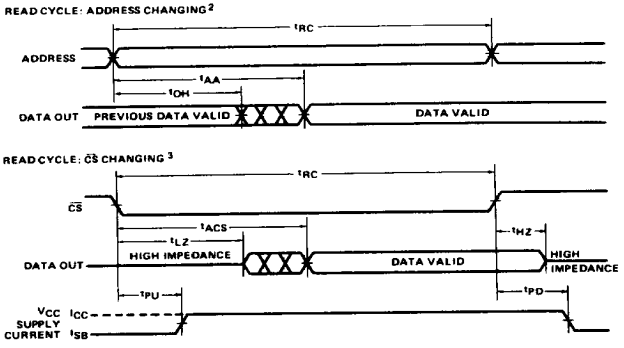
(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Note	Symbol	MBM2147H-70		MBM2147H-55		MBM2147H-45		MBM2147H-35		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time		t_{RC}	70	—	55	—	45	—	35	—	ns
Address Access Time		t_{AA}	—	70	—	55	—	45	—	35	ns
Chip Select Access Time	1	t_{ACS1}	—	70	—	55	—	45	—	35	ns
Chip Select Access Time	2	t_{ACS2}	—	80	—	65		45	—	35	ns
Previous Read Data Valid After Change of Address		t_{OH}	5	—	5	—	5	—	5	—	ns
Chip Select to Power Up		t_{PU}	0	—	0	—	0	—	0	—	ns
Chip Select to Output Active		t_{LZ}	10	—	10	—	5	—	5	—	ns
Chip Select to Output Three-Stated		t_{HZ}	0	40	0	40	0	30	0	30	ns
Chip Select to Power Down		t_{PD}	—	30	—	30	—	20	—	20	ns

Notes: 1) Chip deselected for greater than 55 ns prior to selection.
2) Chip deselected for a finite time that is less than 55 ns prior to selection. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle: Address Changing.)

READ CYCLE[1]



Notes: 1) $\overline{WE}$ is high for read cycle.
2) Device is continuously selected, $\overline{CS}$ = V_{IL}
3) Addresses valid prior to or coincident with $\overline{CS}$ low transition.

WRITE CYCLE

Parameter	Symbol	MBM2147H-70		MBM2147H-55		MBM2147H-45		MBM2147H-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70	—	55	—	45	—	35	—	ns
Address Valid to End of Write	t_{AW}	55	—	45	—	45	—	35	—	ns
Chip Select to End of Write	t_{CW}	55	—	45	—	45	—	35	—	ns
Data Valid to End of Write	t_{DW}	30	—	25	—	25	—	20	—	ns
Data Hold Time	t_{DH}	10	—	10	—	10	—	10	—	ns
Write Pulse Width	t_{WP}	40	—	35	—	25	—	20	—	ns
Write Recovery Time	t_{WR}	15	—	10	—	0	—	0	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	0	—	ns
Output Active From End of Write	t_{OW}	0	—	0	—	0	—	0	—	ns
Write Enabled to Output Three-State	t_{WZ}	0	35	0	30	0	25	0	20	ns

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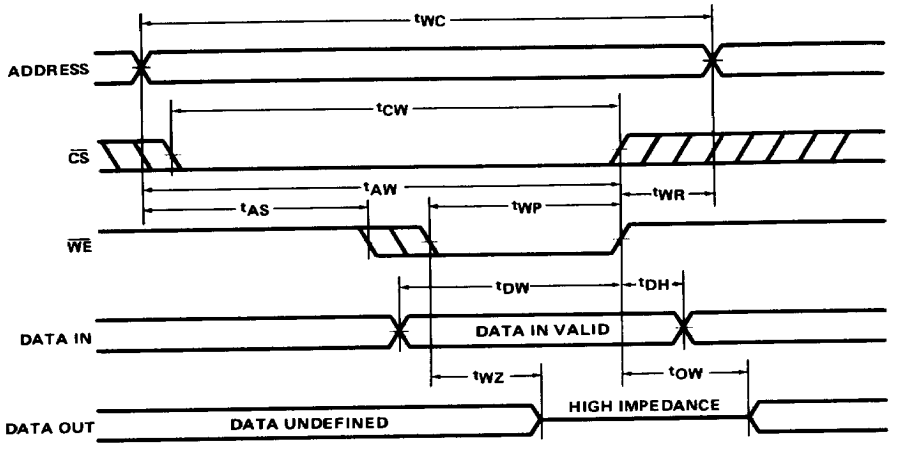
WRITE CYCLE

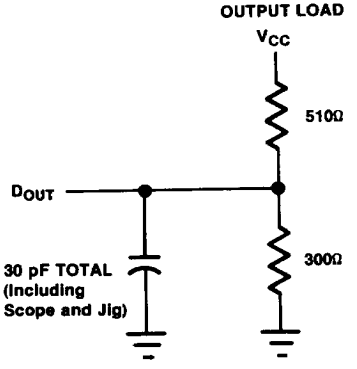


MBM2147H AC TEST CONDITIONS

MBM2147H-70/MBM2147H-55

Input Pulse Levels:	0V to 3.5V
Input Pulse Rise and Fall Times:	10 ns
Timing Measurement Reference Levels:	Inputs: 1.5V Output: 0.8V to 2.0V

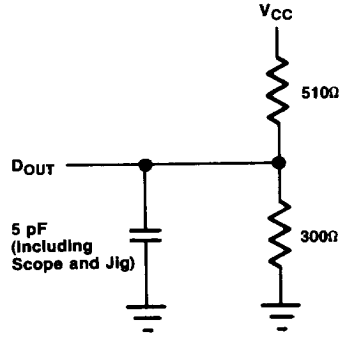
OUTPUT LOAD



MBM2147H-45

Input Pulse Levels:	0V to 3.0V
Input Pulse Rise and Fall Times:	5 ns
Timing Measurement Reference Levels:	Inputs: 1.5V Output: 0.8 to 2.0V

OUTPUT LOAD FOR t_{HZ}, t_{LZ}, t_{WZ} and t_{OW}



MBM2147H-35

Input Pulse Levels:	0V to 3.0V
Input Pulse Rise and Fall Times:	5 ns
Timing Measurement Reference Levels:	Inputs: 1.5V Output: 1.5V

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DESCRIPTION

The MBM2147 family from Fujitsu are high performance parts. They are designed for high speed and low system power requirements.

The high speed is obtained by advanced NMOS processing. The low system power requirements are achieved by the use of the MBM2147's chip select (active low). The MBM2147 automatically enters standby (drawing only I_{SB}) whenever the chip select is high.

Upon activation of chip select ($\overline{CS}$ = LOW) the MBM2147 automatically powers up and draws I_{CC}.

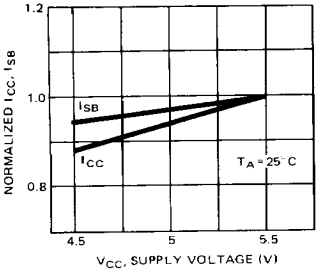
This automatic power up/down is an extremely useful feature. However, care must be used as proper decoupling and PC board layout is required to minimize power line glitches.

PC board layout with proper V_{CC} decoupling will minimize power line glitches.

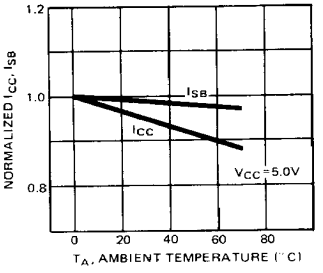
Input and data bus lines are an additional area of concern. Unless bus lines are properly designed and terminated, cross coupling, cross talk and reflections can occur. Of particular importance is the undershoot on address lines. Once again, careful attention to good PC board layout and proper termination techniques will yield a well designed and reliable memory system.

TYPICAL CHARACTERISTICS CURVES

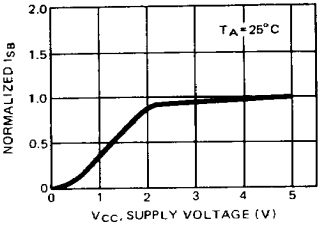
SUPPLY CURRENT vs SUPPLY VOLTAGE



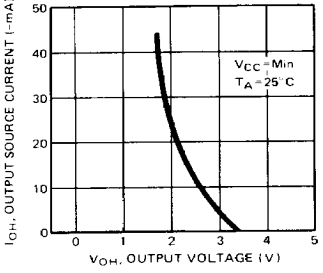
SUPPLY CURRENT vs AMBIENT TEMPERATURE



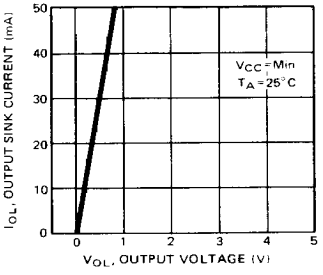
TYPICAL POWER-ON CURRENT vs SUPPLY VOLTAGE



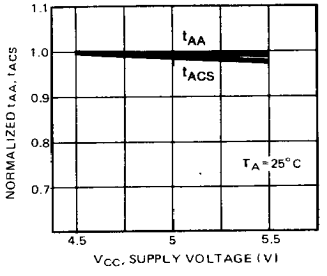
OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE



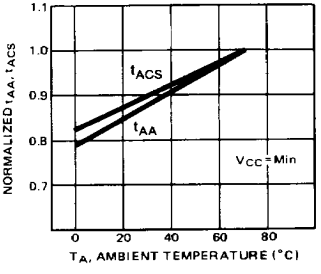
OUTPUT SINK CURRENT vs OUTPUT VOLTAGE



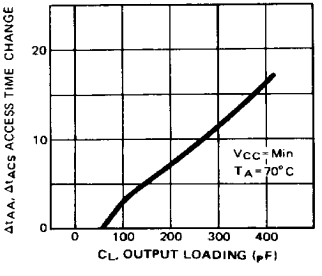
NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE



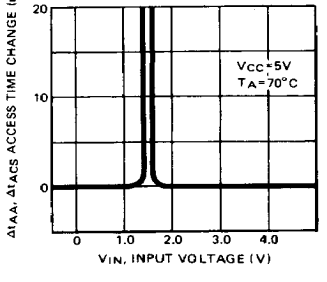
NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE



ACCESS TIME CHANGE vs OUTPUT LOADING



ACCESS TIME CHANGE vs INPUT VOLTAGE



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