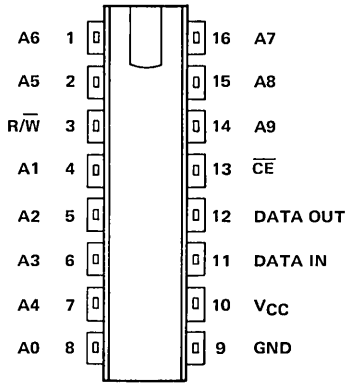
MOS
LSI

TMS 4033 JL, NL; TMS 4034 JL, NL; TMS 4035 JL, NL
1024-WORD BY 1-BIT STATIC RANDOM-ACCESS MEMORIES

BULLETIN NO. DL-S 7512189, OCTOBER 1974—REVISED MAY 1975

- 1024 x 1-Bit Organization
- Static Operation (No Clocks, No Refresh)
- Input Interface
  - Fully Decoded
  - TTL Compatible
  - Static Charge Protection
- Output Interface
  - 3-State
  - Fan-out 1 Series 74 TTL Load
  - OR-Tie Capability
- Access Time
  - TMS 4033 JL, NL . . . 450 ns Max
  - TMS 4034 JL, NL . . . 650 ns Max
  - TMS 4035 JL, NL . . . 1000 ns Max
- Interchangeable with Intel 2102-1, 2102-2, and 2102 Respectively
- N-Channel Silicon-Gate Technology

16-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



3

description

This series is a family of static random-access memories, each organized as 1024 one-bit words. Due to their static design, system overhead costs are minimized by elimination of refresh-clocking circuitry and by simplification of the timing requirements. In addition all inputs and outputs are fully compatible with Series 74 TTL, including the single 5-volt power supply. These memories are fabricated by means of the same technology employed with the TMS 4030 JL, NL 4K RAM — N-channel silicon-gate. This technology provides optimum chip density and performance when cost is considered. Three performance ranges allow the designer to better match the memory to the specific system requirements, thereby maximizing the cost/performance trade-off.

The TMS 4033, TMS 4034, and TMS 4035 are offered in 16-pin dual-in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. These devices are characterized for operation from 0°C to 70°C.

operation

Addresses (A0-A9)

Address inputs are used to select individual storage locations within the RAM. Since the addresses are not latched, the address-valid time determines the cycle time during both the read and write cycle. Therefore, the address-valid time must be a minimum of 450 nanoseconds for the TMS 4033, 650 nanoseconds for the TMS 4034, and 1000 nanoseconds for the TMS 4035. The address inputs can be driven from standard Series 54/74 TTL with no external pull-up resistors.

5

operation (continued)

Chip Enable ($\overline{CE}$)

The $\overline{CE}$ input is used to enable the memory chip for a reading or writing operation. In a single-chip system, this pin can be hardwired to ground so that the chip is continuously enabled. For the read cycle, chip-enable low must extend past the address to ensure valid data for that address. Once the chip-enable goes high, the output buffer will immediately return to the high-impedance state. For the write cycle, chip-enable low must occur before the read/write input goes to the write state ensuring no ambiguity in the chip enabled for a particular write cycle. This input can be driven from Series 54/74 TTL with no external pull-up resistors.

Read/Write (R/$\overline{W}$)

In the write mode prior to an address change, R/$\overline{W}$ must be in the read state (high level) and must remain in that state for a minimum period to eliminate the possibility of data being written into an unwanted location. The read/write input is TTL compatible without external pull-up resistors.

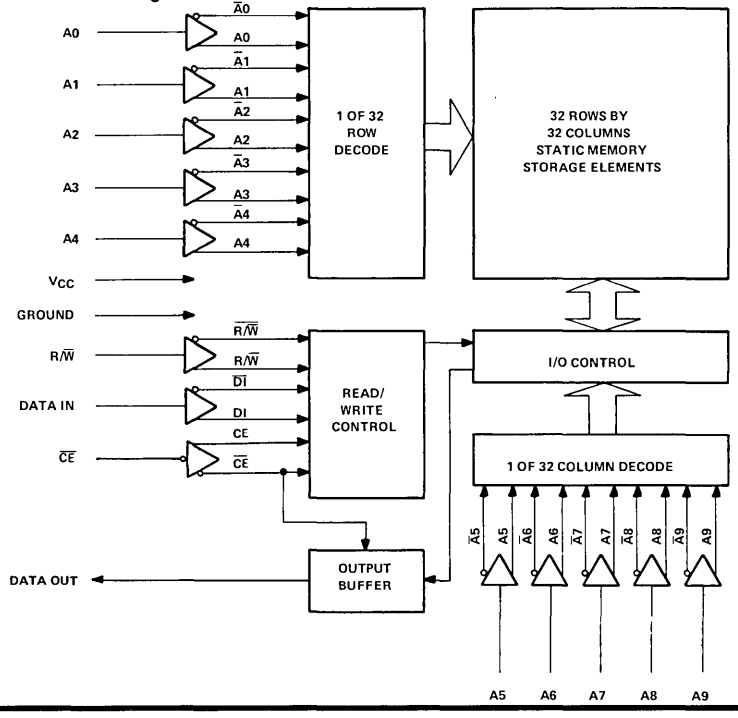
Data In (DI)

The DI input accepts the input data during the write mode. During a write cycle, data must be valid for a minimum time period before the read/write input is brought to the read state ensuring that proper data will enter the location selected. To eliminate any data ambiguity, data must be held valid past the end of the write pulse.

Data Out (DO)

Data out is a three-state terminal controlled by the chip-enable input, which supplies output data during a read cycle. A high level on chip enable places the data-out terminal in the high-impedance state.

functional block diagram



FUNCTION TABLE

$\overline{CE}$	R/$\overline{W}$	I/O
L	L	WRITE
L	H	READ
H	X	HIGH Z

H = HIGH LEVEL
L = LOW LEVEL

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 to 7 V
Input voltage (any input) (see Note 1) . . . . . −0.5 to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the ground terminal.

*COMMENT: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2.2		V_{CC}	V
Low-level input voltage, V_{IL} (see Note 2)	−0.3		0.65	V
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −100 μA,	V_{CC} = 4.75 V	2.2			V
V_{OL}	Low-level output voltage	I_{OL} = 1.9 mA,	V_{CC} = 5.25 V			0.45	V
I_I	Input current	V_I = 0 to 5.25 V				±10	μA
I_{OZH}	Off-state output current, high-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 4 V			10	μA
I_{OZL}	Off-state output current, low-level voltage applied	$\overline{CE}$ at 2.2 V,	V_O = 0.45 V		−10	−100	μA
I_{CC}	Supply current from V_{CC}	V_{CC} = 5.25 V, All inputs at 5.25 V	Data out open,		45	70	mA
C_i	Input capacitance	T_A = 25°C,	f = 1 MHz		3	5	pF
C_o	Output capacitance	T_A = 25°C,	f = 1 MHz		7	10	pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

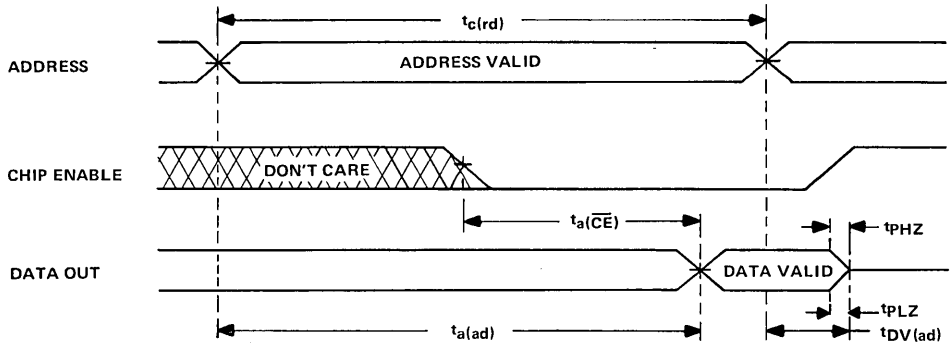
conditions for testing timing requirements

Input high levels . . . . . 2.2 V
Input low levels . . . . . 0.65 V
Input rise and fall times . . . . . 20 ns
Output load . . . . . 1 Series 74 TTL load, C_L = 100 pF
All timing requirements . . . . . 50% point of waveform

read cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C (unless otherwise noted)

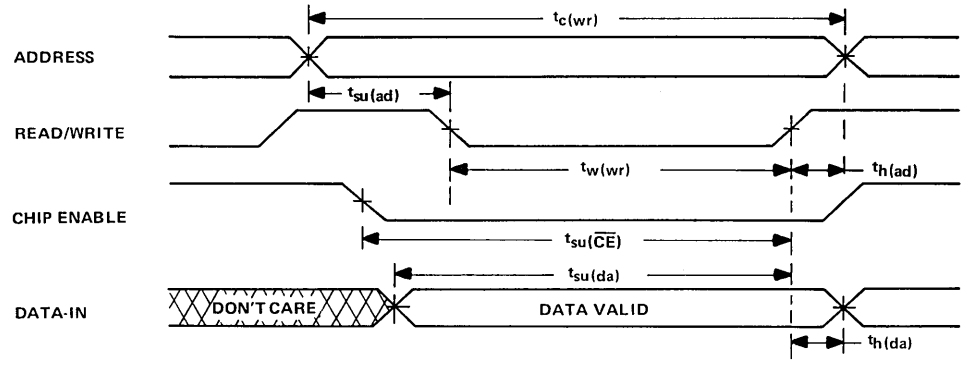
PARAMETER		TMS 4033			TMS 4034			TMS 4035			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{c(rd)}$	Read cycle time	450			650			1000			ns
$t_{a(ad)}$	Access time from address		300	450		450	650		500	1000	ns
$t_{a(\overline{CE})}$	Access time from chip enable			200			300			500	ns
$t_{DV(ad)}$	Previous output data valid from address	50			50			50			ns
t_{PHZ} or t_{PLZ}	Output disable time from chip enable	0		200	0		200	0		200	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.



write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4033		TMS 4034		TMS 4035		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(wr)}$	Write cycle time	450		650		1000		ns
$t_{w(wr)}$	Write pulse width	250		400		750		ns
$t_{su(ad)}$	Address setup time	150		200		200		ns
$t_{su(\overline{CE})}$	Chip enable to write setup time	350		550		850		ns
$t_{su(da)}$	Data-in to write setup time	300		450		800		ns
$t_{h(ad)}$	Address hold time	50		50		50		ns
$t_{h(da)}$	Data hold time	50		50		50		ns



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222