HIGH SPEED FULLY DECODED 64 BIT MEMORY

- **Fast Access Time -- 35 nsec. max. over 0-75° C Temperature Range.** (3101A)
- **Simple Memory Expansion through Chip Select Input -- 17 nsec. max. over 0-75° C Temperature Range.** (3101A)
- **DTL and TTL Compatible -- Low Input Load Current: 0.25mA. max.**
- **OR-Tie Capability -- Open Collector Outputs.**
- **Fully Decoded -- on Chip Address Decode and Buffer.**
- **Minimum Line Reflection -- Low Voltage Diode Input Clamp.**
- **Ceramic and Plastic Package -- 16 Pin Dual In-Line Configuration.**

The Intel 3101 and 3101A are high speed fully decoded 64 bit random access memories, organized 16 words by 4 bits. Their high speed makes them ideal in scratch pad applications. An unselected chip will not generate noise at its output during writing of a selected chip. The output is held high on an unselected chip regardless of the state of the read/write signal.

The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices with gold diffusion processes.

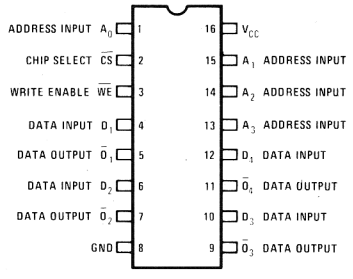
The Intel 3101 and 3101A are packaged in either hermetically sealed 16 pin ceramic packages, or in low cost silicone packages, and their performance is specified over a temperature range from 0° C to 75° C.

The storage cells are addressed through an on chip 1 of 16 binary decoder using four input address leads.

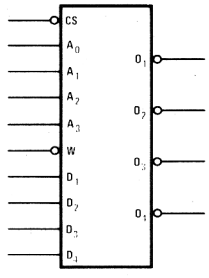
A separate Chip Select lead allows easy selection of an individual package when outputs are OR-tied.

In addition to the address leads and the Chip Select lead, there is a write input which allows data presented at the data leads to be entered at the addressed storage cells.

PIN CONFIGURATION



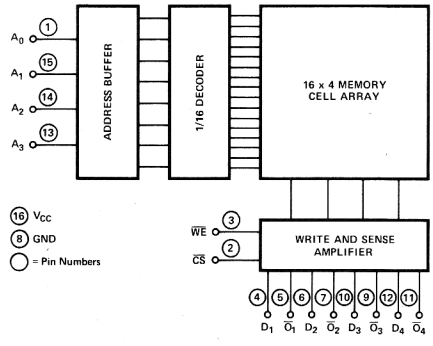
LOGIC SYMBOL



PIN NAMES

D_1–D_4	DATA INPUTS	$\overline{CS}$	CHIP SELECT INPUT
A_0–A_3	ADDRESS INPUTS	$\overline{O}_1$–$\overline{O}_4$	DATA OUTPUTS
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias:	Ceramic	−65°C to +125°C
	Plastic	−65°C to +75°C
Storage Temperature		−65°C to +160°C
All Output or Supply Voltages		−0.5 to +7 Volts
All Input Voltages		−1.0 to +5.5 Volts
Output Currents		100 mA

*COMMENT:

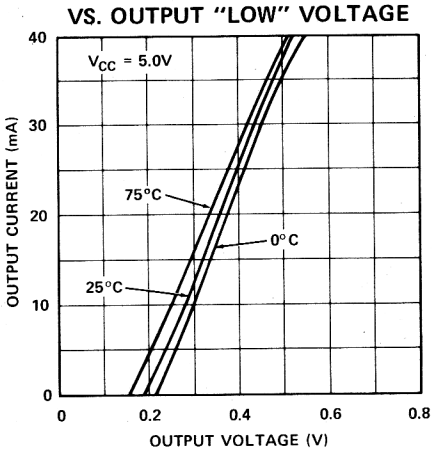
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

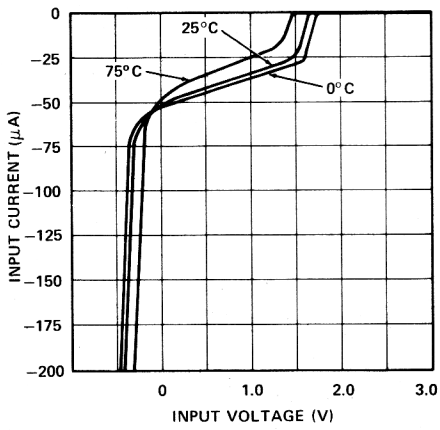
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{FA}	ADDRESS INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_A =0.45V
I_{FD}	DATA INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_D =0.45V
I_{FW}	WRITE INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_W =0.45V
I_{FS}	CHIP SELECT INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_S =0.45V
I_{RA}	ADDRESS INPUT LEAKAGE CURRENT		10	μA	V_{CC} =5.25V, V_A =5.25V
I_{RD}	DATA INPUT LEAKAGE CURRENT		10	μA	V_{CC} =5.25V, V_D =5.25V
I_{RW}	WRITE INPUT LEAKAGE CURRENT		10	μA	V_{CC} =5.25V, V_W =5.25V
I_{RS}	CHIP SELECT INPUT LEAKAGE CURRENT		10	μA	V_{CC} =5.25V, V_S =5.25V
V_{CA}	ADDRESS INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_A =−5.0 mA
V_{CD}	DATA INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_D =−5.0 mA
V_{CW}	WRITE INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_W =−5.0 mA
V_{CS}	CHIP SELECT INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_S =−5.0 mA
V_{OL}	OUTPUT "LOW" VOLTAGE		0.45	V	V_{CC} =4.75V, I_{OL} = 15 mA Memory Stores "Low"
I_{CEX}	OUTPUT LEAKAGE CURRENT		100	μA	V_{CC} =5.25V, V_{CEX} =5.25V V_S =2.5V
I_{CC}	POWER SUPPLY CURRENT		105	mA	V_{CC} =5.25V, V_A =V_S =V_D =0V
V_{IL}	INPUT "LOW" VOLTAGE		0.85	V	V_{CC} =5.0V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	V_{CC} =5.0V

Typical Characteristics

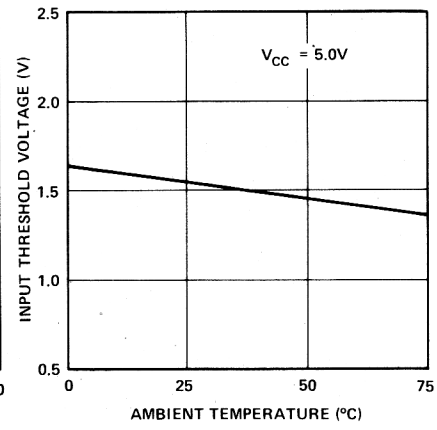
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



INPUT CURRENT VS. INPUT VOLTAGE



INPUT THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE



Switching Characteristics

Conditions of Test:

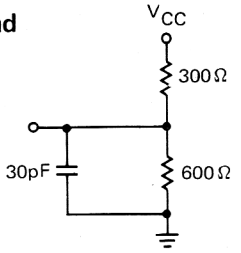
Input Pulse amplitudes: 2.5V

Input Pulse rise and fall times of 5 nanoseconds between 1 volt and 2 volts

Speed measurements are made at 1.5 volt levels

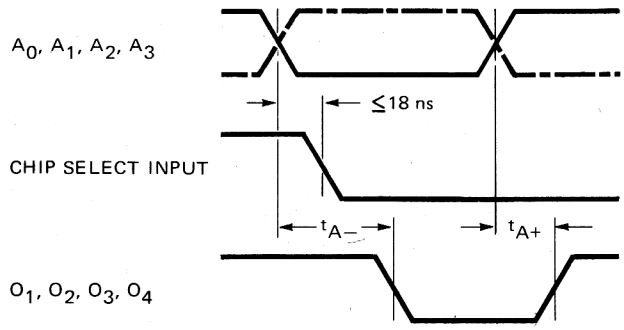
Output loading is 15mA and 30 pF

15 mA Test Load

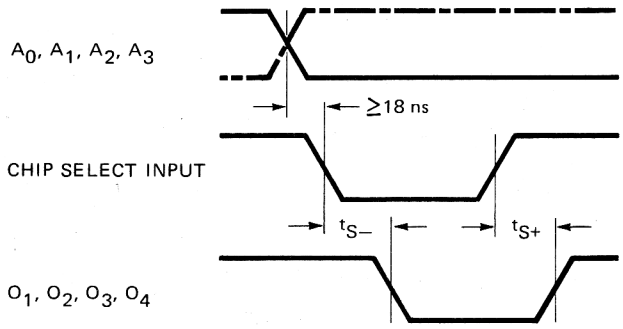


READ CYCLE

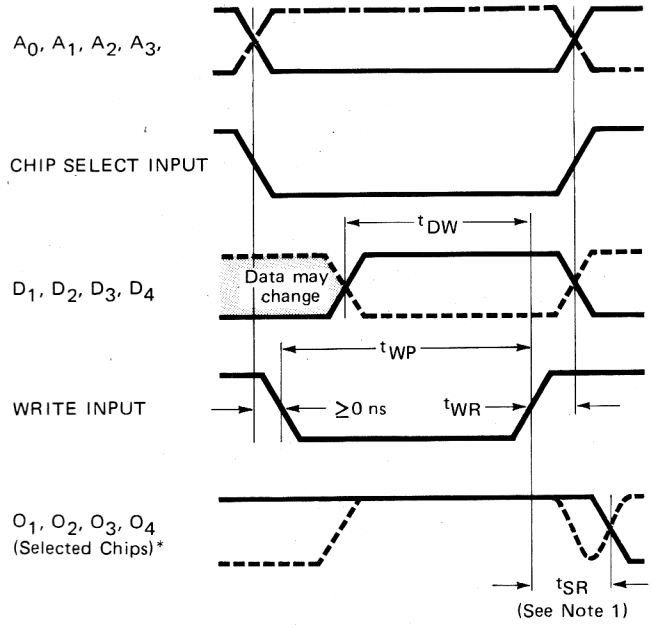
Address to Output Delay



Chip Select to Output Delay



WRITE CYCLE



*Outputs of unselected chips remain high during write cycle.

NOTE 1: t_{SR} is associated with a read cycle following a write cycle and does not affect the access time.

A.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

READ CYCLE					
SYMBOL	PARAMETER	3101A LIMITS (ns)		3101 LIMITS (ns)	
		MIN.	MAX.	MIN.	MAX.
t_{S+}, t_{S-}	Chip Select to Output Delay	5	17	5	42
t_{A-}, t_{A+}	Address to Output Delay	10	35	10	60

WRITE CYCLE					
SYMBOL	TEST	3101A LIMITS (ns)		3101 LIMITS (ns)	
		MIN.	MAX.	MIN.	MAX.
t_{SR}	Sense Amplifier Recovery Time		35		50
t_{WP}	Write Pulse Width	25		40	
t_{DW}	Data-Write Overlap Time	25		40	
t_{WR}	Write Recovery Time	0		5	

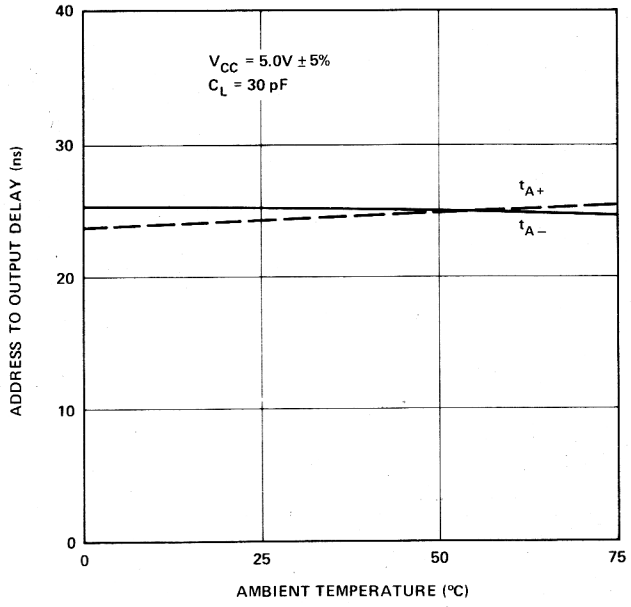
CAPACITANCE(2) T_A = 25° C

C_{IN}	INPUT CAPACITANCE (All Pins)	10 pF maximum
C_{OUT}	OUTPUT CAPACITANCE	12 pF maximum

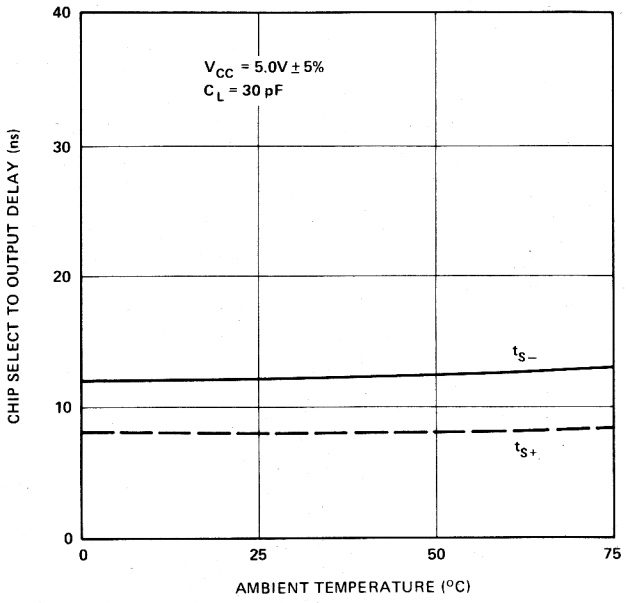
NOTE 2: This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{bias} = 2V, V_{CC} = 0V, and T_A = 25°C.

Typical A.C. Characteristics

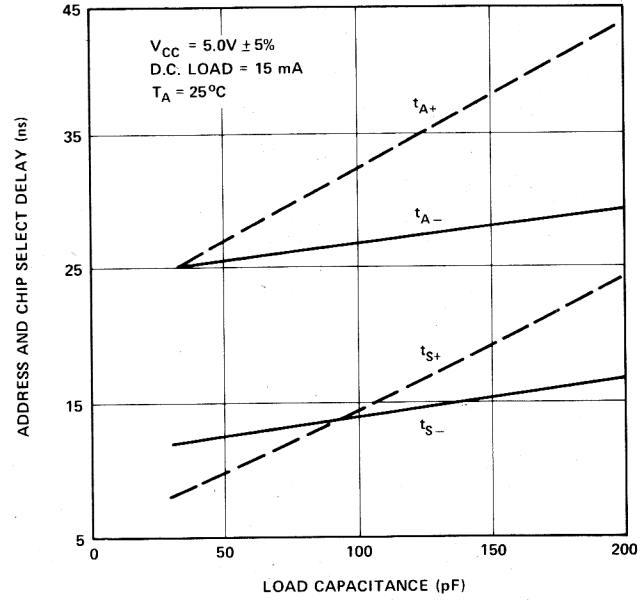
ADDRESS TO OUTPUT DELAY
VS.
AMBIENT TEMPERATURE



CHIP SELECT TO OUTPUT DELAY
VS.
AMBIENT TEMPERATURE



ADDRESS & CHIP SELECT TO OUTPUT DELAY
VS.
LOAD CAPACITANCE



WRITE PULSE WIDTH & SENSE
AMPLIFIER RECOVERY TIME
VS. AMBIENT TEMPERATURE