PYRAMID
SEMICONDUCTOR CORPORATION

P4C164

ULTRA HIGH SPEED 8K X 8 STATIC CMOS RAMS

FEATURES

- **Full CMOS, 6T Cell**
- **High Speed (Equal Access and Cycle Times)**
  - **– 8/10/12/15/20/25/35/70/100 ns (Commercial)**
  - **– 10/12/15/20/25/35/70/100 ns(Industrial)**
  - **– 12/15/20/25/35/45/70/100 ns (Military)**
- **Low Power Operation**
- **Output Enable and Dual Chip Enable Control Functions**
- **Single 5V±10% Power Supply**
- **Data Retention with 2.0V Supply, 10 µA Typical Current (P4C164L Only)**
- **Common Data I/O**
- **Fully TTL Compatible Inputs and Outputs**
- **Standard Pinout (JEDEC Approved)**
  - **– 28-Pin 300 mil Plastic DIP, SOJ**
  - **– 28-Pin 600 mil Plastic DIP**
  - **– 28-Pin 300 mil SOP (70 & 100ns)**
  - **– 28-Pin 300 mil Ceramic DIP**
  - **– 28-Pin 600 mil Ceramic DIP**
  - **– 28-Pin 350 x 550 mil LCC**
  - **– 32-Pin 450 x 550 mil LCC**
  - **– 28-Pin Glass-sealed CERPACK**
  - **– 28-Pin Solder-sealed CERPACK**

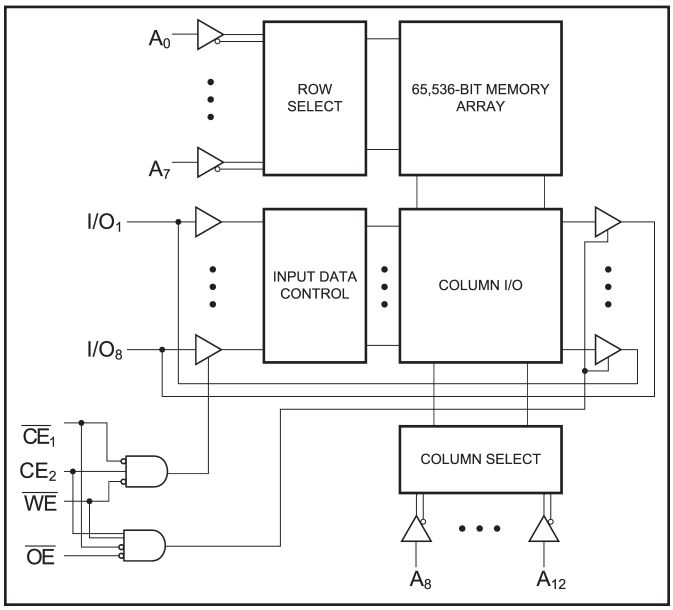
DESCRIPTION

The P4C164 is a 65,536-bit ultra high-speed static RAM organized as 8K x 8. The CMOS memory requires no clocks or refreshing and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5V±10% tolerance power supply. With battery backup (P4C164L Only), data integrity is maintained with supply voltages down to 2.0V. Current drain is typically 10 µA from a 2.0V supply.

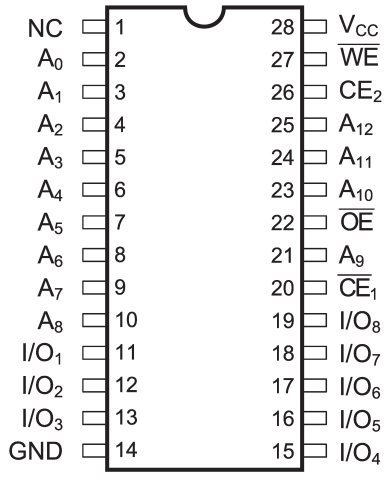
Access times as fast as 8 nanoseconds are available, permitting greatly enhanced system operating speeds.

The P4C164 is available in 28-pin 300 mil DIP and SOJ, 28-pin 600 mil plastic and ceramic DIP, 28-pin 350 x 550 mil LCC, 32-pin 450 x 550 mil LCC, and 28-pin glass-sealed CERPACK and solder-sealed flatpack.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP (P5, P6, C5, C5-1, D5-1, D5-2),
SOJ (J5), CERPACK (F4), SOLDER-SEAL FLATPACK (FS-5), SOP (S6)

SEE PAGE 8 FOR LCC PIN CONFIGURATIONS

MAXIMUM RATINGS[1]

Sym	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	-0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to VCC + 0.5	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

RECOMMENDED OPERATING CONDITIONS

Grade[2]	Ambient Temp	GND	V_{CC}
Commercial	0°C to 70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Sym	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	7	pF

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)[2]

Sym	Parameter	Test Conditions		P4C164 Min	P4C164 Max	P4C164L Min	P4C164L Max	Unit
V_{IH}	Input High Voltage			2.2	V_{CC} + 0.5	2.2	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage			-0.5[3]	0.8	-0.5[3]	0.8	V
V_{HC}	CMOS Input High Voltage			V_{CC} - 0.2	V_{CC} + 0.5	V_{CC} - 0.2	V_{CC} + 0.5	V
V_{LC}	CMOS Input Low Voltage			-0.5[3]	0.2	-0.5[3]	0.2	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min, I_{IN} = -18 mA			-1.2		-1.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +8 mA, V_{CC} = Min			0.4		0.4	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = -4 mA, V_{CC} = Min		2.4		2.4		V
I_{LI}	Input Leakage Current	V_{CC} = Max, V_{IN} = GND to V_{CC}	MIL	-10	+10	-5	+5	µA
			IND/COM	-5	+5	N/A	N/A	
I_{LO}	Output Leakage Current	V_{CC} = Max, $\overline{CE_1}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL	-10	+10	-5	+5	µA
			IND/COM	-5	+5	N/A	N/A	
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE_1}$ ≥ V_{IH} or CE_2 ≤ V_{IL}, V_{CC}=Max, f=Max, Outputs Open	MIL	—	40	—	40	mA
			IND/COM	—	30	—	N/A	
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE_1}$ ≥ V_{HC} or CE_2 ≤ V_{LC}, V_{CC} = Max, f = 0, Outputs Open V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}	MIL	—	25	—	1	mA
			IND/COM	—	15	—	N/A	

N/A = Not applicable

Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.

POWER DISSIPATION CHARACTERISTICS VS. SPEED

Sym	Parameter	Temperature Range	-8	-10	-12	-15	-20	-25	-35	-45	-70	-100	Unit
I_{CC}	Dynamic Operating Current*	Commercial	200	180	170	160	155	150	145	N/A	130	125	mA
		Industrial	N/A	190	180	170	160	155	150	N/A	145	140	mA
		Military	N/A	N/A	180	170	160	155	150	145	145	145	mA

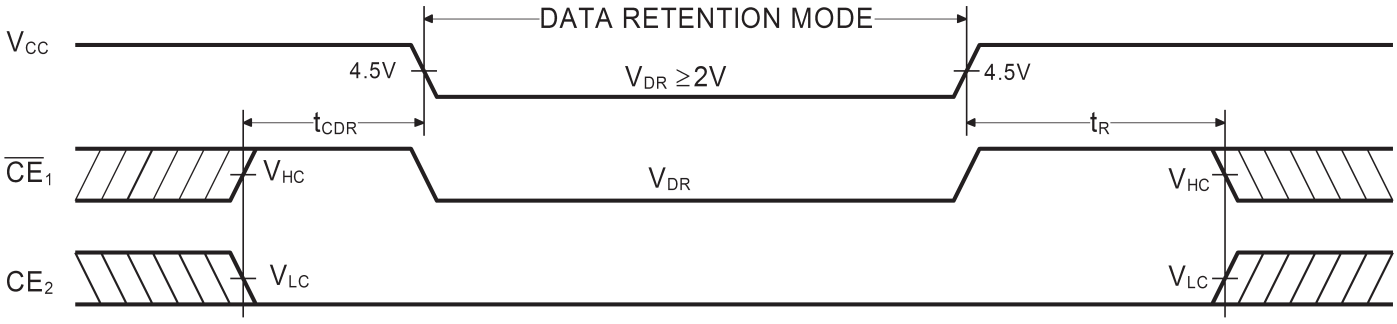
* V_{CC} = 5.5V. Tested with outputs open. f = Max. Switching inputs are 0V and 3V. $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$, $\overline{OE} = V_{IH}$.

DATA RETENTION CHARACTERISTICS (P4C164L Only)

Sym	Parameter	Test Conditions	Min	Typ* V_{cc}=		Max V_{cc}=		Unit
				2.0V	3.0V	2.0V	3.0V	
V_{DR}	V_{CC} for Data Retention		2.0					V
I_{CCDR}	Data Retention Current	$\overline{CE}_1 \geq V_{CC}$ -0.2V or $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$		10	15	200	300	µA
t_{CDR}	Chip Deselect to Data Retention Time		0					ns
t_R†	Operation Recovery Time		t_{RC}§					ns

* T_A = +25°C
§ t_{RC} = Read Cycle Time
† This Parameter is guaranteed but not tested

DATA RETENTION WAVEFORM



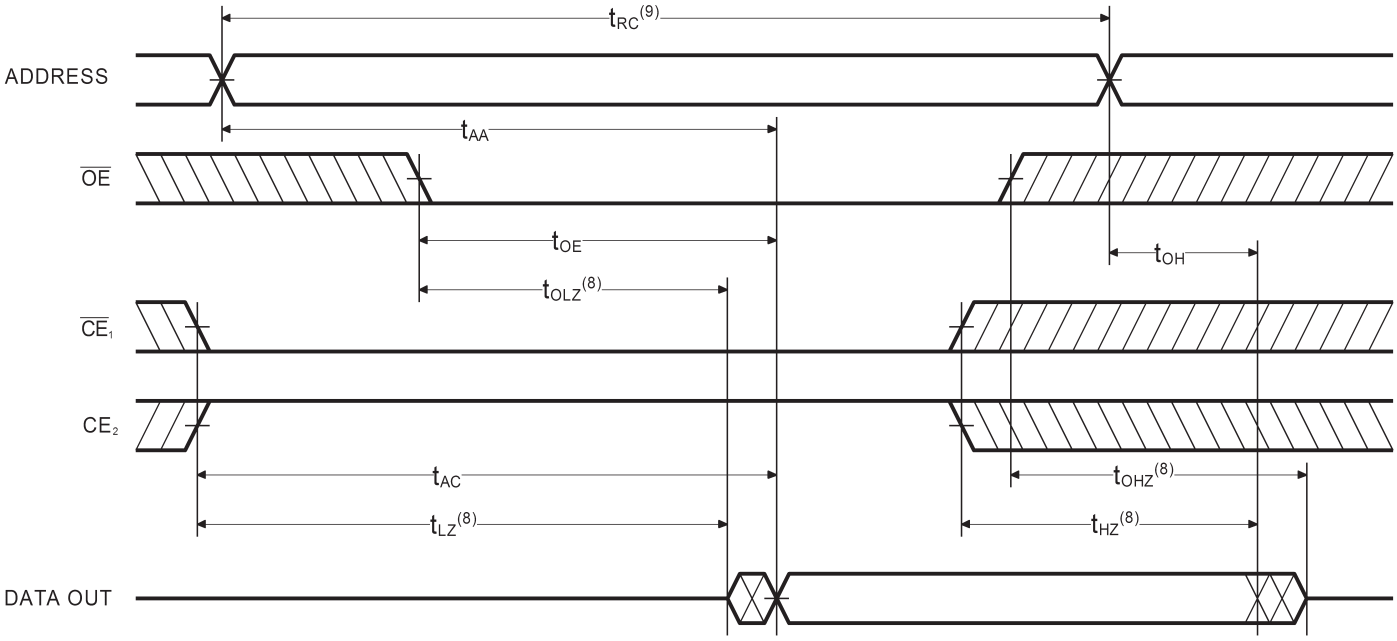
AC ELECTRICAL CHARACTERISTICS—READ CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

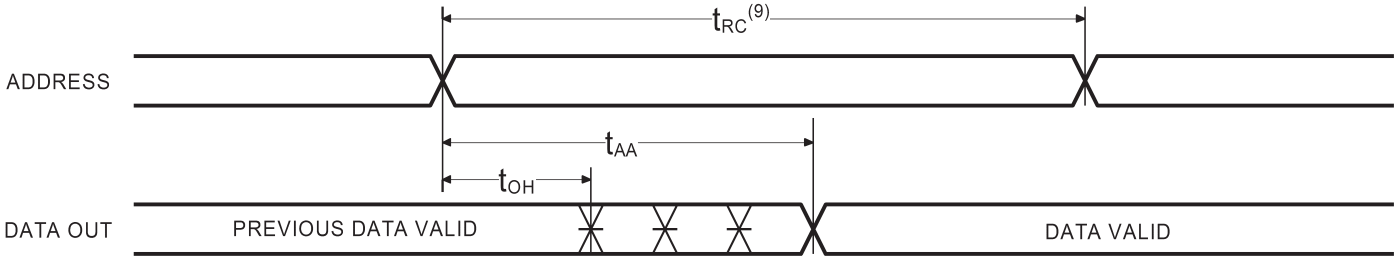
Sym	Parameter	-8		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	8		10		12		15		20		ns
t_{AA}	Address Access Time		8		10		12		15		20	ns
t_{AC}	Chip Enable Access Time		8		10		12		15		20	ns
t_{OH}	Output Hold from Address Change	3		3		3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	2		2		2		2		2		ns
t_{HZ}	Chip Disable to Output in High Z		5		6		7		8		8	ns
t_{OE}	Output Enable Low to Data Valid		5		6		7		9		10	ns
t_{OLZ}	Output Enable Low to Low Z	2		2		2		2		2		ns
t_{OHZ}	Output Enable High to High Z		5		6		7		9		9	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		8		10		12		15		20	ns

Sym	Parameter	-25		-35		-45		-70		-100		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	25		35		45		70		100		ns
t_{AA}	Address Access Time		25		35		45		70		100	ns
t_{AC}	Chip Enable Access Time		25		35		45		70		100	ns
t_{OH}	Output Hold from Address Change	3		3		3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	2		2		2		2		2		ns
t_{HZ}	Chip Disable to Output in High Z		10		15		20		35		45	ns
t_{OE}	Output Enable Low to Data Valid		13		18		20		35		45	ns
t_{OLZ}	Output Enable Low to Low Z	2		2		2		2		2		ns
t_{OHZ}	Output Enable High to High Z		12		15		20		35		45	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		20		20		25		35		45	ns

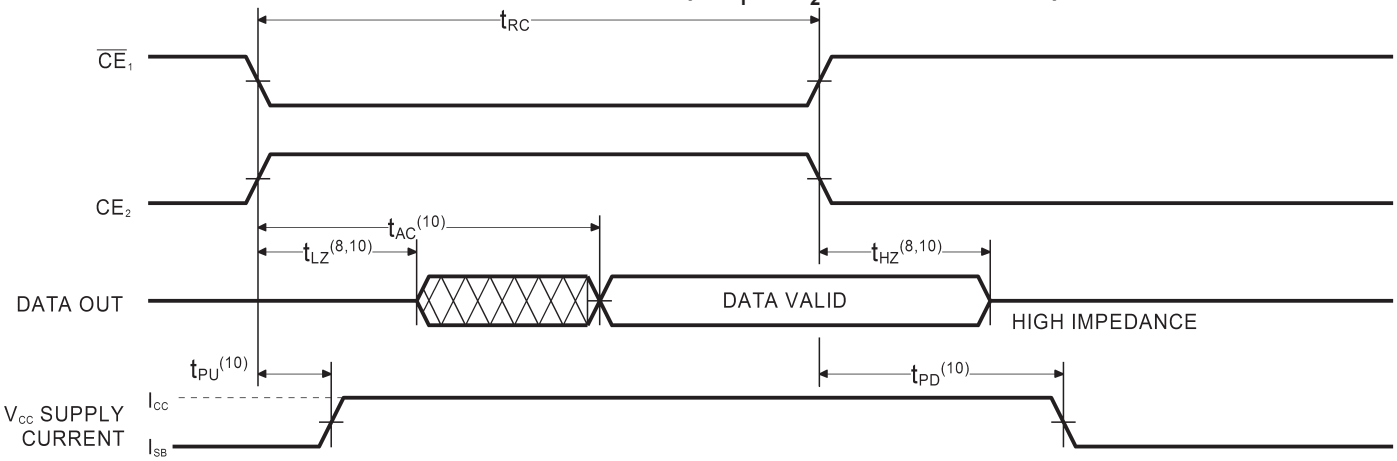
TIMING WAVEFORM OF READ CYCLE NO. 1 ($\overline{OE}$ CONTROLLED)[5]



TIMING WAVEFORM OF READ CYCLE NO. 2 (ADDRESS CONTROLLED)[5,6]



TIMING WAVEFORM OF READ CYCLE NO. 3 ($\overline{CE}_1$, CE_2 CONTROLLED)[5,7,10]



5. $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{OE}$ is LOW for READ cycle.
7. ADDRESS must be valid prior to, or coincident with $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.
8. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
9. Read Cycle Time is measured from the last valid address to the first transitioning address.
10. Transitions caused by a chip enable control have similar delays irrespective of whether $\overline{CE}_1$ or CE_2 causes them.

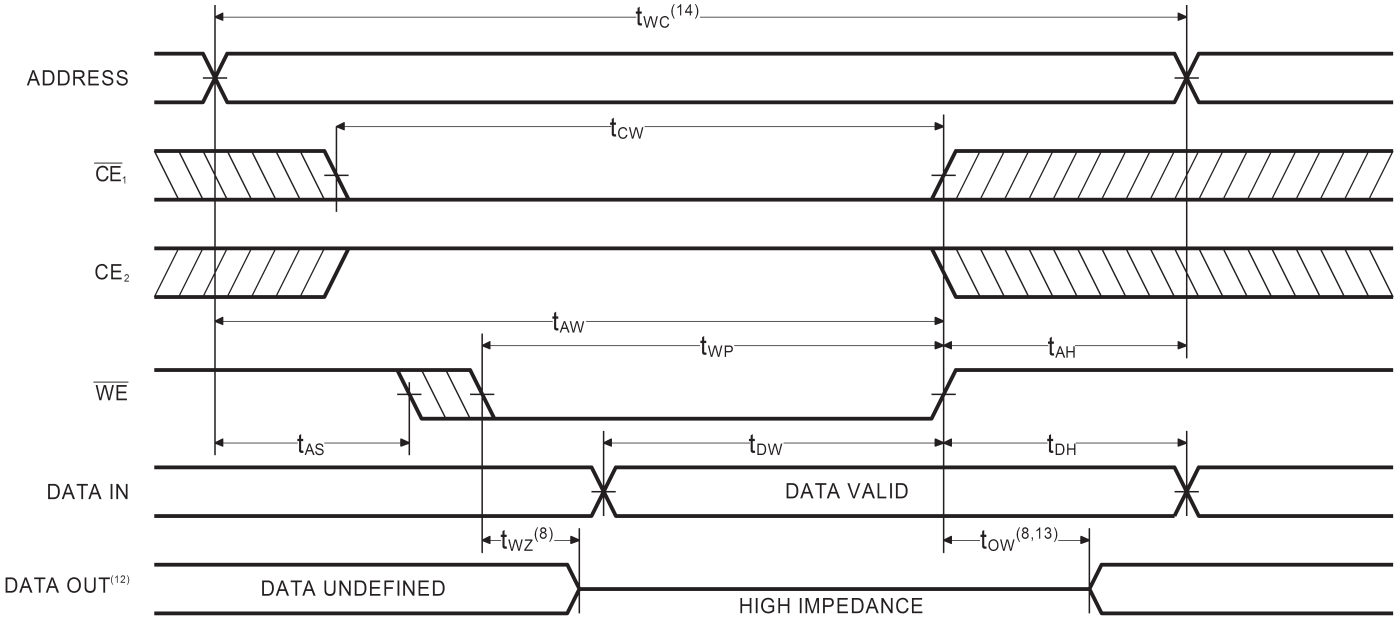
AC CHARACTERISTICS—WRITE CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

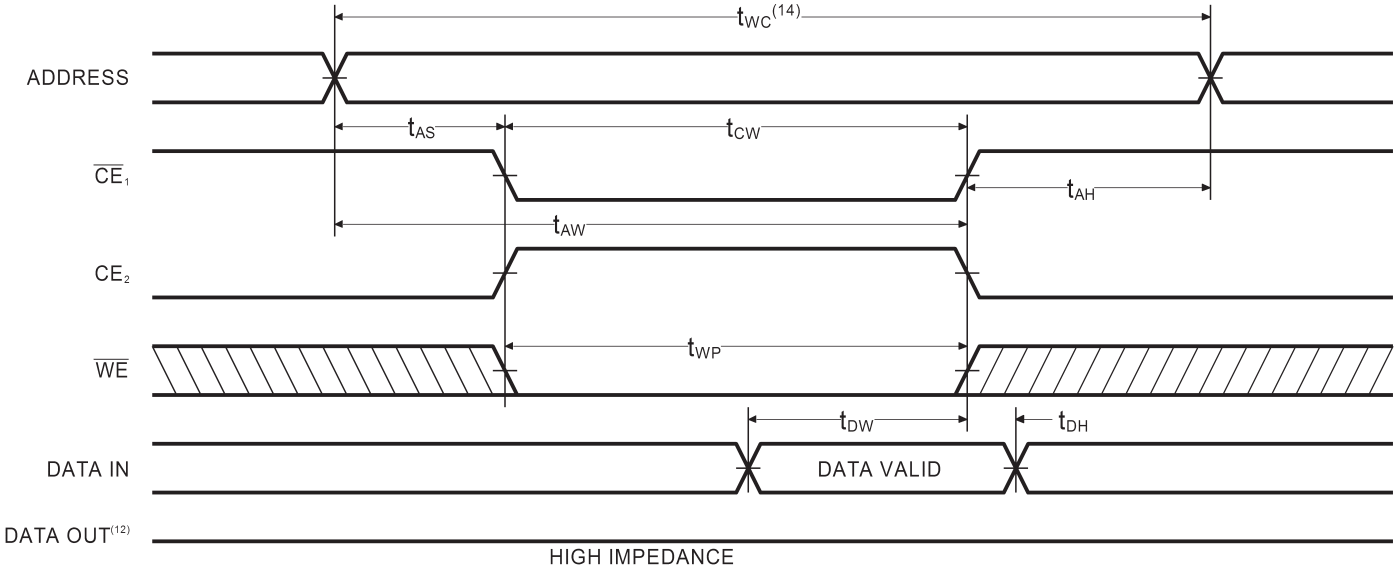
Sym	Parameter	-8		-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	8		10		12		15		20		ns
t_{CW}	Chip Enable Time to End of Write	6		7		8		12		15		ns
t_{AW}	Address Valid to End of Write	7		8		10		12		15		ns
t_{AS}	Address Setup Time	0		0		0		0		0		ns
t_{WP}	Write Pulse Width	7		8		9		12		15		ns
t_{AH}	Address Hold Time	0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	6		7		8		9		11		ns
t_{DH}	Data Hold Time	0		0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		6		7		7		7		8	ns
t_{OW}	Output Active from End of Write	3		3		3		3		3		ns

Sym	Parameter	-25		-35		-45		-70		-100		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	25		35		45		70		100		ns
t_{CW}	Chip Enable Time to End of Write	18		25		33		50		70		ns
t_{AW}	Address Valid to End of Write	18		25		33		50		70		ns
t_{AS}	Address Setup Time	0		0		0		0		0		ns
t_{WP}	Write Pulse Width	18		20		25		40		50		ns
t_{AH}	Address Hold Time	0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	13		15		20		30		40		ns
t_{DH}	Data Hold Time	0		0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		10		14		18		30		40	ns
t_{OW}	Output Active from End of Write	3		3		3		3		3		ns

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[11]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)[11]



Notes:
11. $\overline{CE}$ and $\overline{WE}$ must be LOW, and CE_2 HIGH for WRITE cycle.
12. $\overline{OE}$ is LOW for this WRITE cycle to show t_{WZ} and t_{OW}.
13. If $\overline{CE_1}$ goes HIGH, or CE_2 goes LOW, simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state
14. Write Cycle Time is measured from the last valid address to the first transitioning address.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE

Mode	$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	L	X	X	High Z	Standby
D_{OUT} Disabled	L	H	H	H	High Z	Active
Read	L	H	L	H	D_{OUT}	Active
Write	L	H	X	L	High Z	Active

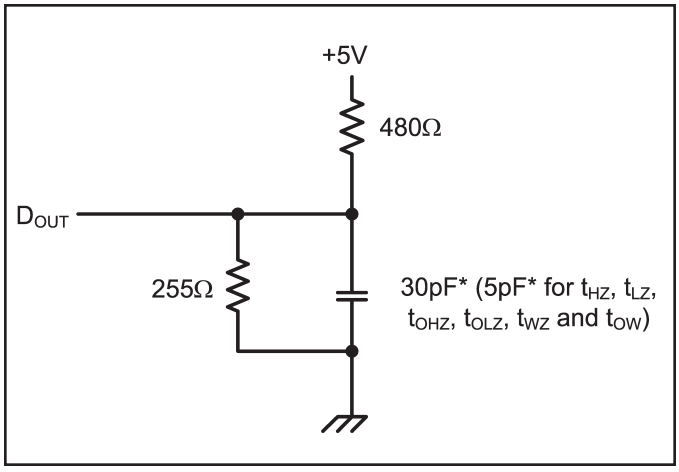


Figure 1. Output Load

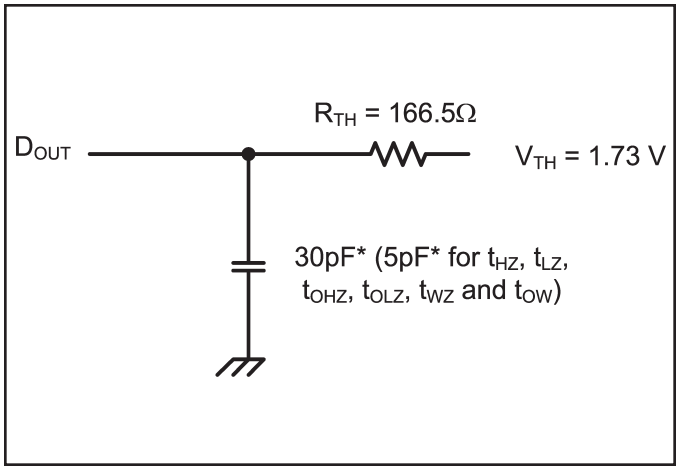
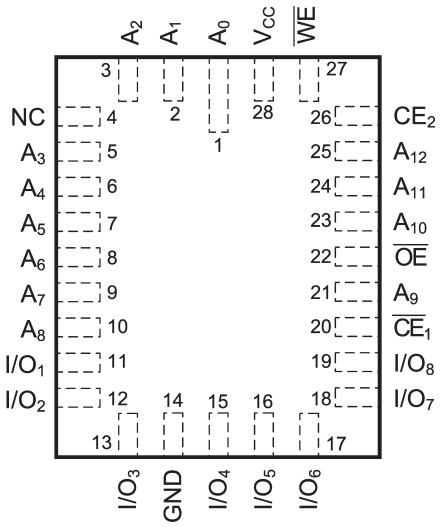


Figure 2. Thevenin Equivalent

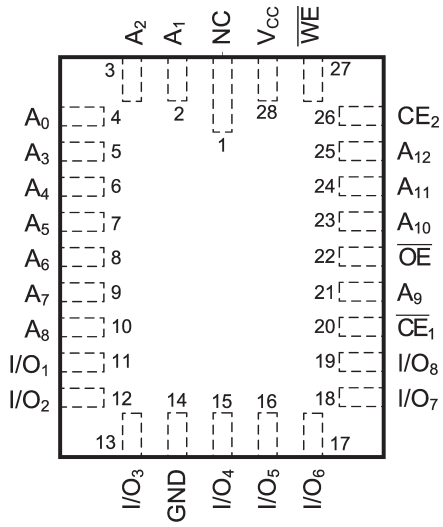
* including scope and test fixture.

Note:
Because of the high speed of the P4C164/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

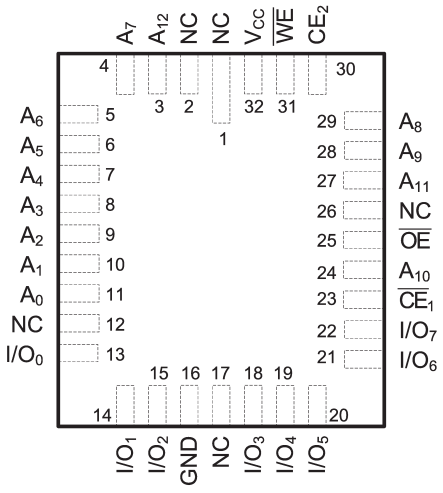
LCC PIN CONFIGURATIONS



LCC (L5)
"L" - STANDARD PIN-OUT

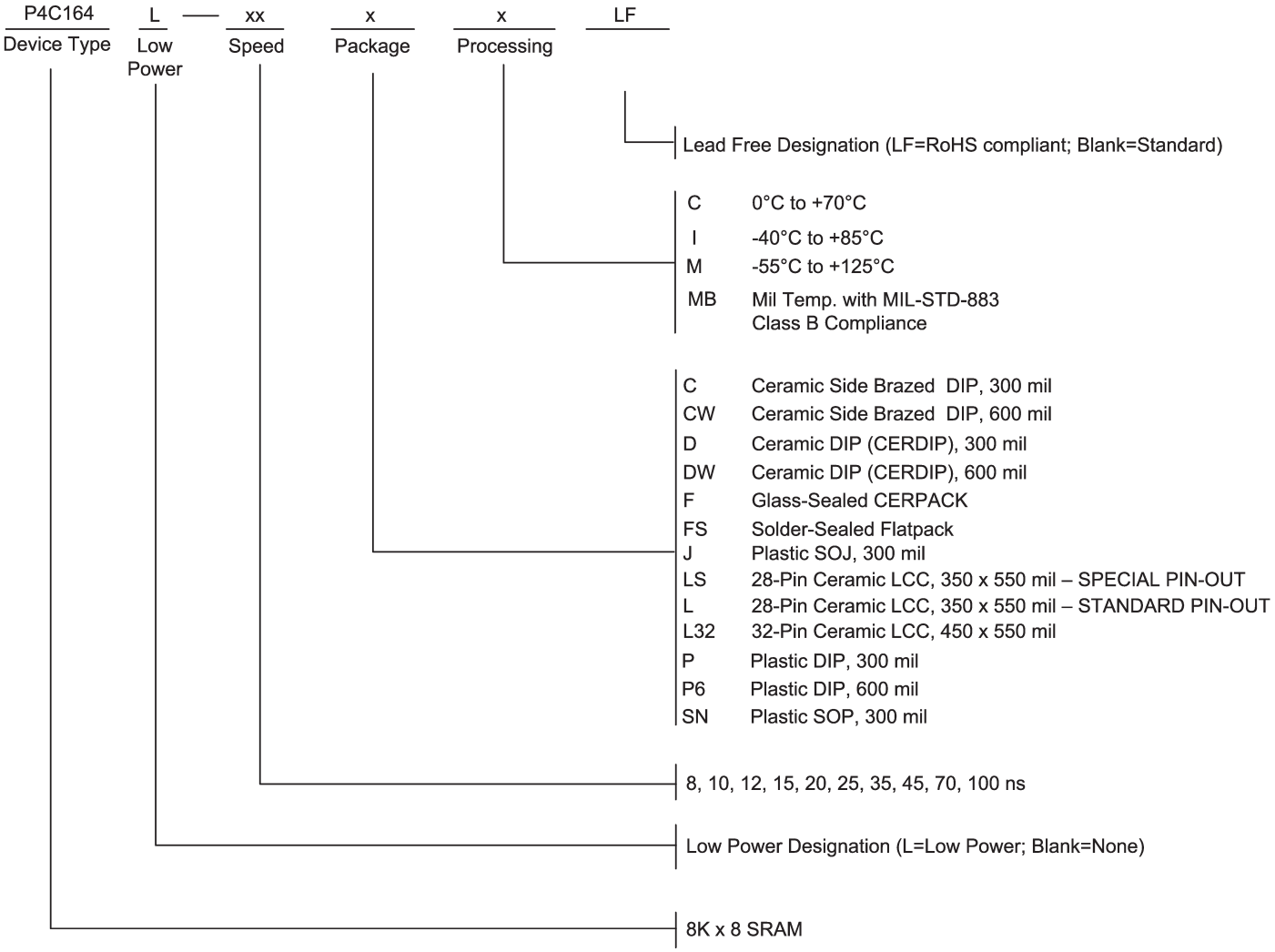


LCC (L5)
"LS" - SPECIAL PIN-OUT



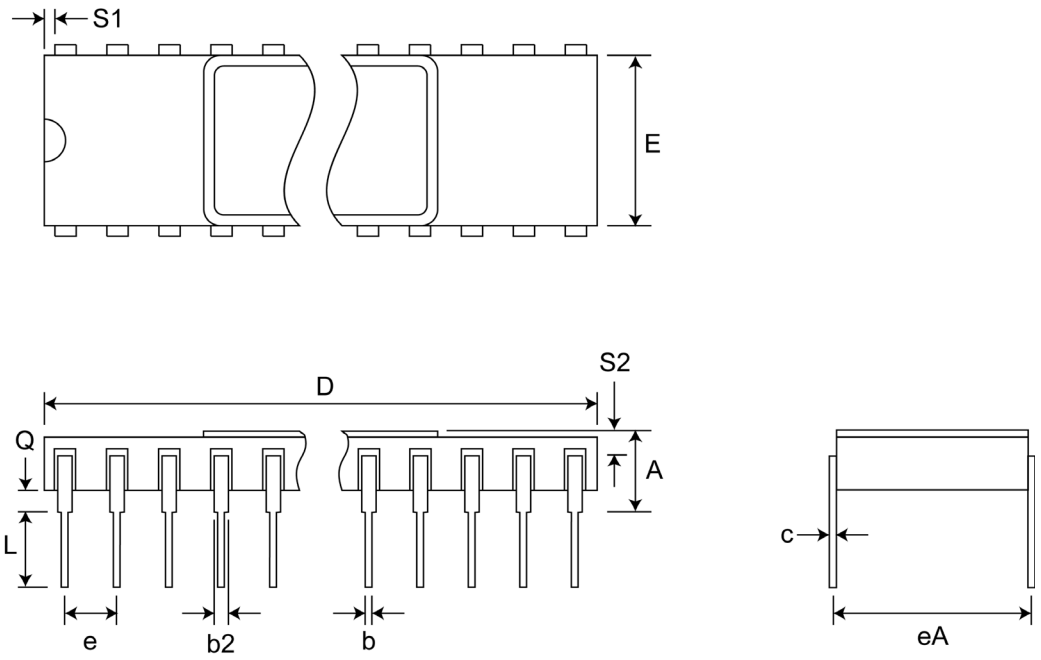
LCC (L6)

ORDERING INFORMATION



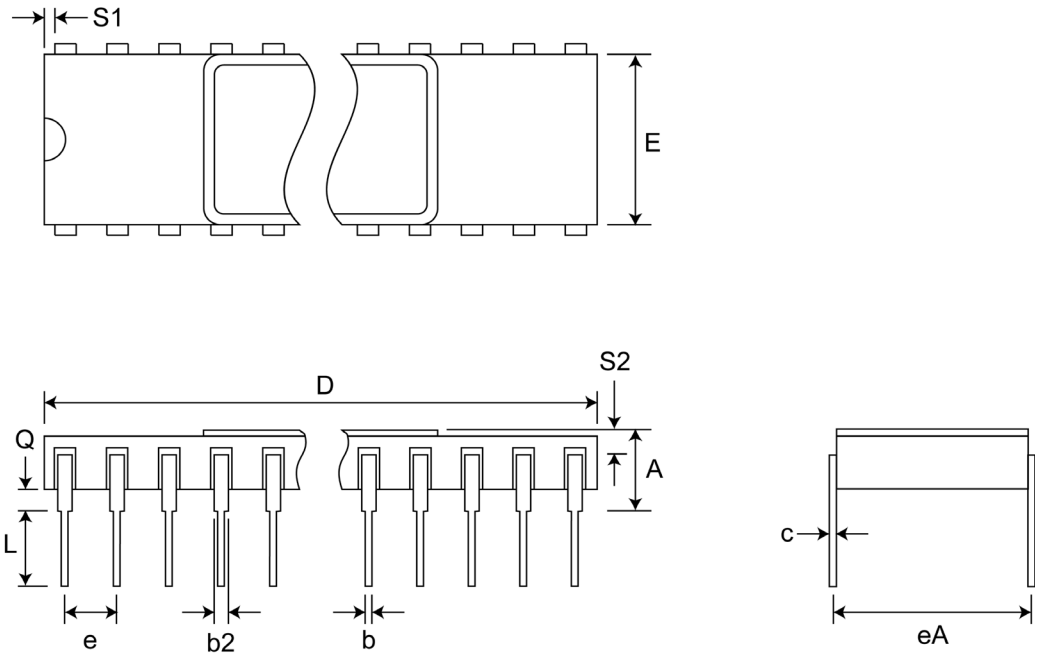
Pkg #	C5	
# Pins	28 (300 mil)	
Symbol	**Min**	**Max**
A	-	0.225
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.485
E	0.240	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	-
S2	0.005	-

SIDEBRAZED DUAL IN-LINE PACKAGE (300 mils)



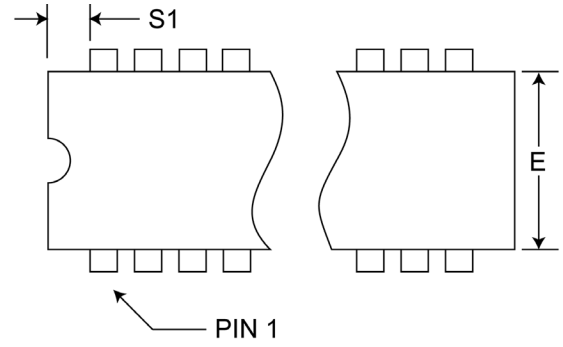
Pkg #	C5-1	
# Pins	28 (600 mil)	
Symbol	**Min**	**Max**
A	-	0.232
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.490
E	0.500	0.610
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0.005	-

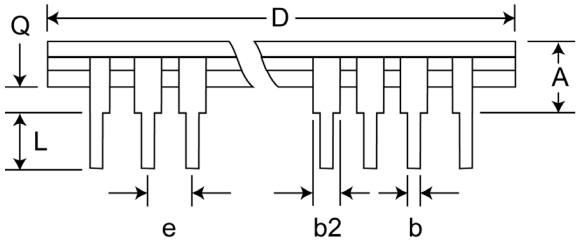
SIDEBRAZED DUAL IN-LINE PACKAGE (600 mils)

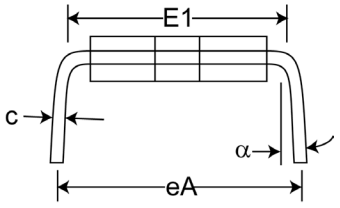


Pkg #	D5-1	
# Pins	28 (600 mil)	
Symbol	**Min**	**Max**
A	-	0.232
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.490
E	0.500	0.610
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
α	0°	15°

CERDIP DUAL IN-LINE PACKAGE

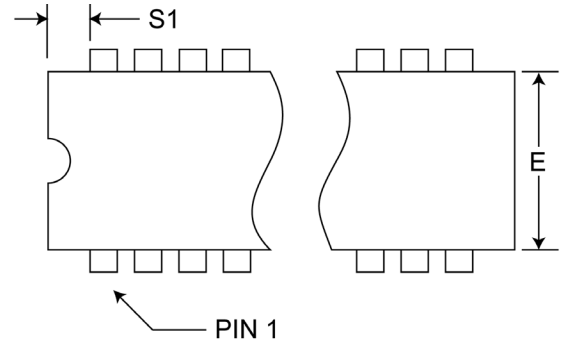


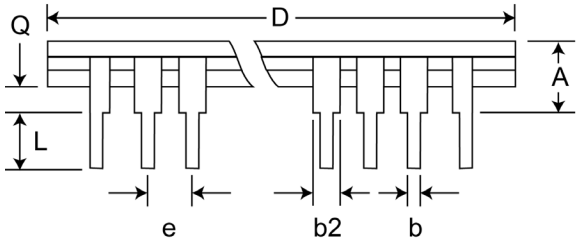


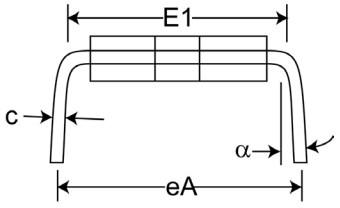


Pkg #	D5-2	
# Pins	28 (300 mil)	
Symbol	**Min**	**Max**
A	-	0.225
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.485
E	0.240	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
α	0°	15°

CERDIP DUAL IN-LINE PACKAGE

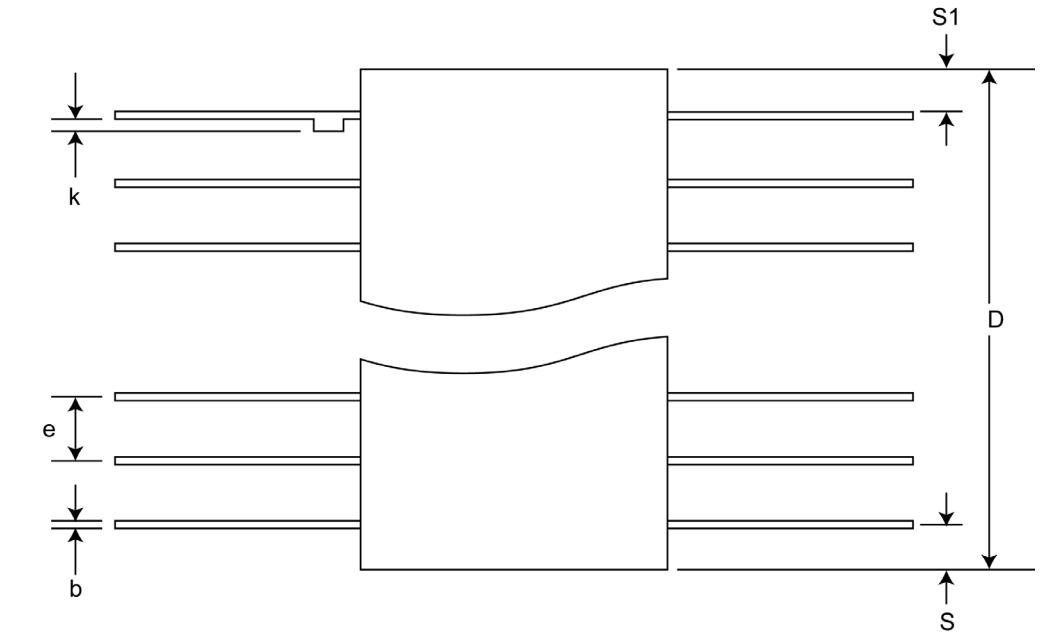


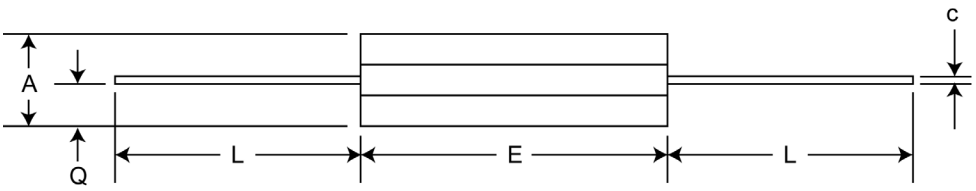




Pkg #	F4	
# Pins	28	
Symbol	**Min**	**Max**
A	0.060	0.090
b	0.015	0.022
c	0.004	0.009
D	-	0.730
E	0.330	0.380
e	0.050 BSC	
k	0.005	0.018
L	0.250	0.370
Q	0.026	0.045
S	-	0.085
S1	0.005	-

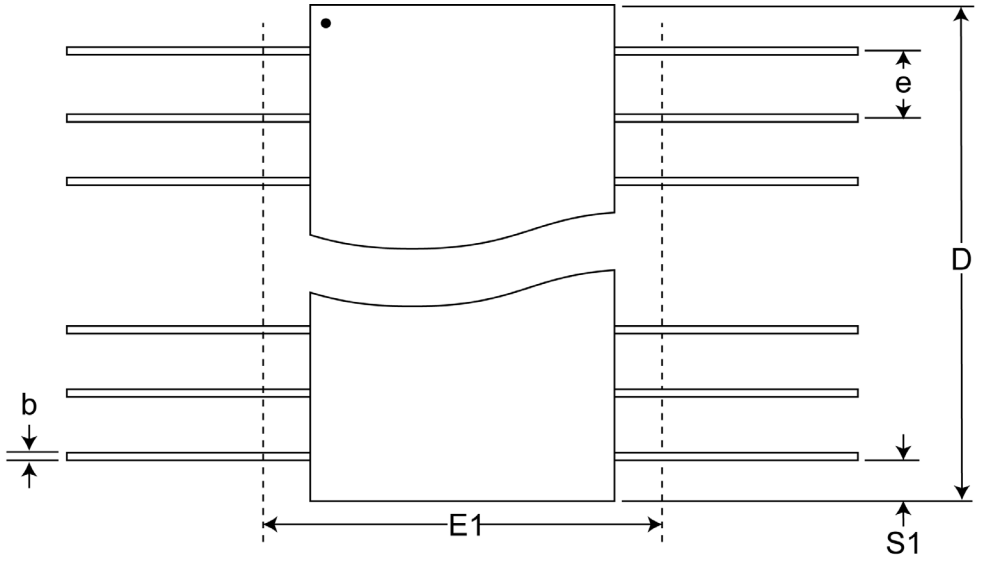
GLASS-SEALED CERAMIC FLATPACK

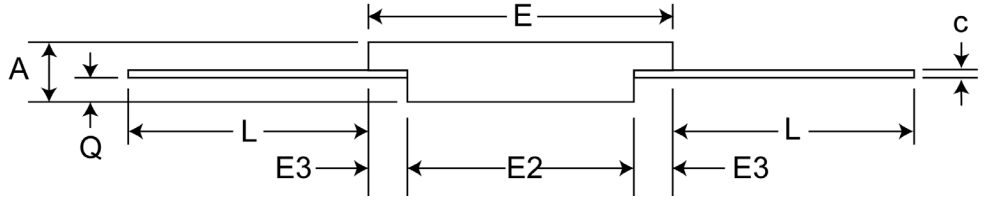




Pkg #	FS-5	
# Pins	28	
Symbol	**Min**	**Max**
A	0.090	0.130
b	0.015	0.022
c	0.004	0.009
D		0.740
E	0.380	0.420
E1	-	0.440
E2	0.180	-
E3	0.030	-
e	0.050 BSC	
L	0.250	0.370
Q	0.026	0.045
S1	0.000	-

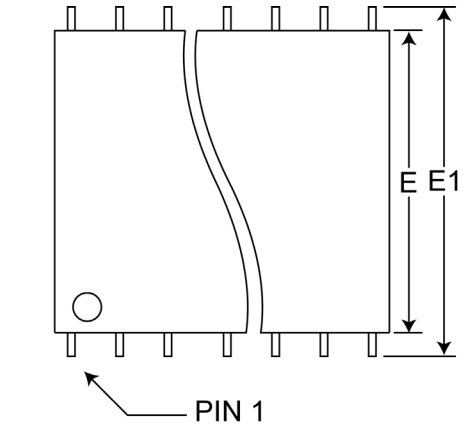
SOLDER-SEAL CERAMIC FLATPACK

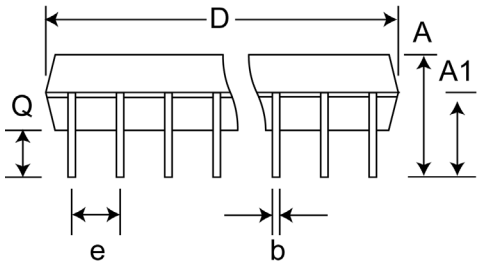


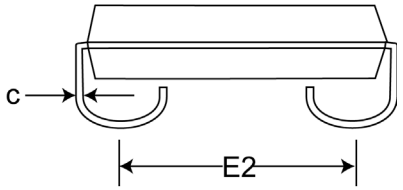


Pkg #	J5	
# Pins	28 (300 mil)	
Symbol	**Min**	**Max**
A	0.120	0.148
A1	0.078	-
b	0.014	0.020
C	0.007	0.011
D	0.700	0.730
e	0.050 BSC	
E	0.292	0.300
E1	0.335	0.347
E2	0.262	0.272
Q	0.025	-

SOJ SMALL OUTLINE IC PACKAGE

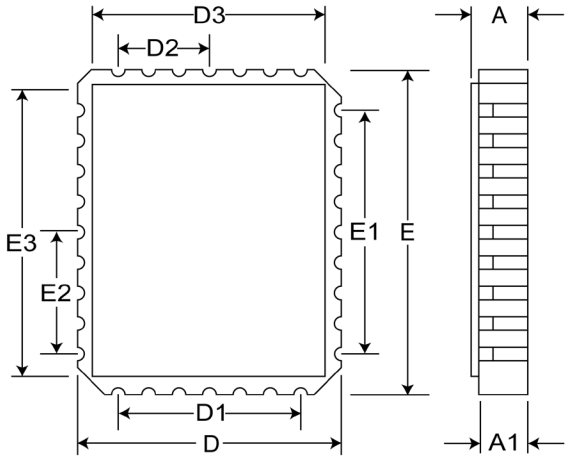


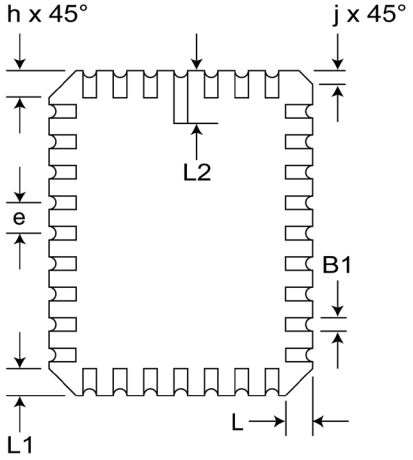




Pkg #	L5	
# Pins	28	
Symbol	**Min**	**Max**
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D	0.342	0.358
D1	0.200 BSC	
D2	0.100 BSC	
D3	-	0.358
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	-	0.558
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	5	
NE	9	

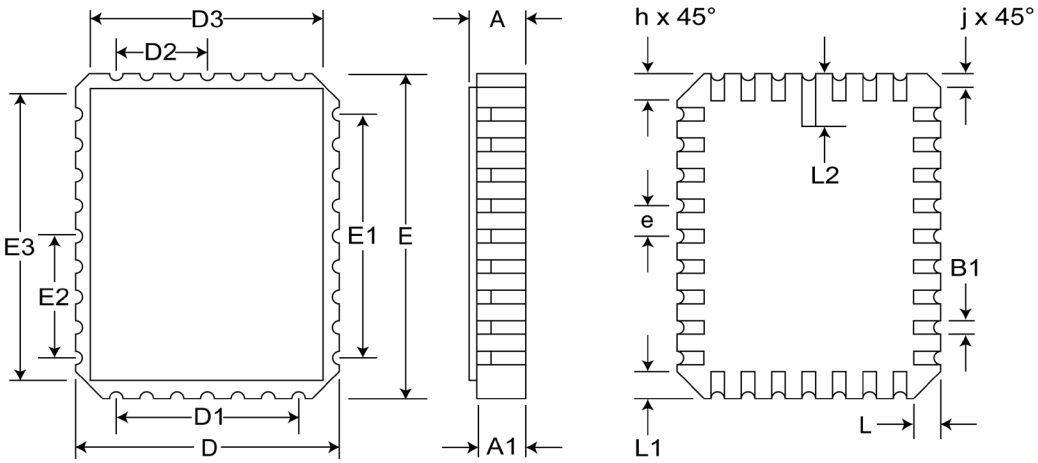
RECTANGULAR LEADLESS CHIP CARRIER





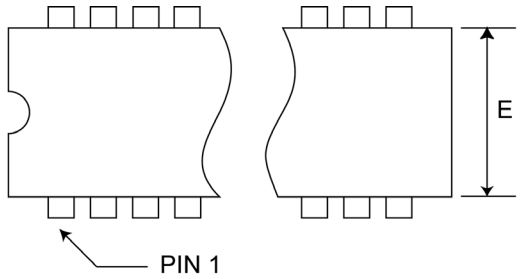
Pkg #	L6	
# Pins	32	
Symbol	**Min**	**Max**
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D	0.442	0.458
D1	0.300 BSC	
D2	0.150 BSC	
D3	-	0.458
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	-	0.558
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	7	
NE	9	

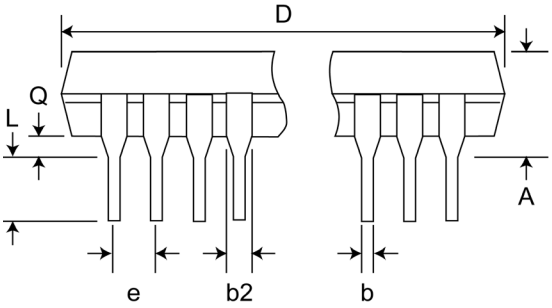
RECTANGULAR LEADLESS CHIP CARRIER

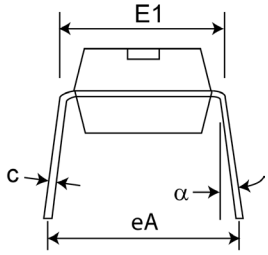


Pkg #	P5	
# Pins	28 (300 mil)	
Symbol	**Min**	**Max**
A	-	0.210
A1		-
b	0.014	0.023
b2	0.045	0.070
C	0.008	0.014
D	1.345	1.400
E1	0.270	0.300
E	0.300	0.380
e	0.100 BSC	
eB	-	0.430
L	0.115	0.150
α	0°	15°

PLASTIC DUAL IN-LINE PACKAGE (300 mils)

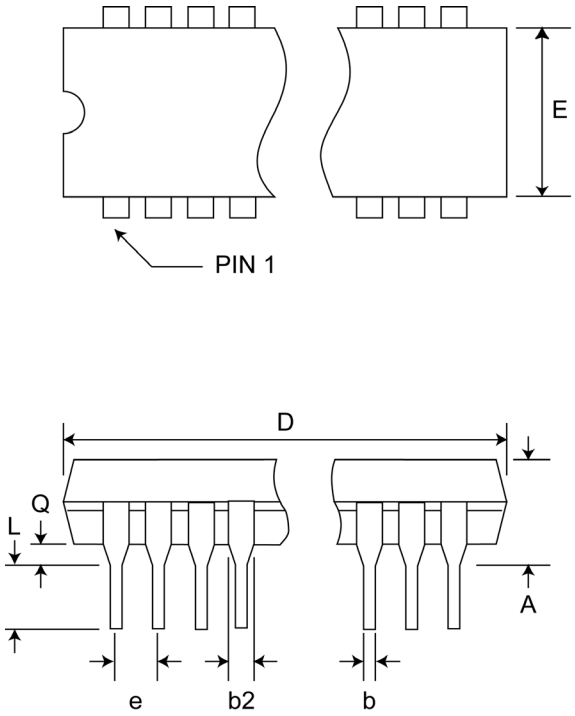






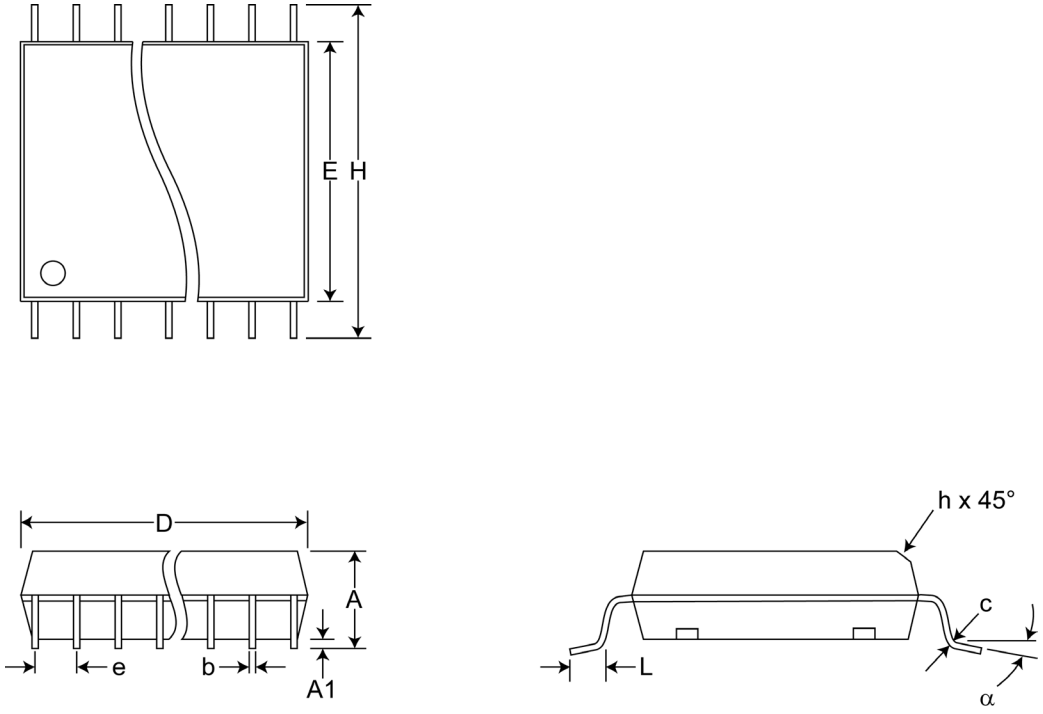
Pkg #	P6	
# Pins	28 (600 mil)	
Symbol	**Min**	**Max**
A	0.090	0.200
A1	0.000	0.070
b	0.014	0.020
b2	0.015	0.065
C	0.008	0.012
D	1.380	1.480
E1	0.485	0.550
E	0.600	0.625
e	0.100 BSC	
eB	0.600 TYP	
L	0.100	0.200
α	0°	15°

PLASTIC DUAL IN-LINE PACKAGE (600 mils)



Pkg #	S6	
# Pins	28 (300 mil)	
Symbol	**Min**	**Max**
A	0.090	0.110
A1	0.003	0.010
B	0.012	0.020
C	0.004	0.012
D	0.700	0.716
e	0.050 BSC	
E	0.290	0.300
H	0.465	0.485
L	0.016	0.050
α	0°	9°

SOIC/SOP SMALL OUTLINE IC PACKAGE (SN)



REVISIONS

DOCUMENT NUMBER	SRAM115
DOCUMENT TITLE	P4C164 ULTRA HIGH SPEED 8Kx8 STATIC CMOS RAM

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	1997	DAB	New Data Sheet
A	Oct-2005	JDB	Changed logo to Pyramid
B	Jun-2006	JDB	Added 28-pin ceramic DIP
C	Aug-2006	JDB	Added Lead-Free designation
D	Aug-2006	JDB	Added "LS" - Special Pin-Out
E	Aug-2006	JDB	Updated SOJ package information
F	Jun-2007	JDB	Corrected SOP package details
G	Sep-2010	JDB	Added P4C164L for non-military temp. Format update.
H	Apr-2011	JDB	Added 28-pin solder-seal flatpack