

MK4802(P/J/N) Series

FEATURES

- Static operation
- Organization: 2K x 8 bit RAM JEDEC pinout
- Pin compatible with Mostek's BYTEWYDE™ memory family
- Double density version of the MK4118 1K x 8 static RAM
- 24/28 pin ROM/PROM compatible pin configuration
- \overline{CE} and \overline{OE} functions facilitate bus control

- High performance

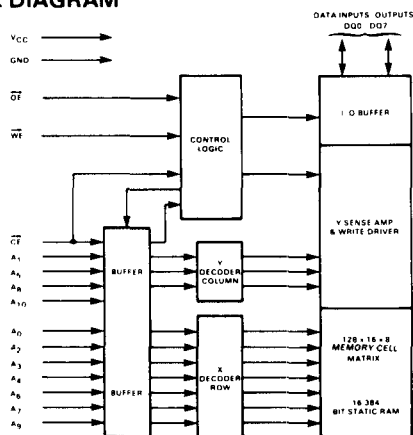
Part No.	Access Time	R/W Cycle Time
MK4802-70	70 nsec	70/80 nsec
MK4802-90	90 nsec	90/100 nsec

DESCRIPTION

The MK4802 uses Mostek's Scaled POLY 5™ process and advanced circuit design techniques to package 16,384 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated™ circuit design techniques.

The MK4802 excels in high speed memory applications where the organization requires relatively shallow depth with a wide word format. The MK4802 presents the user a high density cost effective alternative to bipolar and previous generation N-MOS fast memory. The slower MK4802-3* provides even greater economies with performance suitable for microprocessor memory requirements.

BLOCK DIAGRAM

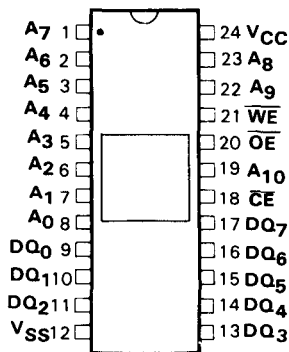


TRUTH TABLE

\overline{CE}	\overline{OE}	\overline{WE}	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	DIN
V_{IL}	V_{IL}	V_{IH}	Read	DOUT
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X - Don't Care

PIN CONNECTIONS



STATIC RAMS

*See MK4802-3 Supplement Data Sheet

PIN NAMES

A ₀ -A ₁₀	Address Inputs	V _{CC}	Power (+5V)
CE	Chip Enable	\overline{WE}	Write Enable
V _{SS}	Ground	\overline{OE}	Output Enable
DQ ₀ -DQ ₇	Data In/Data Out		