Am9708/Am2708

1024 x 8 Erasable Read Only Memory

DISTINCTIVE CHARACTERISTICS

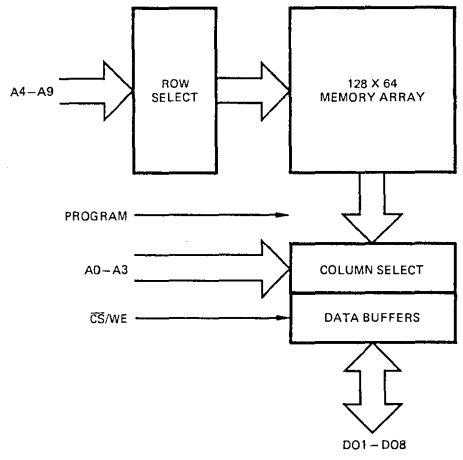
- Direct replacement for Intel 2708/8708
- Interchangeable with Am9208, Am9216 masked ROMs
- Full military temperature operation
- Fast programming time – typically 50 sec.
- TTL compatible interface signals
- Fully static operation – no clocks
- Fast access time – 350ns
- Three-state outputs
- Tested for 100% programmability
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

The Am2708 is an 8,192-bit erasable and programmable MOS read-only memory. It is organized as 1024 words by 8 bits per word. Erasing the data in the EROM is accomplished by projecting ultraviolet light through a transparent window for a predetermined time period.

When the Chip Select/Write Enable input is at the high logic level, the device is unselected and the data lines are in their high impedance state. The device is selected when $\overline{CS}$/WE is at the low logic level. The contents of a particular memory location, specified by the 10 address lines, will be available on the data lines after the access time has elapsed. For programming, $\overline{CS}$/WE is connected to +12V and is used in conjunction with the Program input. The Address and Data lines are TTL compatible for all operating and programming modes.

BLOCK DIAGRAM



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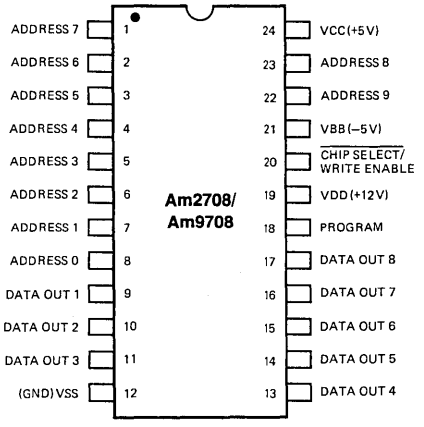
CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation.

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ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Order Number
Hermetic DIP Transparent Window	$0°C \leq T_A \leq +70°C$	AM2708DC (450ns) AM2708-1DC (350ns)
Hermetic DIP Transparent Window	$-55°C \leq T_A \leq +125°C$	AM9708DM (480ns)

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
All Signal Voltages, except Program and $\overline{CS}$/WE, with Respect to VBB	−0.3V to +15V
Program Input Voltage with Respect to VBB	−0.3V to +35V
$\overline{CS}$/WE Input with Respect to VBB	−0.3V to +20V
VCC and VSS with Respect to VBB	−0.3V to +15V
VDD with Respect to VBB	−0.3V to +20V
Power Dissipation	1.5W

The product described by this specification includes internal circuitry designed to protect input devices from excessive accumulation of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to any voltages that exceed the maximum ratings.

OPERATING RANGE

Ambient Temperature	VDD	VCC	VBB	VSS
0°C to +70°C	+12V ±5%	+5V ±5%	−5V ±5%	0V
−55°C to +125°C	+12V ±10%	+5V ±10%	−5V ±10%	0V

PROGRAMMING CONDITIONS

Ambient Temperature	VDD	VCC	VBB	VSS	$\overline{CS}$/WE	VIHP
+25°C	+12V ± 5%	+5V ± 5%	−5V ± 5%	0V	+12V ± 5%	26V ± 1V

READ OPERATION
ELECTRICAL CHARACTERISTICS over operating range (Notes 1, 7)

Parameters	Description	Test Conditions		Min.	Typ.	Max.	Units
VIL	Input LOW Voltage			VSS		0.65	Volts
VIH	Input HIGH Voltage	T_A = 0°C to +70°C		3.0		VCC+1	Volts
		T_A = −55°C to +125°C		2.4		VCC+1	Volts
VOL	Output LOW Voltage	IOL = 1.6mA				0.45	Volts
VOH	Output HIGH Voltage	IOH = − 100μA		3.7			Volts
		IOH = −1.0mA		2.4			Volts
ILI	Address and Chip Select Input Load Current	VSS ≤ VIN ≤ VCC			1.0	10	μA
ILO	Output Leakage Current	VOUT = Worst Case $\overline{CS}$/WE = + 5.0V			1.0	10	μA
IDD	VDD Supply Current	All inputs HIGH. $\overline{CS}$/WE = +5.0V	T_A = 0°C		50	65	mA
			T_A = −55°C			80	
ICC	VCC Supply Current		T_A = 0°C		6.0	10	mA
			T_A = −55°C			15	
IBB	VBB Supply Current		T_A = 0°C		30	45	mA
			T_A = −55°C			60	
PD	Power Dissipation	T_A = 70°C				800	mW
CIN	Input Capacitance	T_A = 25°C f = 1MHz All pins at 0V			4.0	6.0	pF
COUT	Output Capacitance				8.0	12.0	pF

READ OPERATION
SWITCHING CHARACTERISTICS over operating range (Notes 2, 7)

Parameters	Description	Test Conditions	0°C ≤ T_A ≤ 70°C		−55°C ≤ T_A ≤ +125°C		Units
			Min.	Max.	Min.	Max.	
tACC	Address to Output Access Time (Note 3)	tr = tf ≤ 20ns Output Load: One Standard TTL Gate Plus 100pF		2708: 450 / 2708-1: 350		480	ns
tCO	Chip Select to Output on Delay (Note 4)			120		150	ns
tDF	Chip Select to Output OFF Delay		0	120	0	150	
tOH	Previous Read Data Valid with Respect to Address Change		0		0		

PROGRAMMING CHARACTERISTICS under programming conditions

Parameter	Description	Min.	Max.	Units
tAS	Address Set Up Time	10		μs
tCSS	$\overline{CS}$/WE Set Up Time	10		μs
tDS	Data Set Up Time	10		μs
tAH	Address Hold Time (Note 5)	1.0		μs
tCH	$\overline{CS}$/WE Hold Time (Note 5)	0.5		μs
tDH	Data Hold Time	1.0		μs
tDF	Chip Select to Output Off Delay	0	120	ns
tDPR	Program to Read Delay		10	μs
tPW	Program Pulse Width	0.1	1.0	ms
tPR, tPF	Program Pulse Transition Times	0.5	2.0	μs
VIHW	$\overline{CS}$/WE Input High Level	11.4	12.6	Volts
VIHP	Program Pulse High Level (Note 6)	25	27	Volts
VILP	Program Pulse Low Level (Note 6)	VSS	1.0	Volts

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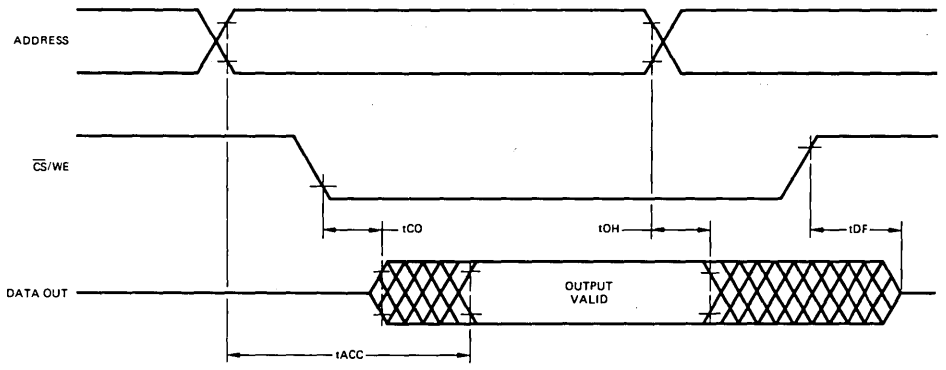
SWITCHING WAVEFORMS

READ CYCLE



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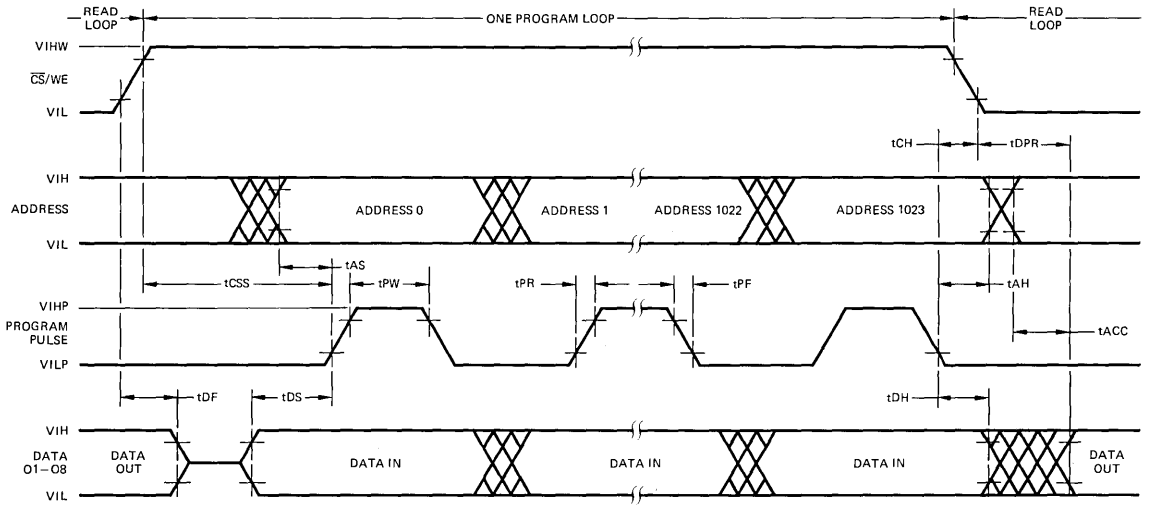
PROGRAM MODE (Note 5)



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PROGRAMMING THE Am2708

All 8192 bits of the Am2708 are in the logic HIGH state after erasure. When any of the output bits are programmed, the output state will change from HIGH to LOW. Programming of the device is initiated by raising the $\overline{CS}$/WE input to +12V. A memory location is programmed by addressing the device and supplying 8 data bits in parallel to the data out lines. When address and data bits are set up, a programming pulse is applied to the program input. All addresses are programmed sequentially in a similar manner. One pass through all 1024 addresses is considered one program loop. The number of program loops (N) required to complete the programming cycle is a function of the program pulse width (tPW) such that N $\geqslant$ 100ms/tPW requirement is met. Do not apply more than one program pulse per address without sequentially programming all other addresses. There should be N successive loops through all locations. The Program pin will source the IIPL current when it is low (VILP) and $\overline{CS}$/WE is high (VIHW). The Program pin should be actively pulled down to maintain its low level.

ERASING THE Am2708

The Am2708 can be erased by exposing the die to high-intensity, short-wave, ultra-violet light at a wavelength of 2537 angstroms through the transparent lid. The recommended dosage is ten watt-seconds per square centimeter. This erasing condition can be obtained by exposing the die to model S-52 ultraviolet lamp manufactured by Ultra-Violet Products, Inc. or Product Specialties, Inc. for approximately 20 to 30 minutes from a distance of about 2.5 centimeters above the transparent lid. The light source should not be operated with a short-wave filter installed. All bits will be in a logic HIGH state when erasure is complete.

CAUTION

Ultraviolet radiation is invisible and can damage human eyes. Precautions should be taken to avoid exposure to direct or reflected ultraviolet radiation. It will often be convenient to fully enclose the ultraviolet source and the EROMs being erased to prevent accidental exposure.

Ultraviolet lamps can also ionize oxygen and create ozone which can be harmful to humans. Erasing should be carried out in a well ventilated area in order to minimize the concentration of ozone.

NOTES:

1. Typical values are for $T_A = 25^\circ C$, nominal supply voltages and nominal processing parameters.
2. Timing reference levels (Read) —
   Inputs: High = 2.8V (DC), 2.2V (DM); Low = 0.8V
   Outputs: High = 2.4V, Low = 0.8V
3. Typical access time is 280ns.
4. Typical chip select to output on delay is 60ns.
5. tAH must be greater than tCH.
6. VIHP – VILP $\geqslant$ 25 Volts.
7. V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.