ICE27C010
1- Megabit(128KX8) OTP EPROM

Description

The ICE27C010 is a low-power, high-performance 1M(1,048,576) bit one-time programmable read only memory (OTP EPROM) organized as 128K by 8 bits. It is single 5V power supply in normal read mode operation. Any byte can be accessed in less than 45 ns. The ICE27C010 typically consumes 10mA , standby mode supply current typically 1μA. Two lines control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention. Programming time is typically only 100 μs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

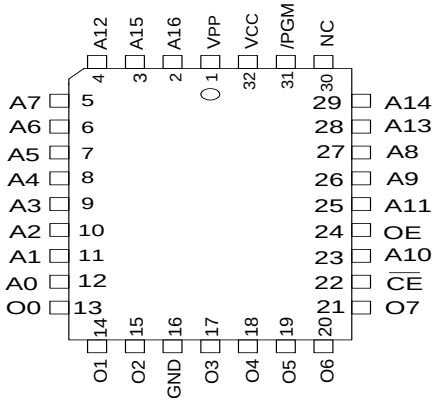
Features

- Fast Read Access Time : – 70ns
- Low-Power consumption
  - 1 μA Typ. Standby
  - 10 mA max. Active at 5MHz
- JEDEC Standard Packages
  - 32-Lead 600-mil PDIP
  - 32-Lead PLCC
  - 32-Lead TSOP
- Operating voltage : 5V ±10%
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200 mA Latchup Immunity
- Programming time : 100 us/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code

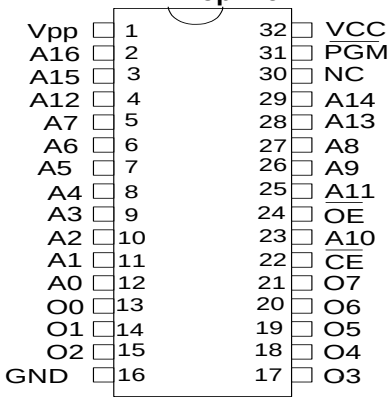
Pin Configurations

Pin Name	Function
A0 – A16	Addresses
O0 – O7	Outputs
/CE	Chip Enable
/OE	Output Enable
/PGM	Program Strobe
NC	No Connect

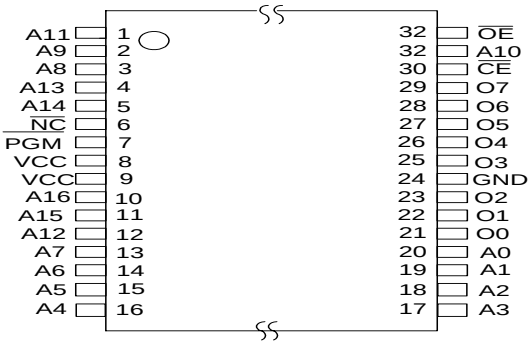
PLCC Top View



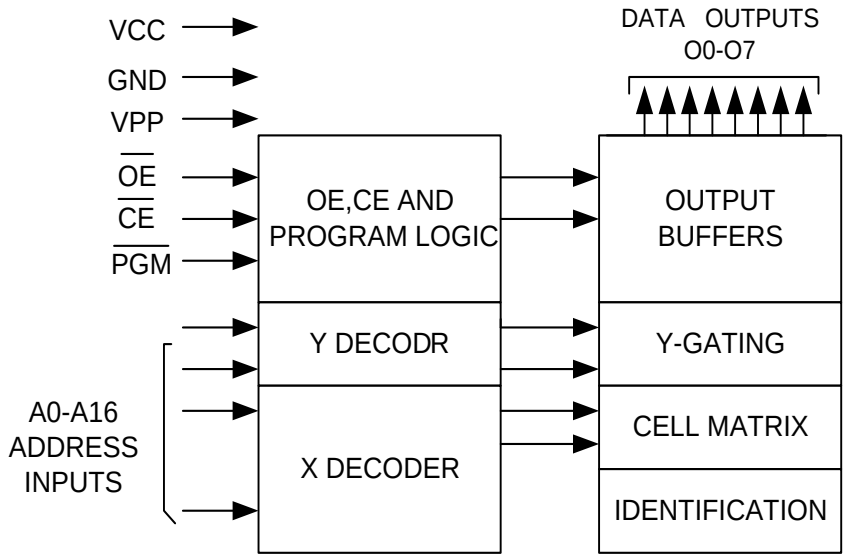
PDIP Top View



TSOP Top View



Block Diagram



Absolute Maximum Rating

Operation Temperature Commercial	0℃ to +70℃
Storage Temperature	-65℃ to +125℃
Voltage on Any Pin with Respect to Ground	-0.6V to +7.0V(1)
Vpp Supply Voltage with Respect to Ground	-0.6V to +13.5V(1)

Operating Modes

Mode\Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	VPP	Outputs
Read	V_{IL}	V_{IL}	X(1)	Ai	X	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	High Z
Standby	V_{IH}	X	X	X	X	High Z
Rapid Program(2)	V_{IL}	VPP	V_{IL}	Ai	VPP	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	VPP	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	VPP	High Z
Product Identification(4)	V_{IL}	V_{IL}	X	A9 = V_H(3) A0,A1 = V_{IH} or V_{IL} A2 – A16 = V_{IL}	X	Identification Code

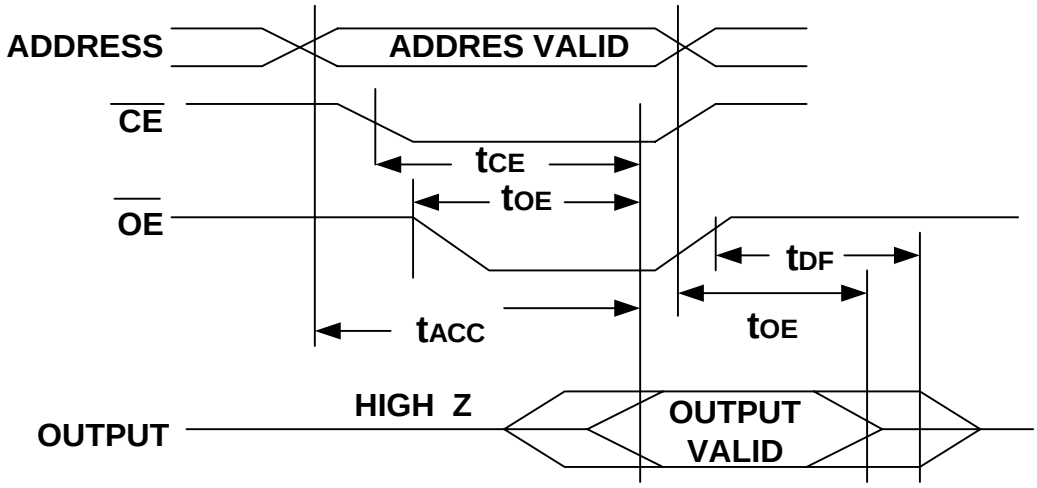
Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming Characteristics.
3. V_H = 12 ± 0.5V.
4. See Product Identification Code item.

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to Vcc	Com.		± 1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to Vcc	Com.		± 5	µA
IPP1[2]	Vpp[1] Read/Standby Current	Vpp = Vcc			3	uA
I_{SB}	Vcc[1] Standby Current	I_{SB1}(CMOS), $\overline{CE}$ = Vcc ± 0.3V			3	µA
		I_{SB2}(TTL), $\overline{CE}$ = 2.0 to Vcc + 0.5V			500	uA
I_{CC}	Vcc Active Current	f = 5MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}			10	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.2	Vcc + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		2.4		V

Notes: 1. Vcc must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.
2. Vpp may be connected directly to Vcc except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

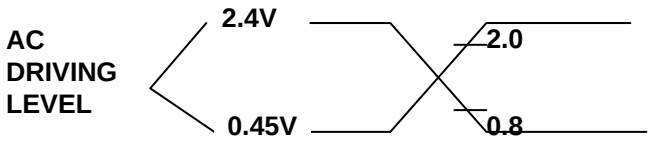
AC Waveforms for Read Operation [1]



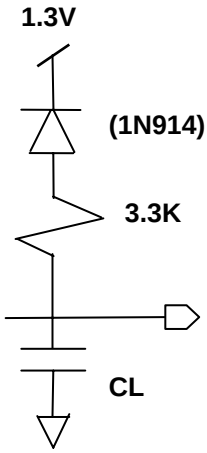
Notes:

1. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
2. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address in valid without impact on t_{ACC}.
3. This parameter is only sampled and is not 100% tested.
4. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels

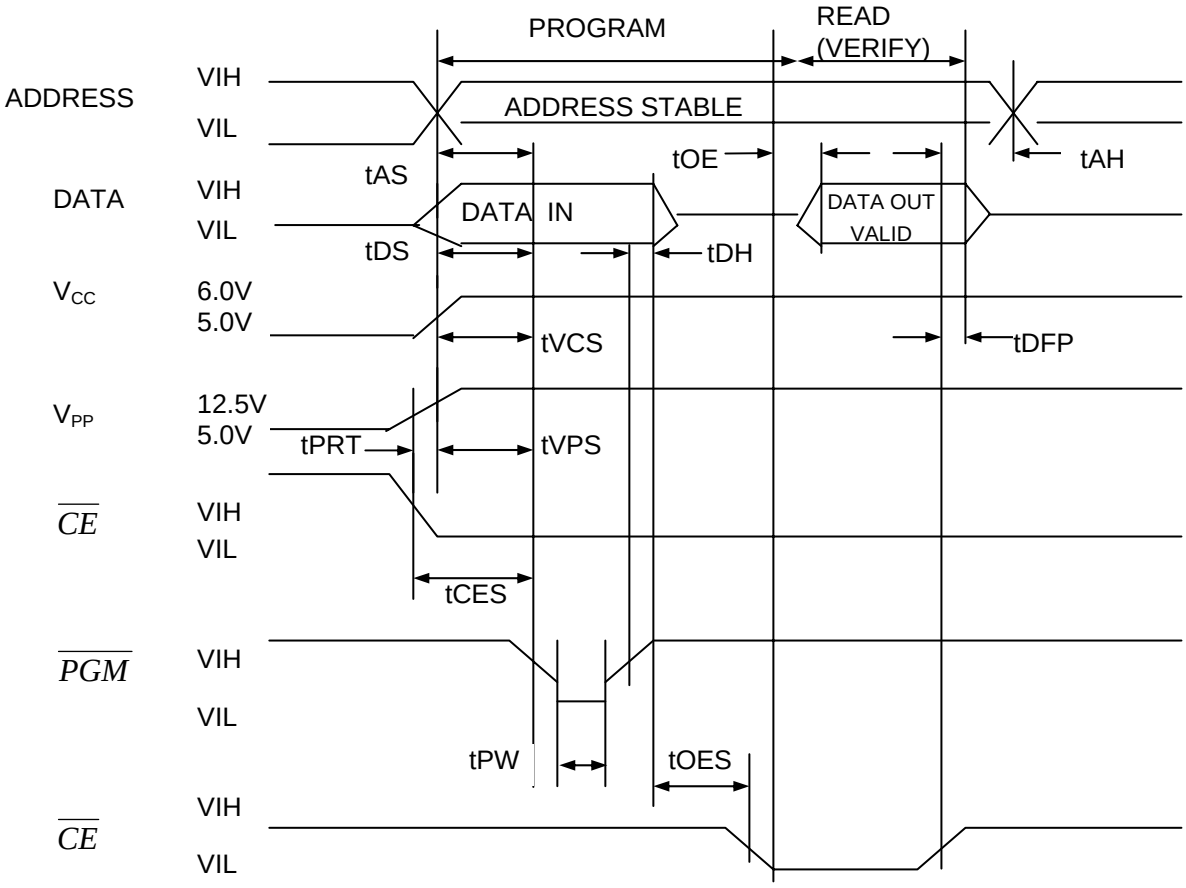


Output Test Load



Note: C_L = 50 pF including jig capacitance

Programming Waveforms (1)



Notes:

1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the ICE27C010 at 0.1uF capacitor is required across V_{pp} and ground to suppress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5℃, Vcc = 5.5 ± 0.5V, Vpp = 12 ± 0.5V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{LI}	Input Load Current	$I_{IN} = V_{IL}, V_{IH}$		± 10	μA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	Vcc + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 μA	2.4		V
I_{CC2}	Vcc Supply Current (Program and Verify)			20	mA
I_{PP2}	$\overline{OE}$ Supply Current	$\overline{CE} = \overline{PGM} = V_{IL}$		10	mA
V_{ID}	A9 Product Identification Voltage		10	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, Vcc = 5.5 ± 0.5V, Vpp = 12.0 ± 0.5V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
t_{AS}	Address Setup Time	Input Rise and Fall Times (10% to 90%) 20ns Input Pulse Levels 0.45V to 2.4V Input Timing Reference Level 0.8V to 2.0V Output Timing Reference Level 0.8V to 2.0V	2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay(2)		0	130	ns
t_{VPS}	Vpp Setup Time		2		µs
t_{VCS}	Vcc Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width(3)		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			70	ns
t_{PRT}	Vpp Pulse Rise Time During Programming		50		ns

Notes: 1. Vcc must be applied simultaneously or before Vpp.and removed simultaneously or after Vpp.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

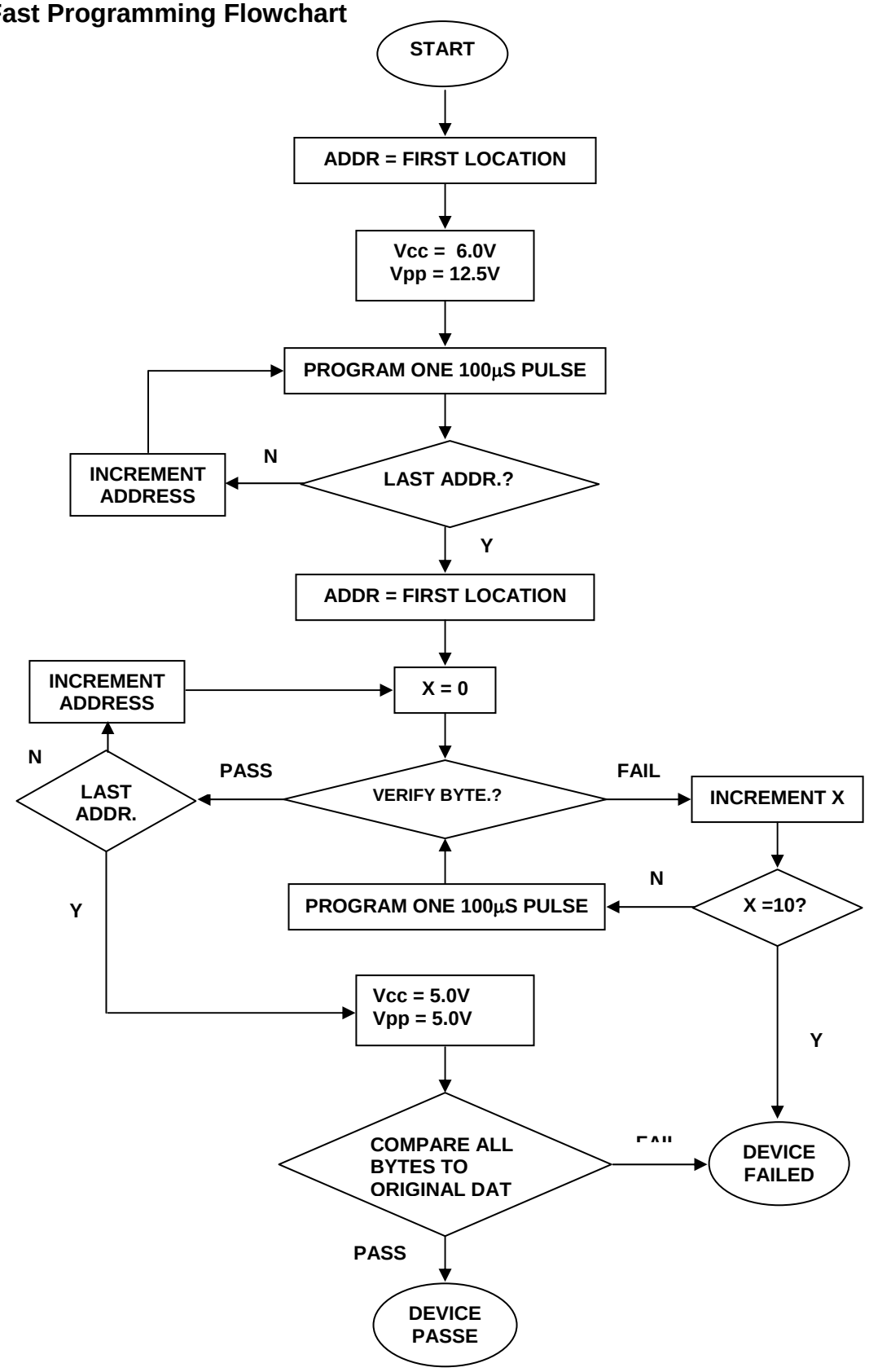
Product Identification Code

Codes	Pins										Hex Data
	A1	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Continue Code 1	0	0	0	1	1	1	1	1	1	1	7F
Continue Code 2	0	1	0	1	1	1	1	1	1	1	7F
Manufacturer	1	0	0	1	0	1	1	1	1	0	5E
Device Type	1	1	1	1	0	0	0	0	0	1	C1

Rapid Programming Algorithm

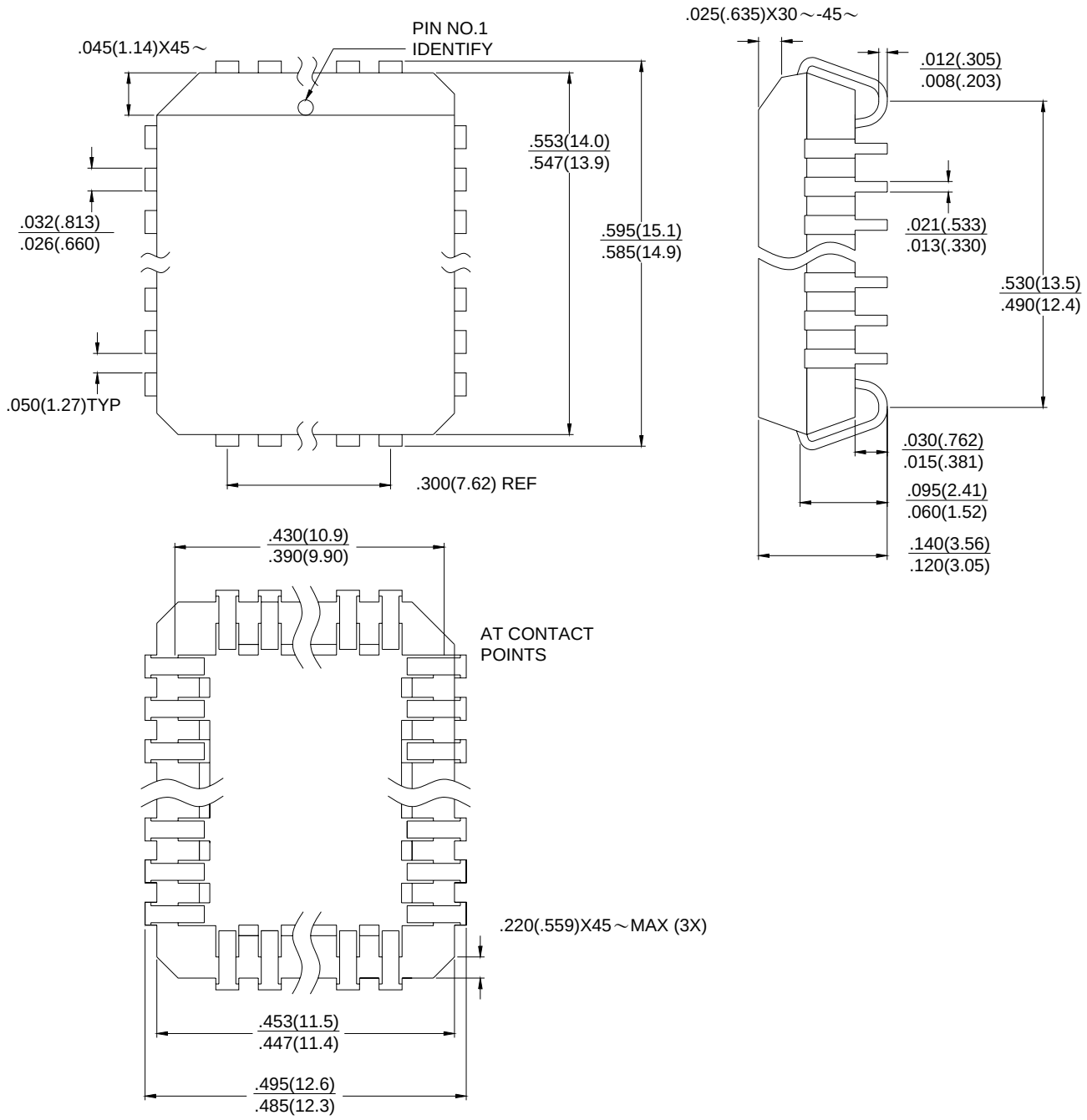
A 100 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. Vcc is raised to 6.0V and Vpp is raised to 12.5V. Each address is first programmed with one 100 µs $\overline{PGM}$ pulse without verification. Then a verification/ reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. Vpp is then lowered to 5.0V and Vcc to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.

Fast Programming Flowchart

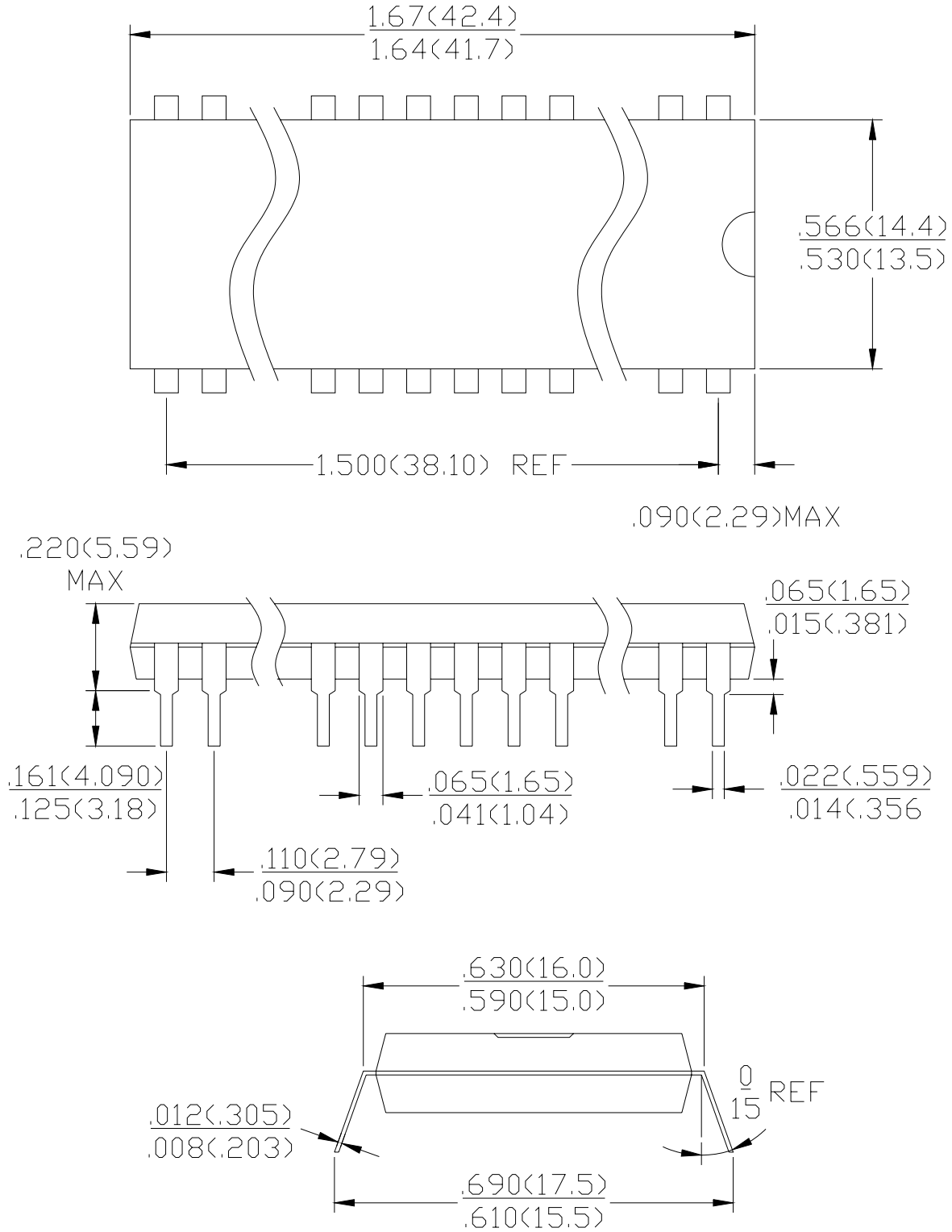


Packaging Information

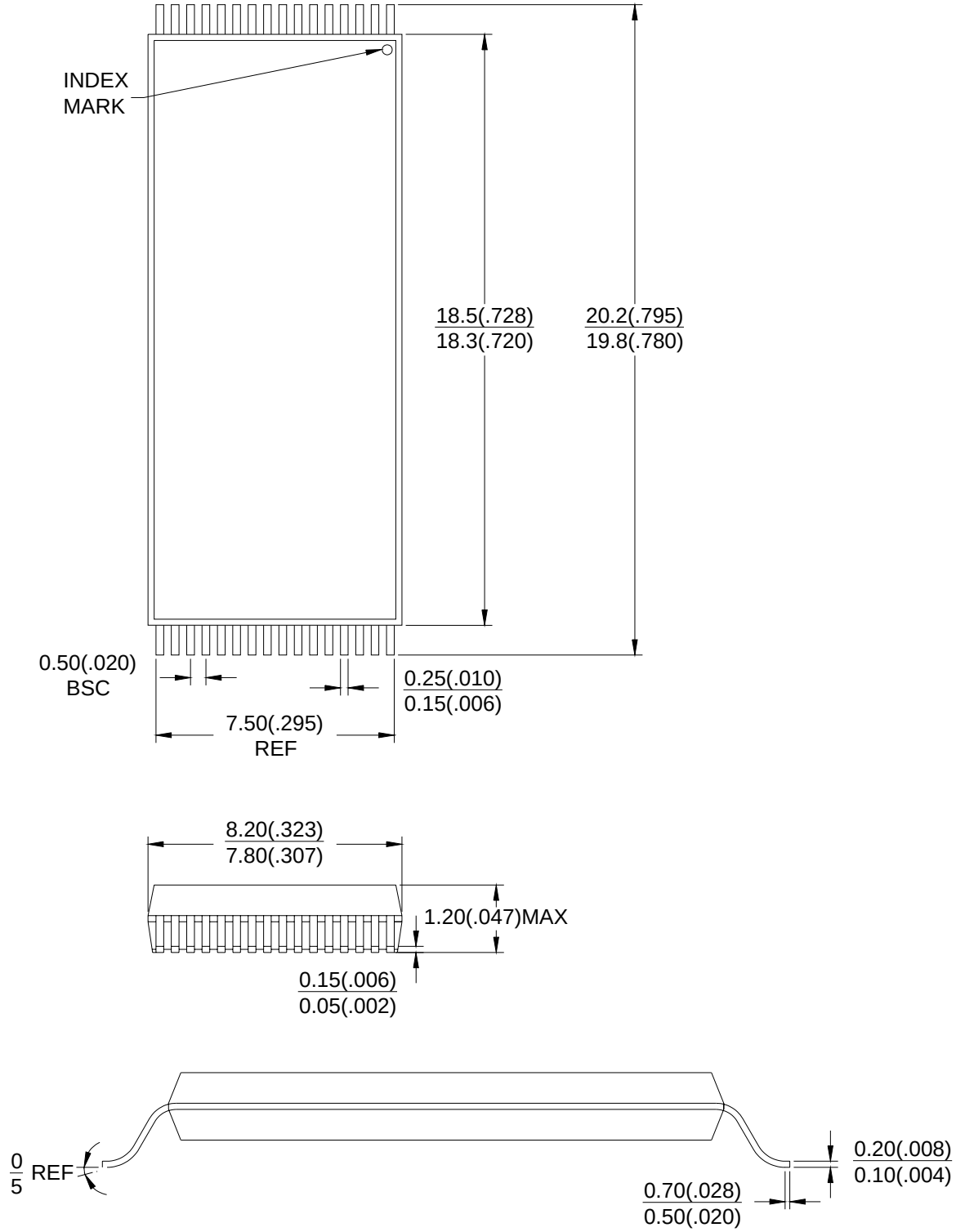
32P, 32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-016 AE



32D, 32-Lead, 0.600” wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



32T, 32-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*
JEDEC OUTLINE MO- 141 BD



*Controlling dimension: millimeters