MAX 5000

Programmable Logic Device Family

May 1999, ver. 5 — Data Sheet

Features...

- Advanced Multiple Array MatriX (MAX®) 5000 architecture combining speed and ease-of-use of PAL devices with the density of programmable gate arrays
- Complete family of high-performance, erasable CMOS EPROM erasable programmable logic devices (EPLDs) for designs ranging from fast 28-pin address decoders to 100-pin LSI custom peripherals
- 600 to 3,750 usable gates (see Table 1)
- Fast, 15-ns combinatorial delays and 76.9-MHz counter frequencies
- Configurable expander product-term distribution allowing more than 32 product terms in a single macrocell
- 28 to 100 pins available in dual in-line package (DIP), J-lead chip carrier, pin-grid array (PGA), and quad flat pack (QFP) packages
- Programmable registers providing D, T, JK, and SR flipflop functionality with individual clear, preset, and clock controls
- Programmable security bit for protection of proprietary designs
- Software design support featuring the Altera® MAX+PLUS® II development system on Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations

Table 1. MAX 5000 Device Features

Feature	EPM5032	EPM5064	EPM5128	EPM5130	EPM5192
Usable gates	600	1,250	2,500	2,500	3,750
Macrocells	32	64	128	128	192
Logic array blocks (LABs)	1	4	8	8	12
Expanders	64	128	256	256	384
Routing	Global	PIA	PIA	PIA	PIA
Maximum user I/O pins	24	36	60	84	72
t_{PD} (ns)	15	25	25	25	25
t_{ASU} (ns)	4	4	4	4	4
t_{CO} (ns)	10	14	14	14	14
f_{CNT} (MHz)	76.9	50	50	50	50

…and More Features

- Programming support with Altera's Master Programming Unit (MPU) or programming hardware from third-party manufacturers
- Additional design entry and simulation support provided by EDIF, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and Viewlogic

General Description

The MAX 5000 family combines innovative architecture and advanced process technologies to offer optimum performance, flexibility, and the highest logic-to-pin ratio of any general-purpose programmable logic device (PLD) family. The MAX 5000 family provides 600 to 3,750 usable gates, pin-to-pin delays as fast as 15 ns, and counter frequencies of up to 76.9 MHz (see Table 2).

Table 2. MAX 5000 Device Speed Grades

Device	Speed (t_{PD1})				
	15 ns	20 ns	25 ns	30 ns	35 ns
EPM5032	✓	✓	✓		
EPM5064			✓	✓	✓
EPM5128			✓	✓	✓
EPM5130			✓		✓
EPM5192			✓		✓

The MAX 5000 architecture supports 100% TTL emulation and high-density integration of multiple SSI, MSI, and LSI logic functions. For example, an EPM5192 device can replace over 100 74-series devices; it can integrate complete subsystems into a single package, saving board area and reducing power consumption. MAX 5000 EPLDs are available in a wide range of packages (see Table 3), including the following:

- Windowed ceramic and plastic dual in-line (CerDIP and PDIP)
- Plastic J-lead chip carrier (PLCC)
- Windowed ceramic pin-grid array (PGA)
- Plastic quad flat pack (PQFP)

Table 3. MAX 5000 Pin Count & Package Options

Device	Pin Count				
	CerDIP	PDIP	PLCC	PGA	PQFP
EPM5032	28	28	28		
EPM5064			44		
EPM5128			68	68	
EPM5130			84	100	100
EPM5192			84	84	

MAX 5000 EPLDs have between 32 and 192 macrocells that are combined into groups called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register that provides D, T, JK, or SR operation with independent programmable clock, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with shareable expander product terms ("shared expanders") to provide more than 32 product terms per macrocell.

The MAX 5000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The MAX+PLUS II system provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools. The MAX+PLUS II software runs on Windows-based PCs as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.

For more information on the MAX+PLUS II development system, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

Functional Description

This section provides a functional description of MAX 5000 EPLDs, which have the following architectural features:

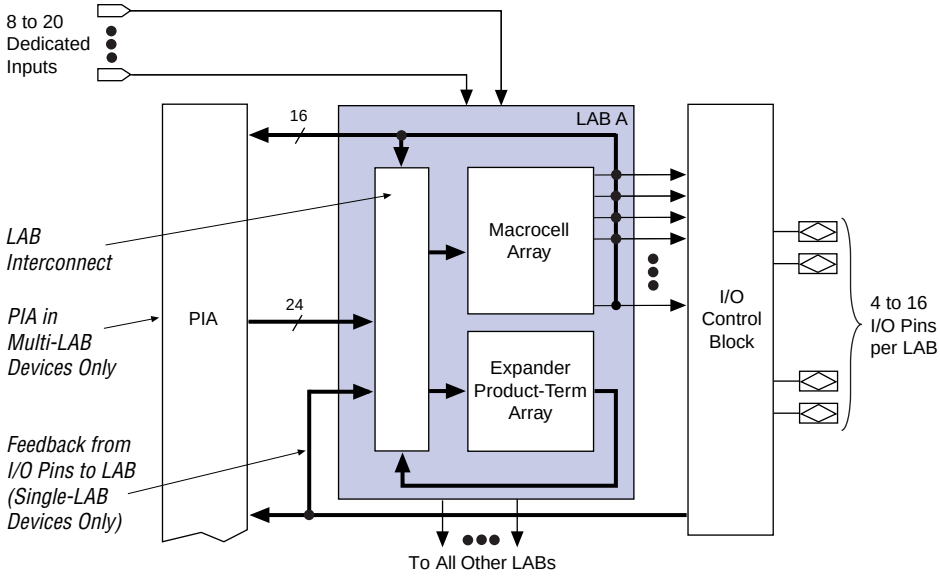
- Logic array blocks
- Macrocells
- Clocking options
- Expander product terms
- Programmable interconnect array
- I/O control blocks

The MAX 5000 architecture is based on the concept of linking high-performance, flexible logic array modules called LABs. Multiple LABs are linked via the programmable interconnect array (PIA), a global bus that is fed by all I/O pins and macrocells. In addition to these basic elements, the MAX 5000 architecture includes 8 to 20 dedicated inputs, each of which can be used as a high-speed, general-purpose input. Alternatively, one of the dedicated inputs can be used as a high-speed global clock for registers.

Logic Array Blocks

MAX 5000 EPLDs contain 1 to 12 LABs. The EPM5032 has a single LAB, while the EPM5064, EPM5128, EPM5130, and EPM5192 contain multiple LABs. Each LAB consists of a macrocell array and an expander product-term array (see Figure 1). The number of macrocells and expanders in the arrays varies with each device.

Figure 1. MAX 5000 Architecture

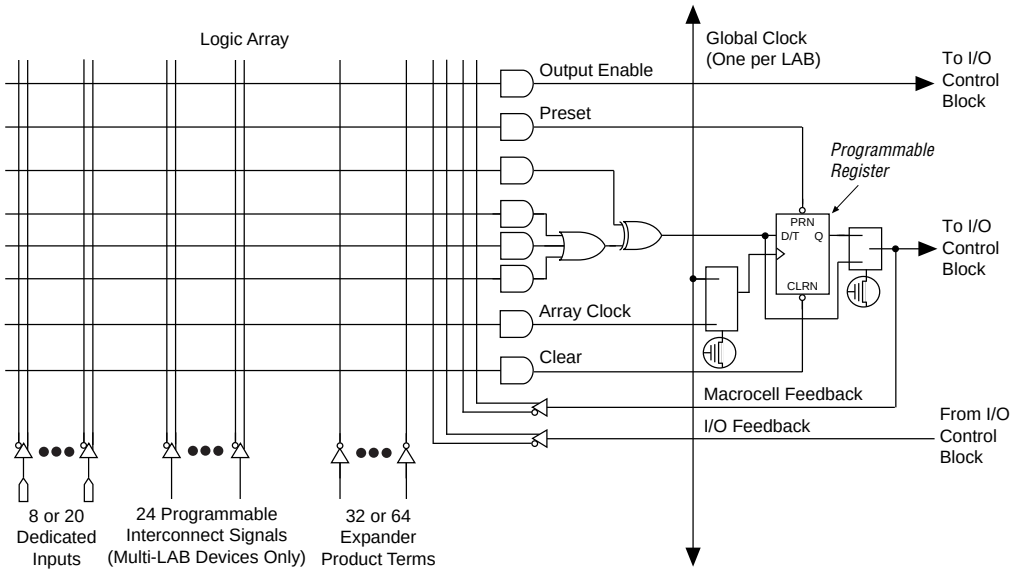


Macrocells are the primary resource for logic implementation. Additional logic capability is available from expanders, which can be used to supplement the capabilities of any macrocell. The expander product-term array consists of a group of unallocated, inverted product terms that can be used and shared by all macrocells in the LAB to create combinatorial and registered logic. These flexible macrocells and shareable expanders facilitate variable product-term designs without the inflexibility of fixed product-term architectures. All macrocell outputs are globally routed within an LAB via the LAB interconnect. The outputs of the macrocells also feed the I/O control block, which consists of groups of programmable tri-state buffers and I/O pins. In the EPM5064, EPM5128, EPM5130, and EPM5192 devices, multiple LABs are connected by a PIA. All macrocells feed the PIA to provide efficient routing for high-fan-in designs.

Macrocells

The MAX 5000 macrocell consists of a programmable logic array and an independently configurable register (see Figure 2). The register can be programmed to emulate D, T, JK, or SR operation, as a flow-through latch, or bypassed for combinatorial operation. Combinatorial logic is implemented in the programmable logic array, in which three product terms that are ORed together feed one input to an XOR gate. The second input to the XOR gate is used for complex XOR arithmetic logic functions and for De Morgan's inversion. The output of the XOR gate feeds the programmable register or bypasses it for combinatorial operation.

Figure 2. MAX 5000 Device Macrocell



Additional product terms (called secondary product terms) are used to control the output enable, preset, clear, and clock signals. Preset and clear product terms drive the active-low asynchronous preset and asynchronous clear inputs to the configurable flipflop. The clock product term allows each register to have an independent clock and supports positive- and negative-edge-triggered operation. Macrocells that drive an output pin can use the output enable product term to control the active-high tri-state buffer in the I/O control block.

The MAX 5000 macrocell configurability makes it possible to efficiently integrate complete subsystems into a single device.

Clocking Options

Each LAB supports either global or array clocking. Global clocking is provided by a dedicated clock signal (CLK) that offers fast clock-to-output delay times. Because each LAB has one global clock, all flipflop clocks within the LAB can be positive-edge-triggered from the CLK pin. If the CLK pin is not used as a global clock, it can be used as a high-speed dedicated input.

In the array clocking mode, each flipflop is clocked by a product term. Any input pin or internal logic can be used as a clock source. Array clocking allows each flipflop to be configured for positive- or negative-edge-triggered operation, giving the macrocell increased flexibility. Systems that require multiple clocks are easily integrated into MAX 5000 EPLDs.

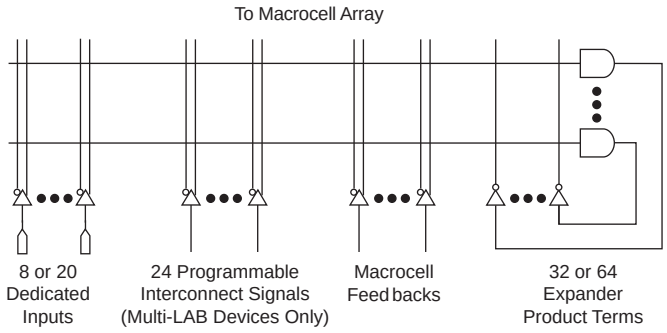
Each flipflop in an LAB can be clocked by a different array-generated clock; however, global and array clocking modes cannot be mixed in the same LAB.

Expander Product Terms

While most logic functions can be implemented with the product terms available in each macrocell, some logic functions are more complex and require additional product terms. Although additional macrocells can be used to supply the needed logic resources, the MAX 5000 architecture can also use shared expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Each LAB has 32 shared expanders (except for EPM5032 devices, which have 64). The expanders can be viewed as a pool of uncommitted product terms. The expander product-term array (see Figure 3) contains unallocated, inverted product terms that feed the macrocell array. Expanders can be used and shared by all product terms in the LAB. Wherever extra logic is needed (including register control functions), expanders can be used to implement the logic. These expanders provide the flexibility to implement register- and product-term-intensive designs in MAX 5000 EPLDs.

Figure 3. Expander Product Terms



Expanders are fed by all signals in the LAB. One expander can feed all macrocells in the LAB or multiple product terms in the same macrocell. Because expanders also feed the secondary product terms of each macrocell, complex logic functions can be implemented without using additional macrocells. A small delay (t_{SEXP}) is incurred when shared expanders are used.

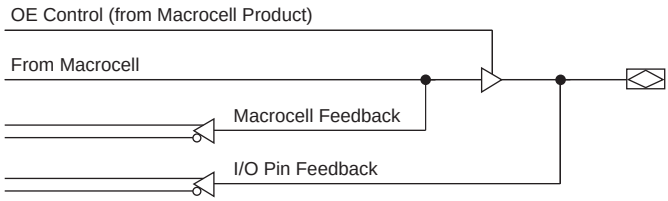
Programmable Interconnect Array

The multi-LAB MAX 5000 devices—EPM5064, EPM5128, EPM5130, and EPM5192 devices—use a PIA to route signals between the various LABs. The PIA, which is fed by all macrocell and I/O pin feedbacks, routes only the signals required for implementing logic in an LAB. While the routing delays of segmented routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 5000 PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

I/O Control Blocks

Each LAB has an I/O control block that allows each I/O pin to be individually configured for input, output, or bidirectional operation (see Figure 4). The I/O control block is fed by the macrocell array. A dedicated macrocell product term controls a tri-state buffer, which drives the I/O pin.

Figure 4. I/O Control Block



The MAX 5000 architecture provides dual I/O feedback in which macrocell and I/O pin feedbacks are independent, allowing maximum flexibility. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic. Using an I/O pin as an input in single-LAB devices reduces the number of available expanders by two. In multi-LAB devices, I/O pins feed the PIA directly.

Design Security

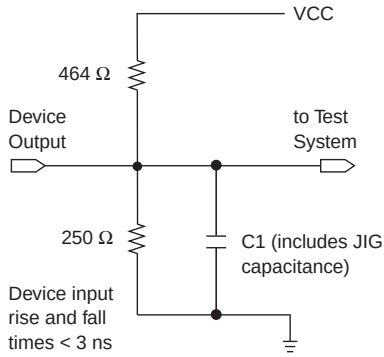
All MAX 5000 EPLDs contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EPROM cells is invisible. The security bit that controls this function, as well as all other program data, is reset only when the device is erased.

Generic Testing

MAX 5000 EPLDs are fully functionally tested. Complete testing of each programmable EPROM bit and all internal logic elements ensures 100% programming yield. Test patterns can be used and then erased during early stages of the device production flow. The devices also contain on-board logic test circuitry to allow verification of function and AC specifications during the production flow. AC test measurements are taken under conditions equivalent to those in Figure 5.

Figure 5. AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



Device Programming

All MAX 5000 EPLDs can be programmed on Windows-based PCs with the MAX+PLUS II Programmer, an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU checks continuity to ensure adequate electrical contact between the adapter and the device.

For more information, see the *Altera Programming Hardware Data Sheet*.

The MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text Editor or Waveform Editor to test a programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 5000 EPLD with the simulation results. This feature requires a device adapter with the "PLM-" prefix.

Data I/O, BP Microsystems, and other programming hardware manufacturers also offer programming support for Altera devices.

For more information, see *Programming Hardware Manufacturers.*

QFP Carrier & Development Socket

MAX 5000 devices in 100-pin QFP packages are shipped in special plastic carriers to protect the QFP leads. Each carrier can be used with a prototype development socket and programming hardware available from Altera or third-party programming manufacturers such as Data I/O and BP Microsystems. This carrier technology makes it possible to program, test, erase, and reprogram devices without exposing the leads to mechanical stress.

For detailed information and carrier dimensions, refer to the *QFP Carrier & Development Socket Data Sheet* and *Application Note 71 (Guidelines for Handling J-Lead & QFP Devices)*.

Operating Conditions

Tables 4 through 8 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 5000 devices.

Table 4. MAX 5000 Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	135	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		Plastic packages, under bias		135	° C

Table 5. MAX 5000 Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*(3)*, *(4)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		–0.3	V_{CC}+0.3	V
V_O	Output voltage		0	V_{CC}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

Table 6. MAX 5000 Device DC Operating Conditions *Note (5)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC *(6)*	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC *(6)*			0.45	V
I_I	Leakage current of dedicated inputs	$V_I = V_{CC}$ or ground	–10		10	µA
I_{OZ}	I/O pin tri-state output off-state current	$V_O = V_{CC}$ or ground	–40		40	µA

Table 7. EPM5032 MAX 5000 Device Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

Table 8. EPM5064, EPM5128, EPM5130 & EPM5192 MAX 5000 Device Capacitance

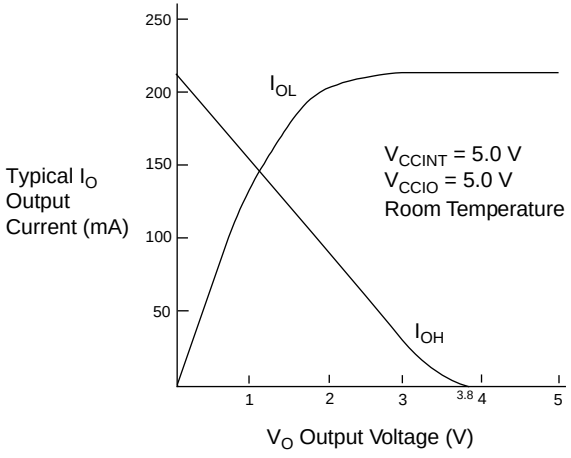
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time for MAX 5000 devices is 10 ms.
(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(6) The I_{OH} parameter refers to high-level TTL output current; the I_{OL} parameter refers to low-level TTL output current.

Figure 6 shows typical output drive characteristics of MAX 5000 devices.

Figure 6. Output Drive Characteristics of MAX 5000 Devices

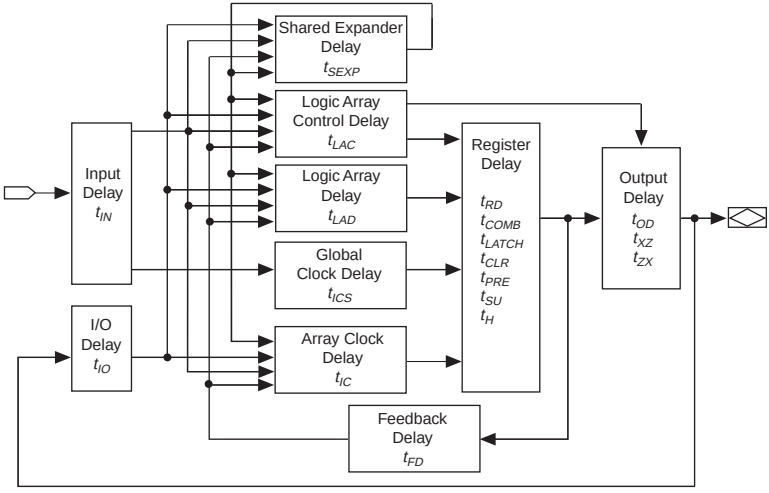


Timing Model

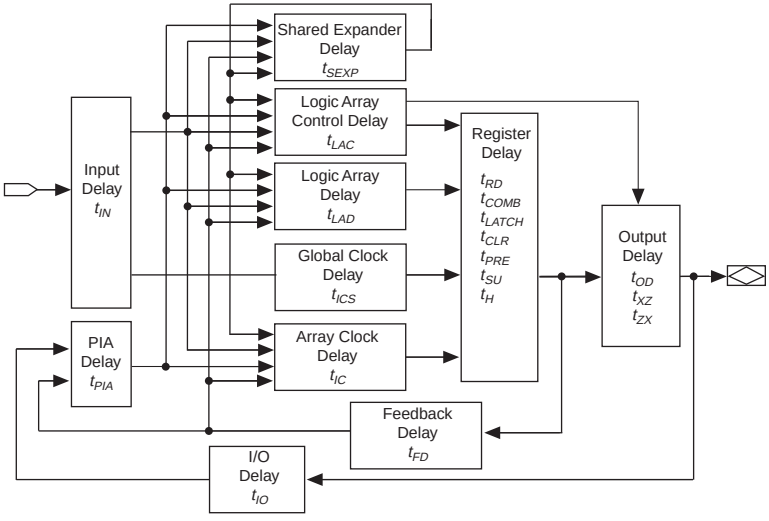
MAX 5000 EPLD timing can be analyzed with the MAX+PLUS II software, with a variety of other industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 7. MAX 5000 EPLDs have fixed internal delays that allow the designer to determine the worst-case timing for any design. The MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for system-level performance evaluation.

Figure 7. MAX 5000 Timing Model

Single-LAB EPLDs



Multi-LAB EPLDs



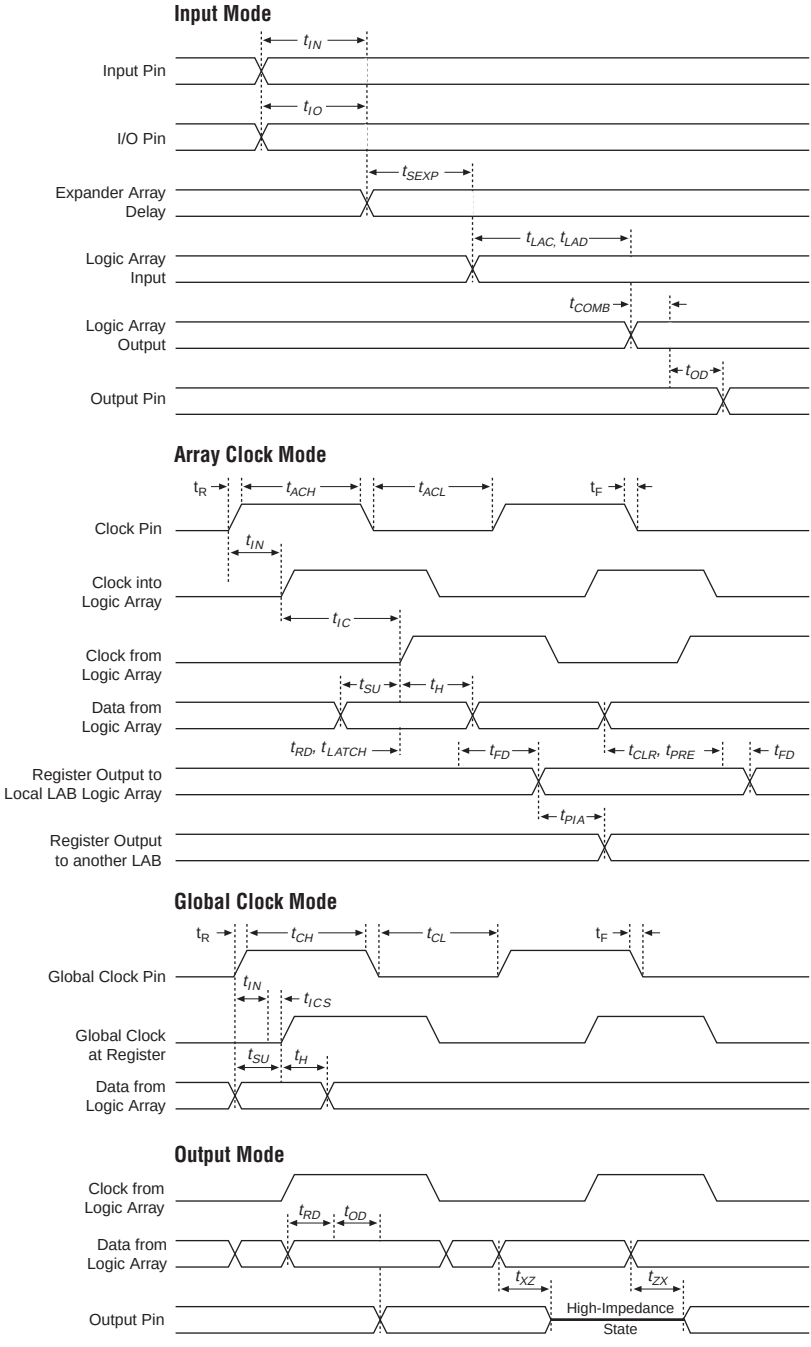
Timing information can be derived from the timing model and parameters for a particular EPLD. External timing parameters are calculated with the sum of internal parameters and represent pin-to-pin timing delays. Figure 8 shows the internal timing relationship for internal and external delay parameters.

See *Application Note 78 (Understanding MAX 5000 & Classic Timing)* for more information on EPLD timing.

Figure 8. Switching Waveforms

In multi-LAB EPLDs, I/O pins that are used as inputs traverse the PIA.

t_R and t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low.



Tables 9 and 10 show EPM 5032 timing parameters.

Table 9. EPM5032 External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-15		-20		-25		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		15.0		20.0		25.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		15.0		20.0		25.0	ns
t_{SU}	Global clock setup time		9.0		12.0		15.0		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		10.0		12.0		15.0	ns
t_{CH}	Global clock high time		6.0		7.0		8.0		ns
t_{CL}	Global clock low time		6.0		7.0		8.0		ns
t_{ASU}	Array clock setup time		5.0		6.0		8.0		ns
t_{AH}	Array clock hold time		5.0		6.0		8.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15.0		18.0		22.0	ns
t_{ACH}	Array clock high time	*(2)*	6.0		7.0		9.0		ns
t_{ACL}	Array clock low time		7.0		9.0		11.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(3)*	1.0		1.0		1.0		ns
t_{CNT}	Minimum global clock period			13.0		16.0		20.0	ns
f_{CNT}	Maximum internal global clock frequency	*(4)*	76.9		62.5		50.0		MHz
t_{ACNT}	Minimum array clock period			13.0		16.0		20.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(4)*	76.9		62.5		50.0		MHz
f_{MAX}	Maximum clock frequency	*(5)*	83.3		71.4		62.5		MHz

Table 10. EPM5032 Internal Timing Parameters *Note (6)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-15		-20		-25		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			3.0		5.0		7.0	ns
t_{IO}	I/O input pad and buffer delay			3.0		5.0		7.0	ns
t_{SEXP}	Expander array delay			8.0		10.0		15.0	ns
t_{LAD}	Logic array delay			7.0		10.0		13.0	ns
t_{LAC}	Logic control array delay			4.0		4.0		4.0	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		4.0		4.0		4.0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		7.0		7.0		7.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		7.0		7.0		7.0	ns
t_{SU}	Register setup time		4.0		4.0		5.0		ns
t_{LATCH}	Flow-through latch delay			1.0		1.0		1.0	ns
t_{RD}	Register delay			1.0		1.0		1.0	ns
t_{COMB}	Combinatorial delay			1.0		1.0		1.0	ns
t_{H}	Register hold time		5.0		8.0		10.0		ns
t_{IC}	Array clock delay			7.0		8.0		10.0	ns
t_{ICS}	Global clock delay			2.0		2.0		3.0	ns
t_{FD}	Feedback delay			1.0		1.0		1.0	ns
t_{PRE}	Register preset time			5.0		6.0		9.0	ns
t_{CLR}	Register clear time			5.0		6.0		9.0	ns

Table 11. EPM5064, EPM5128, EPM5130 & EPM5192 External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade *(7)*						Unit
			-1		-2		EPM5064 EPM5128 EPM5130 EPM5192		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		25.0		30.0		35.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		40.0		45.0		55.0	ns
t_{SU}	Global clock setup time		15.0		20.0		25.0		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14.0		16.0		20.0	ns
t_{CH}	Global clock high time		8.0		10.0		12.5		ns
t_{CL}	Global clock low time		8.0		10.0		12.5		ns
t_{ASU}	Array clock setup time		5.0		6.0		10.0		ns
t_{AH}	Array clock hold time		6.0		8.0		10.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25.0		30.0		35.0	ns
t_{ACH}	Array clock high time	*(2)*	11.0		14.0		16.0		ns
t_{ACL}	Array clock low time		9.0		11.0		14.0		ns
t_{CNT}	Minimum global clock period			20.0		25.0		30.0	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(3)*	2.0		2.0		2.0		ns
f_{CNT}	Maximum internal global clock frequency	*(4)*	50.0		40.0		33.3		MHz
t_{ACNT}	Minimum array clock period			20.0		25.0		30.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(4)*	50.0		40.0		33.3		MHz
f_{MAX}	Maximum clock frequency	*(5)*	62.5		50.0		40.0		MHz

Table 12. EPM5064, EPM5128, EPM5130 & EPM5192 Internal Timing Parameters *Note (6)*

Symbol	Parameter	Conditions	Speed Grade (7)						Unit
			-1		-2		EPM5064 EPM5128 EPM5130 EPM5192		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			5.0		7.0		11.0	ns
t_{IO}	I/O input pad and buffer delay			6.0		6.0		11.0	ns
t_{SEXP}	Expander array delay			12.0		14.0		20.0	ns
t_{LAD}	Logic array delay			12.0		14.0		14.0	ns
t_{LAC}	Logic control array delay			10.0		12.0		13.0	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5.0		5.0		6.0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		10.0		11.0		13.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10.0		11.0		13.0	ns
t_{SU}	Register setup time		6.0		8.0		12.0		ns
t_{LATCH}	Flow-through latch delay			3.0		4.0		4.0	ns
t_{RD}	Register delay			1.0		2.0		2.0	ns
t_{COMB}	Combinatorial delay			3.0		4.0		4.0	ns
t_{H}	Register hold time		4.0		6.0		8.0		ns
t_{IC}	Array clock delay			14.0		16.0		16.0	ns
t_{ICS}	Global clock delay			3.0		2.0		1.0	ns
t_{FD}	Feedback delay			1.0		1.0		2.0	ns
t_{PRE}	Register preset time			5.0		6.0		7.0	ns
t_{CLR}	Register clear time			5.0		6.0		7.0	ns
t_{PIA}	Programmable interconnect array delay			14.0		16.0		20.0	ns

Notes to tables:

(1) Operating conditions are specified in Table 5 on page 719.
(2) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(3) This parameter is a guideline that is sample-tested only. It is based on extensive device characterization and applies to both global and array clocking.
(4) For EPM5032 devices, this parameter is measured with a 32-bit counter programmed into the device. For EPM5064, EPM5128, EPM5130, and EPM5192 devices, this parameter is measured with a 16-bit counter programmed into each LAB.
(5) The f_{MAX} values represent the highest frequency for pipelined data.
(6) For information on internal timing parameters, refer to *Application Note 78 (Understanding MAX 5000 & Classic Timing)* in this data book.
(7) The EPM 5064, EPM 5128, EPM 5130, and EPM 5132 are listed without speed grade designators.

Figure 9 shows the typical supply current versus frequency of MAX 5000 devices.

Figure 9. I_{CC} vs. Frequency for MAX 5000 Devices (Part 1 of 2)

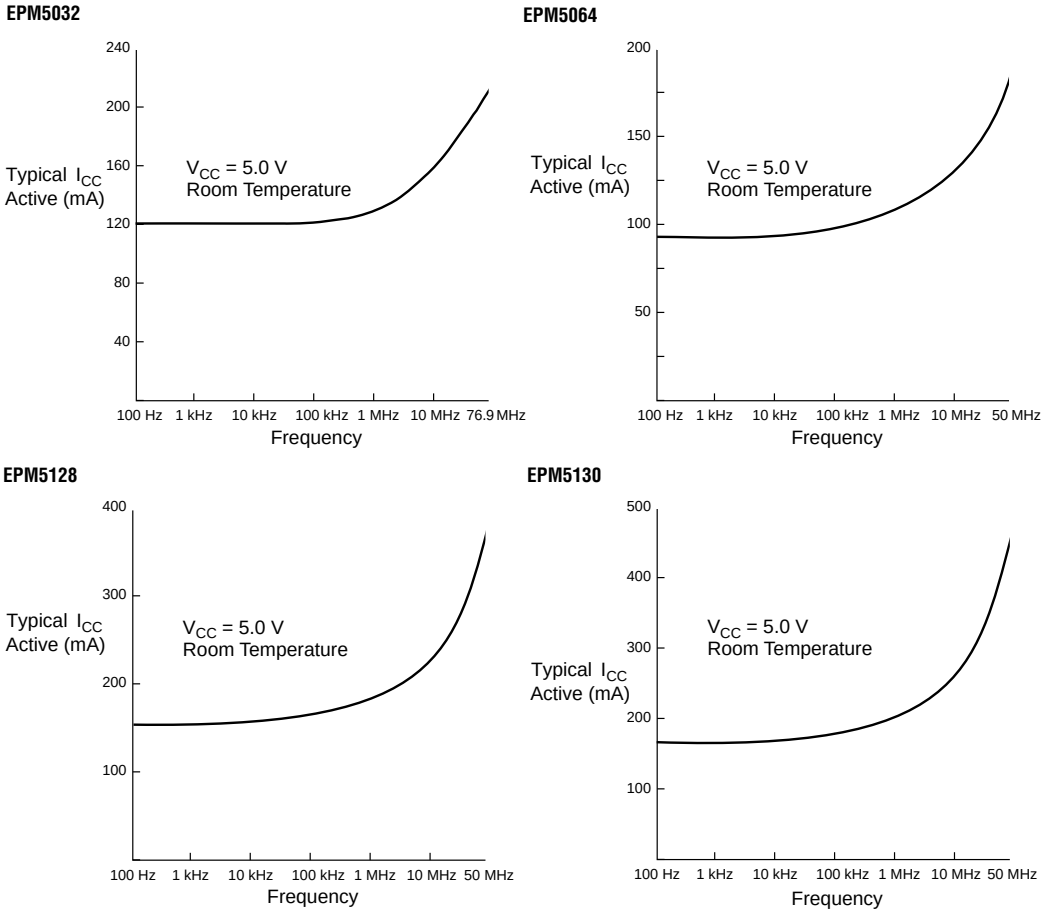
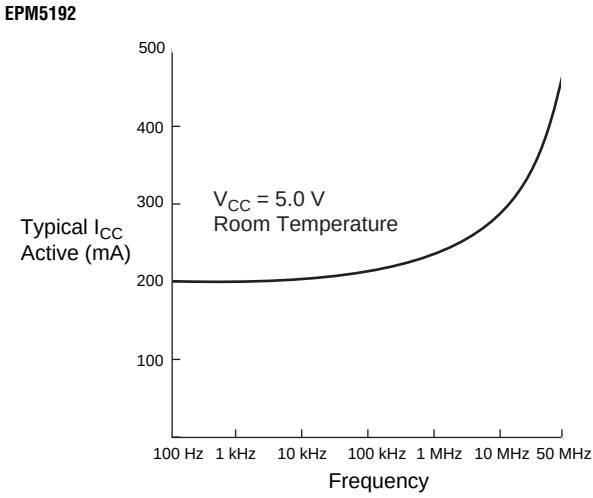


Figure 9. I_{CC} vs. Frequency for MAX 5000 Devices (Part 2 of 2)



Device Pin-Outs

Tables 13 through 22 show the pin names and numbers for the pins in each MAX 5000 device package.

Table 13. EPM5032 Dedicated Pin-Outs

Pin Name	28-Pin PLCC	28-Pin DIP
INPUT/CLK	9	2
INPUT	6, 7, 8, 20, 21, 22, 23	1, 13, 14, 15, 16, 27, 28
GND	15, 28	8, 21
VCC	1, 14	7, 22

Table 14. EPM5032 I/O Pin-Outs

LAB	MC	28-Pin PLCC	28-Pin DIP	LAB	MC	28-Pin PLCC	28-Pin DIP
A	1	10	3	B	17	24	17
	2	–	–		18	–	–
	3	11	4		19	25	18
	4	–	–		20	–	–
	5	12	5		21	26	19
	6	–	–		22	–	–
	7	13	6		23	27	20
	8	–	–		24	–	–
	9	16	9		25	2	23
	10	–	–		26	–	–
	11	17	10		27	3	24
	12	–	–		28	–	–
	13	18	11		29	4	25
	14	–	–		30	–	–
	15	19	12		31	5	26
	16	–	–		32	–	–

Table 15. EPM5064 Dedicated Pin-Outs

Pin Name	44-Pin PLCC
INPUT/CLK	34
INPUT	9, 11, 12, 13, 31, 33, 35
GND	10, 21, 32, 43
VCC	3, 14, 25, 36

Table 16. EPM5064 I/O Pin-Outs (Part 1 of 2)

LAB	MC	44-Pin PLCC	LAB	MC	44-Pin PLCC
A	1	2	B	17	15
	2	4		18	16
	3	5		19	17
	4	6		20	18
	5	7		21	19
	6	8		22	20
	7	–		23	22
	8	–		24	23
	9	–		25	–
	10	–		26	–
	11	–		27	–
	12	–		28	–
	13	–		29	–
	14	–		30	–
	15	–		31	–
	16	–		32	–

Table 16. EPM5064 I/O Pin-Outs (Part 2 of 2)

LAB	MC	44-Pin PLCC	LAB	MC	44-Pin PLCC
C	33	24	D	49	37
	34	26		50	38
	35	27		51	39
	36	28		52	40
	37	29		53	41
	38	30		54	42
	39	–		55	44
	40	–		56	1
	41	–		57	–
	42	–		58	–
	43	–		59	–
	44	–		60	–
	45	–		61	–
	46	–		62	–
	47	–		63	–
	48	–		64	–

Table 17. EPM5128 Dedicated Pin-Outs

Pin Name	68-Pin PLCC	68-Pin PGA
INPUT/CLK	1	B6
INPUT	2, 32, 34, 35, 36, 66, 68	A6, L4, L5, L6, K6, A8, A7
GND	16, 33, 50, 67	B7, E2, G10, K5
VCC	3, 20, 37, 54	B5, E10, G2, K7

Table 18. EPM5128 I/O Pin-Outs (Part 1 of 3)

LAB	MC	68-Pin PLCC	68-Pin PGA	LAB	MC	68-Pin PLCC	68-Pin PGA
A	1	4	A5	B	17	12	C2
	2	5	B4		18	13	C1
	3	6	A4		19	14	D2
	4	7	B3		20	15	D1
	5	8	A3		21	17	E1
	6	9	A2		22	–	–
	7	10	B2		23	–	–
	8	11	B1		24	–	–
	9	–	–		25	–	–
	10	–	–		26	–	–
	11	–	–		27	–	–
	12	–	–		28	–	–
	13	–	–		29	–	–
	14	–	–		30	–	–
	15	–	–		31	–	–
	16	–	–		32	–	–

Table 18. EPM5128 I/O Pin-Outs (Part 2 of 3)

LAB	MC	68-Pin PLCC	68-Pin PGA	LAB	MC	68-Pin PLCC	68-Pin PGA
C	33	18	F2	E	65	38	L7
	34	19	F1		66	39	K8
	35	21	G1		67	40	L8
	36	22	H2		68	41	K9
	37	23	H1		69	42	L9
	38	–	–		70	43	L10
	39	–	–		71	44	K10
	40	–	–		72	45	K11
	41	–	–		73	–	–
	42	–	–		74	–	–
	43	–	–		75	–	–
	44	–	–		76	–	–
	45	–	–		77	–	–
	46	–	–		78	–	–
	47	–	–		79	–	–
	48	–	–		80	–	–
D	49	24	J2	F	81	46	J10
	50	25	J1		82	47	J11
	51	26	K1		83	48	H10
	52	27	K2		84	49	H11
	53	28	L2		85	51	G11
	54	29	K3		86	–	–
	55	30	L3		87	–	–
	56	31	K4		88	–	–
	57	–	–		89	–	–
	58	–	–		90	–	–
	59	–	–		91	–	–
	60	–	–		92	–	–
	61	–	–		93	–	–
	62	–	–		94	–	–
	63	–	–		95	–	–
	64	–	–		96	–	–

Table 18. EPM5128 I/O Pin-Outs (Part 3 of 3)

LAB	MC	68-Pin PLCC	68-Pin PGA	LAB	MC	68-Pin PLCC	68-Pin PGA
G	97	52	F10	H	113	58	C10
	98	53	F11		114	59	C11
	99	55	E11		115	60	B11
	100	56	D10		116	61	B10
	101	57	D11		117	62	A10
	102	–	–		118	63	B9
	103	–	–		119	64	A9
	104	–	–		120	65	B8
	105	–	–		121	–	–
	106	–	–		122	–	–
	107	–	–		123	–	–
	108	–	–		124	–	–
	109	–	–		125	–	–
	110	–	–		126	–	–
	111	–	–		127	–	–
	112	–	–		128	–	–

Table 19. EPM5130 Dedicated Pin-Outs

Pin Name	84-Pin PLCC	100-Pin PGA	100-Pin PQFP
INPUT/CLK	1	C7	16
INPUT	2, 5, 6, 7, 36, 37, 38, 41, 42, 43, 44, 47, 48, 49, 78, 79, 80, 83, 84	A5, A7, A8, A9, A10, B5, B7, B9, C6, L7, L8, M5, M7, M9, N4, N5, N6, N7, N9	9, 10, 11, 14, 15, 16, 17, 20, 21, 22, 59, 60, 61, 64, 65, 66, 67, 70, 71, 72
GND	19, 20, 39, 40, 61, 62, 81, 82	B8, C8, F2, F3, H11, H12, L6, M6	12, 13, 37, 38, 62, 63, 87, 88
VCC	3, 4, 23, 24, 45, 46, 65, 66	A6, B6, F12, F13, H1, H2, M8, N8	18, 19, 43, 44, 68, 69, 93, 94

Table 20. EPM5130 I/O Pin-Outs (Part 1 of 3)

LAB	MC	84-Pin PLCC	100-Pin PGA	100-Pin PQFP	LAB	MC	84-Pin PLCC	100-Pin PGA	100-Pin PQFP
A	1	8	B13	1	B	17	14	A4	23
	2	9	C12	2		18	15	B4	24
	3	10	A13	3		19	16	A3	25
	4	11	B12	4		20	17	A2	26
	5	12	A12	5		21	18	B3	27
	6	13	B11	6		22	21	A1	28
	7	–	A11	7		23	–	B2	29
	8	–	B10	8		24	–	B1	30
	9	–	–	–		25	–	–	–
	10	–	–	–		26	–	–	–
	11	–	–	–		27	–	–	–
	12	–	–	–		28	–	–	–
	13	–	–	–		29	–	–	–
	14	–	–	–		30	–	–	–
	15	–	–	–		31	–	–	–
	16	–	–	–		32	–	–	–

Table 20. EPM5130 I/O Pin-Outs (Part 2 of 3)

LAB	MC	84-Pin PLCC	100-Pin PGA	100-Pin PQFP	LAB	MC	84-Pin PLCC	100-Pin PGA	100-Pin PQFP
C	33	22	C2	31	E	65	50	M1	51
	34	25	C1	32		66	51	L2	52
	35	26	D2	33		67	52	N1	53
	36	27	D1	34		68	53	M2	54
	37	28	E2	35		69	54	N2	55
	38	29	E1	36		70	55	M3	56
	39	–	F1	39		71	–	N3	57
	40	–	G2	40		72	–	M4	58
	41	–	–	–		73	–	–	–
	42	–	–	–		74	–	–	–
	43	–	–	–		75	–	–	–
	44	–	–	–		76	–	–	–
	45	–	–	–		77	–	–	–
	46	–	–	–		78	–	–	–
	47	–	–	–		79	–	–	–
	48	–	–	–		80	–	–	–
D	49	30	G3	41	F	81	56	N10	73
	50	31	G1	42		82	57	M10	74
	51	32	H3	45		83	58	N11	75
	52	33	J1	46		84	59	N12	76
	53	34	J2	47		85	60	M11	77
	54	35	K1	48		86	63	M13	78
	55	–	K2	49		87	–	M12	79
	56	–	L1	50		88	–	M13	80
	57	–	–	–		89	–	–	–
	58	–	–	–		90	–	–	–
	59	–	–	–		91	–	–	–
	60	–	–	–		92	–	–	–
	61	–	–	–		93	–	–	–
	62	–	–	–		94	–	–	–
	63	–	–	–		95	–	–	–
	64	–	–	–		96	–	–	–

Table 20. EPM5130 I/O Pin-Outs (Part 3 of 3)

LAB	MC	84-Pin PLCC	100-Pin PGA	100-Pin PQFP	LAB	MC	84-Pin PLCC	100-Pin PGA	100-Pin PQFP
G	97	64	L12	81	H	113	72	G11	91
	98	67	L13	82		114	73	G13	92
	99	68	K12	83		115	74	F11	95
	100	69	K13	84		116	75	E13	96
	101	70	J12	85		117	76	E12	97
	102	71	J13	86		118	77	D13	98
	103	–	H13	89		119	–	D12	99
	104	–	G12	90		120	–	C13	100
	105	–	–	–		121	–	–	–
	106	–	–	–		122	–	–	–
	107	–	–	–		123	–	–	–
	108	–	–	–		124	–	–	–
	109	–	–	–		125	–	–	–
	110	–	–	–		126	–	–	–
	111	–	–	–		127	–	–	–
	112	–	–	–		128	–	–	–

Table 21. EPM5192 Dedicated Pin-Outs

Pin Name	84-Pin PLCC	84-Pin PGA
INPUT/CLK	1	A6
INPUT	2, 41, 42, 43, 44, 83, 84	A5, K6, J6, J7, L7, C7, C6
GND	18, 19, 39, 40, 60, 61, 81, 82	A7, B7, E1, E2, G10, G11, K5, L5
VCC	3, 24, 45, 66	B5, E10, G2, K7

Table 22. EPM5192 I/O Pin-Outs (Part 1 of 4)

LAB	MC	84-Pin PLCC	84-Pin PGA	LAB	MC	84-Pin PLCC	84-Pin PGA
A	1	4	C5	B	17	12	C2
	2	5	A4		18	13	B1
	3	6	B4		19	14	C1
	4	7	A3		20	15	D2
	5	8	A2		21	–	–
	6	9	B3		22	–	–
	7	10	A1		23	–	–
	8	11	B2		24	–	–
	9	–	–		25	–	–
	10	–	–		26	–	–
	11	–	–		27	–	–
	12	–	–		28	–	–
	13	–	–		29	–	–
	14	–	–		30	–	–
	15	–	–		31	–	–
	16	–	–		32	–	–

Table 22. EPM5192 I/O Pin-Outs (Part 2 of 4)

LAB	MC	84-Pin PLCC	84-Pin PGA	LAB	MC	84-Pin PLCC	84-Pin PGA
C	33	16	D1	E	65	27	H2
	34	17	E3		66	28	J1
	35	20	F2		67	29	K1
	36	21	F3		68	30	J2
	37	–	–		69	–	–
	38	–	–		70	–	–
	39	–	–		71	–	–
	40	–	–		72	–	–
	41	–	–		73	–	–
	42	–	–		74	–	–
	43	–	–		75	–	–
	44	–	–		76	–	–
	45	–	–		77	–	–
	46	–	–		78	–	–
	47	–	–		79	–	–
	48	–	–		80	–	–
D	49	22	G3	F	81	31	L1
	50	23	G1		82	32	K2
	51	25	F1		83	33	K3
	52	26	H1		84	34	L2
	53	–	–		85	35	L3
	54	–	–		86	36	K4
	55	–	–		87	37	L4
	56	–	–		88	38	J5
	57	–	–		89	–	–
	58	–	–		90	–	–
	59	–	–		91	–	–
	60	–	–		92	–	–
	61	–	–		93	–	–
	62	–	–		94	–	–
	63	–	–		95	–	–
	64	–	–		96	–	–

Table 22. EPM5192 I/O Pin-Outs (Part 3 of 4)

LAB	MC	84-Pin PLCC	84-Pin PGA	LAB	MC	84-Pin PLCC	84-Pin PGA
G	97	46	L6	I	129	58	H11
	98	47	L8		130	59	F10
	99	48	K8		131	62	G9
	100	49	L9		132	63	F9
	101	50	L10		133	–	–
	102	51	K9		134	–	–
	103	52	L11		135	–	–
	104	53	K10		136	–	–
	105	–	–		137	–	–
	106	–	–		138	–	–
	107	–	–		139	–	–
	108	–	–		140	–	–
	109	–	–		141	–	–
	110	–	–		142	–	–
	111	–	–		143	–	–
	112	–	–		144	–	–
H	113	54	J10	J	145	64	F11
	114	55	K11		146	65	E11
	115	56	J11		147	67	E9
	116	57	H10		148	68	D11
	117	–	–		149	–	–
	118	–	–		150	–	–
	119	–	–		151	–	–
	120	–	–		152	–	–
	121	–	–		153	–	–
	122	–	–		154	–	–
	123	–	–		155	–	–
	124	–	–		156	–	–
	125	–	–		157	–	–
	126	–	–		158	–	–
	127	–	–		159	–	–
	128	–	–		160	–	–

Table 22. EPM5192 I/O Pin-Outs (Part 4 of 4)

LAB	MC	84-Pin PLCC	84-Pin PGA	LAB	MC	84-Pin PLCC	84-Pin PGA
K	161	69	D10	L	177	73	A11
	162	70	C11		178	74	B10
	163	71	B11		179	75	B9
	164	72	C10		180	76	A10
	165	–	–		181	77	A9
	166	–	–		182	78	B8
	167	–	–		183	79	A8
	168	–	–		184	80	B6
	169	–	–		185	–	–
	170	–	–		186	–	–
	171	–	–		187	–	–
	172	–	–		188	–	–
	173	–	–		189	–	–
	174	–	–		190	–	–
	175	–	–		191	–	–
	176	–	–		192	–	–