PRODUCT SPECIFICATION

GM71256

262,144 x 1BIT DYNAMIC RAM

Description

The GM71256 is high speed, high performance dynamic RAM,organized 262,144 and manufactured using advanced NMOS silicon-gate technology. The design is optimised for both high speed and low power dissipation.

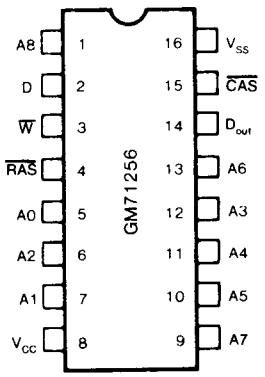
The GM71256 features multiplexed addressing, and all input signals, include clocks, are TTL-compatible, input and output signals are the same polarity, and the 3-state output buffer is $\overline{CAS}$ controlled. The Hi-C single transistor memory cell is used to enhance signal margin and reduce the α particle included soft error. This device offers page mode operation which allows high speed random access memory cells within the same row.

The GM71256 features single power supply of 5V±10% tolerance and is available a 16 pin plastic DIP or cerdip

Features

- **262,144 words x 1-bit organization**
- **100/120/150 ns access time from $\overline{RAS}$**
- **50/60/75 ns access time from $\overline{CAS}$**
- **385/360/330 mW active power, Page Mode,**
- **25 mW standby power**
- **Multiplexed address inputs**
- **±10% power supply tolerance**
- **Read-Modify-Write capabilities**
- **$\overline{RAS}$ Only Refresh/Hidden Refresh**
- **Latched or high impedance output during refresh**
- **256 refresh cycles/4ms**
- **Page Mode operation**

Pin Configuration



Pin Description

V_{CC}	+5V Supply
D	Data In
D_{out}	Data Out
A_0-A_8	Address Input (0-8)
$\overline{W}$	Write Enable
$\overline{RAS}$	Row Enable
$\overline{CAS}$	Column Enable
V_{SS}	Ground
NC	No Connect

Absolute Maximum Ratings*

PARAMETER	SYMBOL	VALUE	UNIT
Voltage Range on V_{CC} Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Power Dissipation	PD	1.0	W
Case Operating Temperature Range	T_C	0 to 85	°C
Ambient Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range**	T_{stg}		
Ceramic Package		−65 to +160	°C
Plastic Package		−55 to +120	°C
Short Circuit Output Current	I_{OS}	50	mA

* Maximum Ratings are defined as the limiting conditions that the user can apply to the device under all variations of circuit and environmental conditions. If any rating is exceeded, permanent damage to the device may result. Extended operation at any of these conditions may result in reduced reliability.

** Bonding or soldering of the external pins of these devices can be performed safely at temperatures up to 300°C.

Recommended Opreating Conditions: (T_A=0 to 70°C)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Supply Voltages	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V
Input Voltages* High Level—All Inputs (Logic 1) Low Level—All Inputs (Logic 0)	 V_{IH} V_{IL}	 2.4 −1.0	 — —	 6.5 0.8	 V V
Refresh Cycle Time**	t_{REF}	—	—	4.0	ms

* Application of invalid levels may destroy stored information during that cycle as well as the first cycle using valid levels. Data out is indeterminate.

** Addresses A0-A7 are used for refresh. A8 must be a valid one or zero.

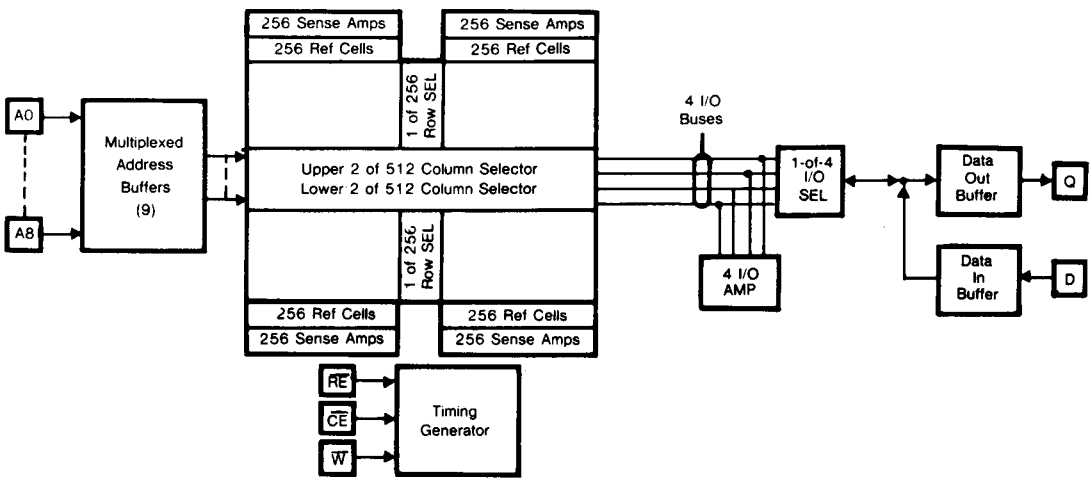


Figure 1. GM71256 Dynamic RAM Block Diagram

Electrical Characteristics: (V_{CC}=5V ±10%, V_{SS}=0V, T_A=0 to 70°C)

PARAMETER	SYMBOL	GM71256-10		GM71256-12		GM71256-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Output Voltages								
Low Level (I_{OL}=4.2mA)	V_{OL}	—	0.4	—	0.4	—	0.4	V
High Level (I_{OH}=−5.0mA)	V_{OH}	2.4	—	2.4	—	2.4	—	V
Power Supply Currents Operating Current (Average Operating Current $\overline{RAS}$ & $\overline{CAS}$ Cycling, t_{RC}=minimum)	I_{CC1}	—	70*	—	65*	—	60*	mA
Standby Current ($\overline{RAS}$=V_{IH}, Q=High Impedance)	I_{CC2}	—	4.5	—	4.5	—	4.5	mA
Refresh Current (Average Operating Current, Refresh Mode Operation) $\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}, t_{RC}=min.	I_{CC3}	—	55*	—	50*	—	45*	mA
Page Mode Current (Average Operating Current, Page Mode Operation, $\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling, t_{PC}=minimum)	I_{CC4}	—	50*	—	45*	—	40*	mA
Input Leakage Current (V_{CC}=5.5 V, V_I=0 to 6.5 V, All other leads at 0 V)	I_I	−10	10	−10	10	−10	10	μA
Output Leakage Current (Q=High Impedance, V_Q=0 to V_{CC})	I_O	−10	10	−10	10	−10	10	μA
Input Capacitance (A0-A8)**	C_{11}	—	5	—	5	—	5	pF
Input Capacitance (D, $\overline{W}$ Leads)**	C_{12}	—	5	—	5	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$ Leads)**	C_{13}	—	10	—	10	—	10	pF
Output Capacitance (Q Lead)**	C_O	—	7	—	7	—	7	pF

* Maximum occurs at T_A=0°C. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} are specified with output open-circuited.
** Parameter periodically sampled and not 100% tested.

Timing Characteristics: (V_{CC}=5V ±10%, V_{SS}=0V, T_A=0 to 70°C) (Notes 1, 2, and 3)

DESCRIPTION	SYMBOL	JEDEC SYMBOL	GM71256-10		GM71256-12		GM71256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
Random Read/Write Cycle Time	t_{RC}	t_{RELREL}	200	—	220	—	260	—	ns
Access Time from $\overline{RAS}$ (Notes 4 & 5)	t_{RAC}	t_{RELQV}	—	100	—	120	—	150	ns
Access Time from $\overline{CAS}$ (Notes 5 & 6)	t_{CAC}	t_{CELQV}	—	50	—	60	—	75	ns
Output Buffer Time Off Delay (Note 7)	t_{OFF}	t_{CEHQZ}	0	20	0	30	0	30	ns
Transition Time	t_T	t_T	2	50	2	50	2	50	ns
$\overline{RAS}$ Precharge Time	t_{RP}	t_{REHREL}	90	—	90	—	100	—	ns
$\overline{RAS}$ Pulse Width	t_{RAS}	t_{RELREH}	100	10000	120	10000	150	10000	ns
$\overline{RAS}$ Hold Time	t_{RSH}	t_{CELREH}	50	—	60	—	75	—	ns
$\overline{CAS}$ Pulse Width (Note 8)	t_{CAS}	t_{CELCEH}	50	10000	60	10000	75	10000	ns
$\overline{CAS}$ Hold Time	t_{CSH}	t_{RELCEH}	100	—	120	—	150	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay (Note 4)	t_{RCD}	t_{RELCEL}	25	50	25	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	t_{CEHREL}	0	—	0	—	0	—	ns
Row Address Setup Time	t_{ASR}	t_{RAVREL}	0	—	0	—	0	—	ns
Row Address Hold Time	t_{RAH}	t_{RELRAX}	15	—	15	—	15	—	ns
Column Address Setup Time	t_{ASC}	t_{CAVCEL}	0	—	0	—	0	—	ns
Column Address Hold Time	t_{CAH}	t_{CELCAX}	20	—	25	—	30	—	ns
Column Address Hold Time Ref. to $\overline{RAS}$	t_{AR}	t_{RELCAX}	75	—	90	—	105	—	ns
Read Command Hold Time Ref. to $\overline{RAS}$	t_{RRH}	t_{REHWX}	10	—	10	—	10	—	ns
Read Command Setup Time	t_{RCS}	t_{WHCEL}	0	—	0	—	0	—	ns
Read Command Hold Time Ref. to $\overline{CAS}$	t_{RCH}	t_{CEHWX}	0	—	0	—	0	—	ns
Write Command Hold Time	t_{WCH}	t_{CELWX}	15	—	20	—	25	—	ns
Write Command Hold Time Ref. to $\overline{RAS}$	t_{WCR}	t_{RELWX}	85	—	100	—	120	—	ns
Write Command Pulse Width	t_{WP}	t_{WLWH}	15	—	20	—	25	—	ns
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	t_{WLREH}	30	—	35	—	45	—	ns
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	t_{WLCEH}	20	—	30	—	40	—	ns
Data In Setup Time	t_{DS}	t_{DVCEL}	0	—	0	—	0	—	ns
Data In Hold Time	t_{DH}	t_{CELDX}	15	—	20	—	25	—	ns
Data In Hold Time Ref. to $\overline{RAS}$	t_{DHR}	t_{RELDX}	85	—	100	—	120	—	ns
Write Command Setup Time (Note 9)	t_{WCS}	t_{WLCEL}	0	—	0	—	0	—	ns
$\overline{CAS}$ to $\overline{W}$ Delay (Read-Modify-Write)	t_{CWD}	t_{CELWL}	25	—	30	—	35	—	ns
$\overline{RAS}$ to $\overline{W}$ Delay (Read-Modify-Write) (Note 6)	t_{RWD}	t_{RELWL}	75	—	100	—	125	—	ns
Data In Hold Time (Read-Modify-Write) (Note 6)	t_{DH}	t_{WLDX}	20	—	20	—	20	—	ns
Data In Setup Time (Read-Modify-Write)	t_{DS}	t_{DVWL}	0	—	0	—	0	—	ns
Refresh Period	t_{REF}	t_R	—	4.0	—	4.0	—	4.0	ms
Cycle Time (Read-Modify-Write)	t_{RMW}	$t_{WRELREL}$	245	—	260	—	310	—	ns

DESCRIPTION	SYMBOL	JEDEC SYMBOL	GM71256-10		GM71256-12		GM71256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
PAGE MODE OPTION									
Page Mode Cycle Time	t_{PC}	t_{CELCEL}	120	—	130	—	145	—	ns
$\overline{CAS}$ Precharge Time	t_{CP}	t_{CEHCEL}	45	—	50	—	60	—	ns

Notes:

1. Timing specifications given assume t_T = 5ns.
2. V_{IH} (min), V_{IL} (max) are reference levels for timing specifications or inputs signals. Transition times are to be measured between these reference levels.
3. An initial pause of 100 μs followed by a minimum of 8 refresh cycles is necessary after V_{CC} is applied, to achieve proper device operation. Address A0-A7 are used for refresh. A8 must be a valid one or zero.
4. For $t_{RELCEL} > t_{RELCEL}$ (max.), t_{RELQV} will increase by the amount that t_{RELCEL} (max.) is exceded.
5. Q load assumed to be equivalent to 2 TTL loads and 100 pF.
6. Assumes $t_{RELCEL} \geq t_{RELCEL}$ (max.)
7. t_{CEHQZ} (max.) defines the time at which Q achieves the open circuit condition.
8. $\overline{CAS}$ can be held at Logic 0 for an indefinite time for latched output during refresh. However, t_{RELRAX} must be increased to 100ns.
9. Non-restrictive operating parameter. If $t_{WLCEL} \geq t_{WLCEL}$ (min.), the cycle is an early write cycle and the dat out (Q) will remain an open circuit (high impedance) for the entire cycle. If $t_{CELWL} \geq t_{CELWL}$ (min.) and $t_{RELWL} \geq t_{RELWL}$ (min.), the cycle is a read-write cycle and the data out (Q) will validly reproduce the data contained in the selected cell. If neither of the above sets or conditions is satisfied, data out will be indeterminate.

Timing Waveforms

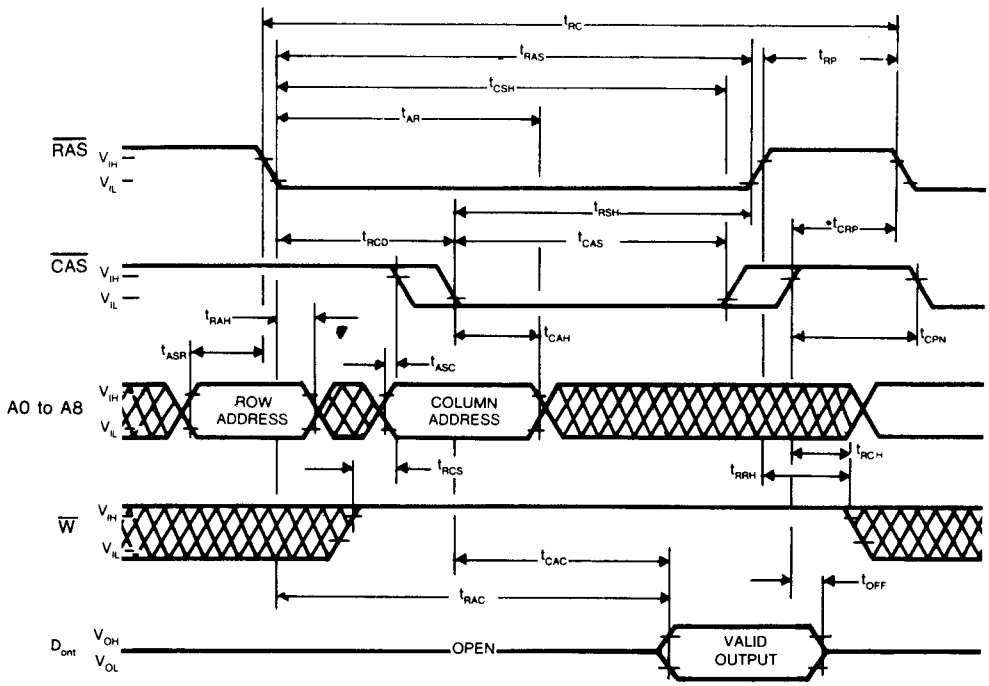


Figure 2 Read Cycle

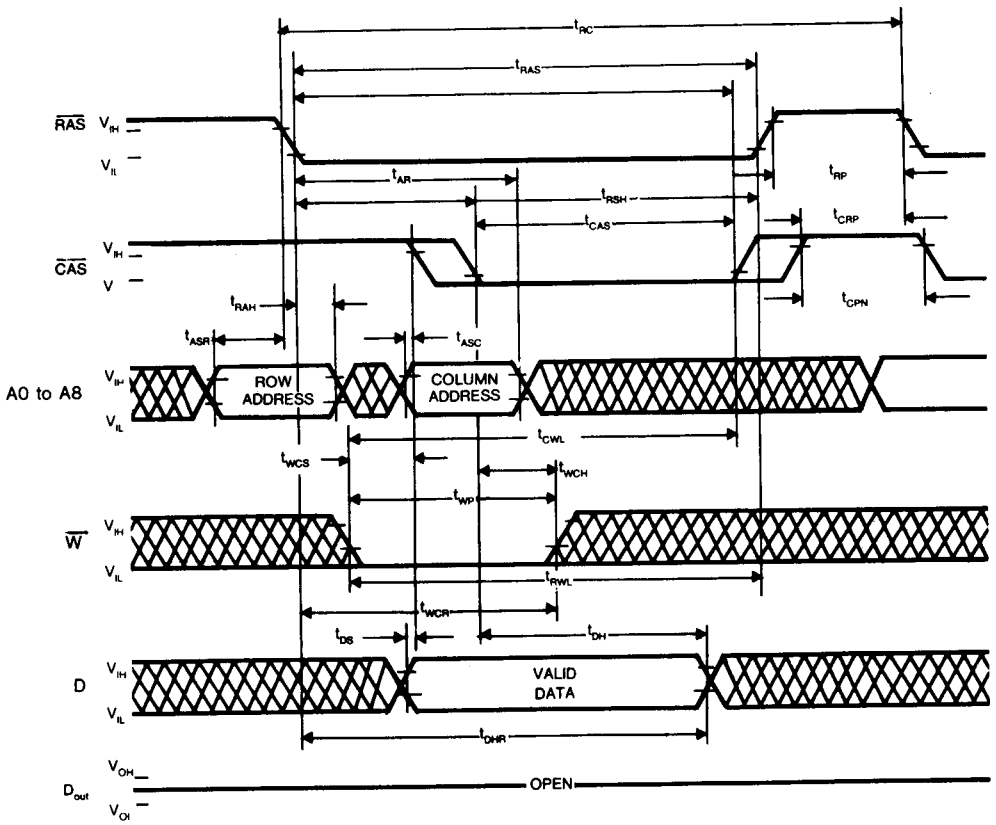


Figure 3. Write Cycle (Early Write)

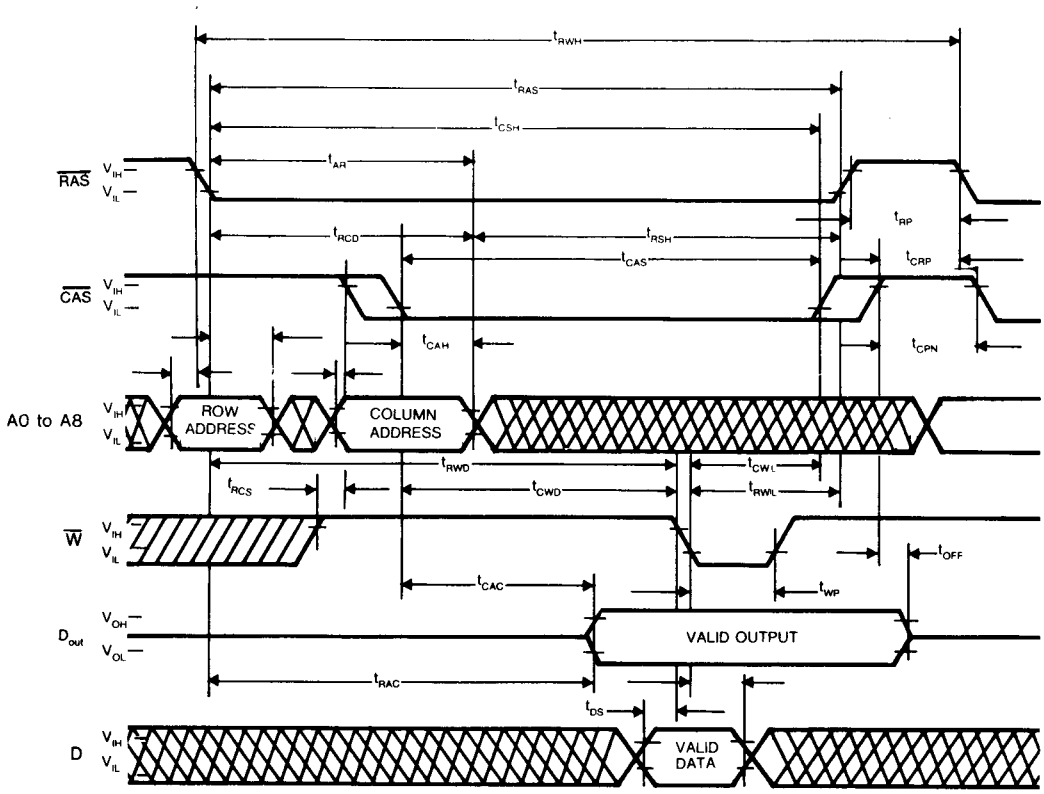
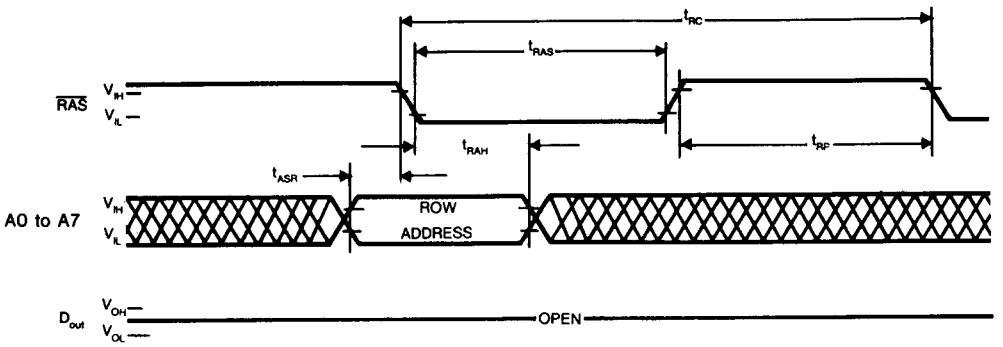


Figure 4. Read-Write/Read-Modify-Write Cycle



NOTE: Input $\overline{CS} \geq V_{IH}$, Input $\overline{W}$= Don't Care

Figure 5. $\overline{RAS}$ Only Refresh Cycle (Note 3)

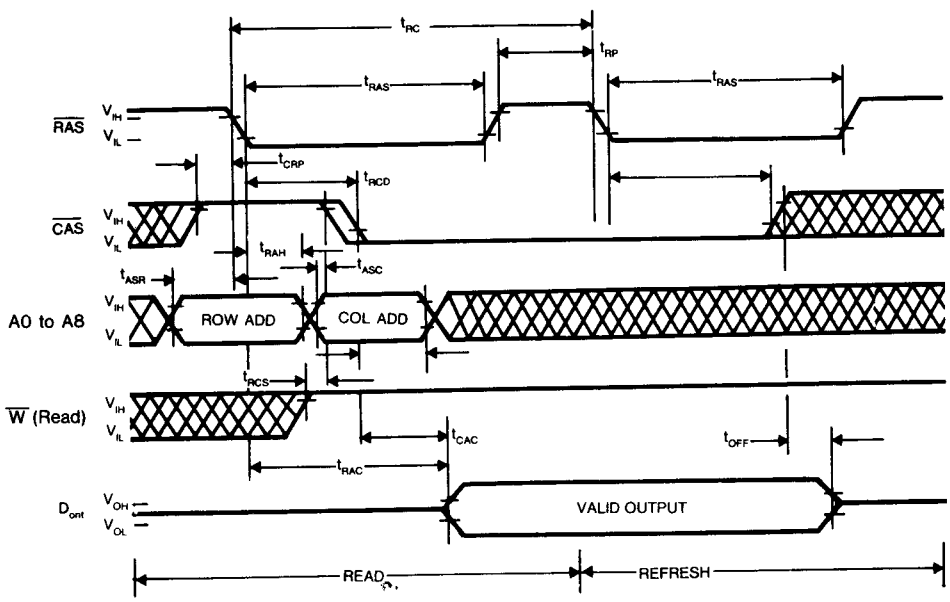


Figure 6. Hidden Refresh Cycle (Notes 3 and 8)

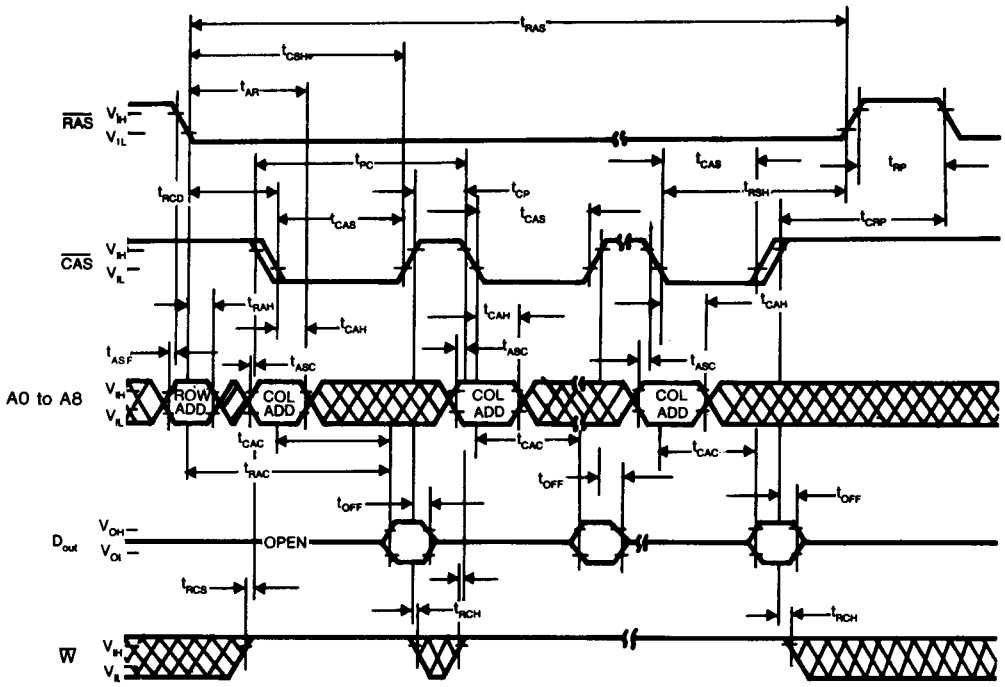


Figure 7. Page Mode Read Cycle

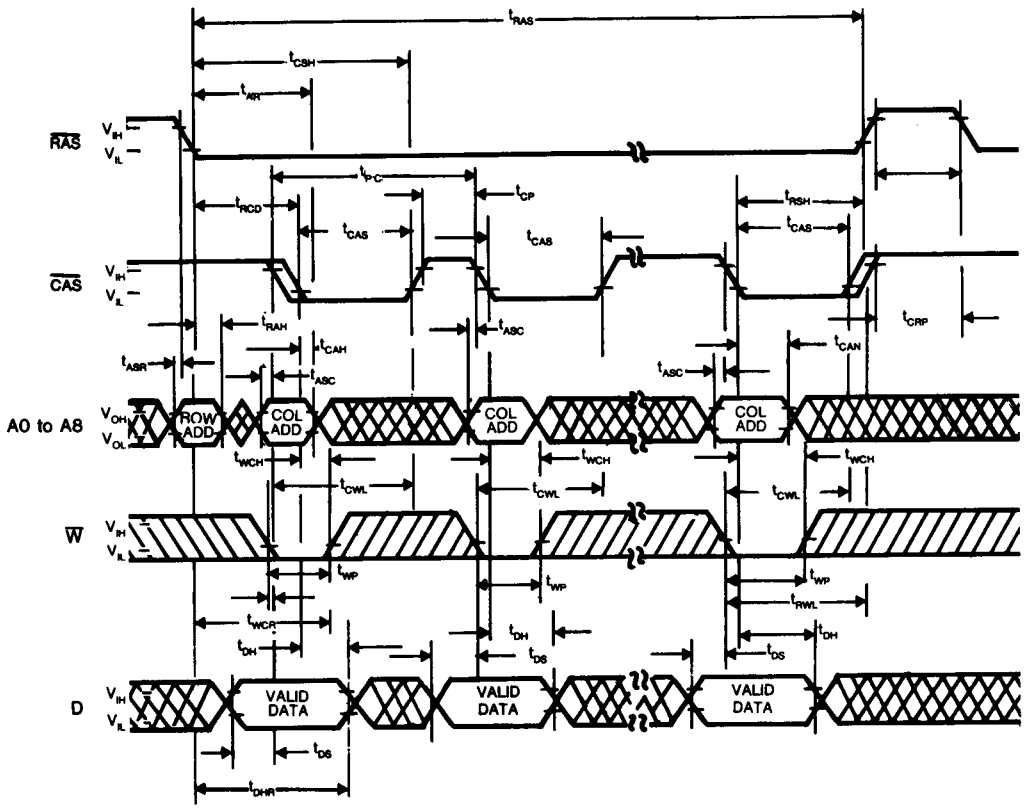


Figure 8. Page Mode Write Cycle

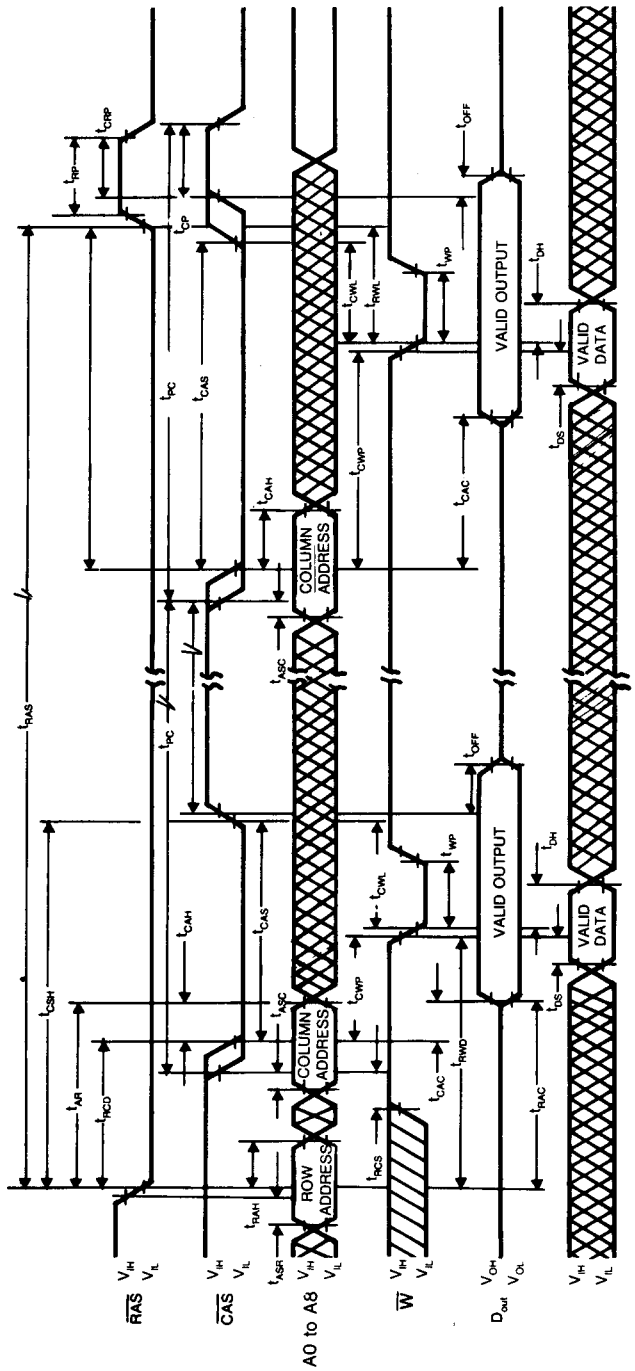
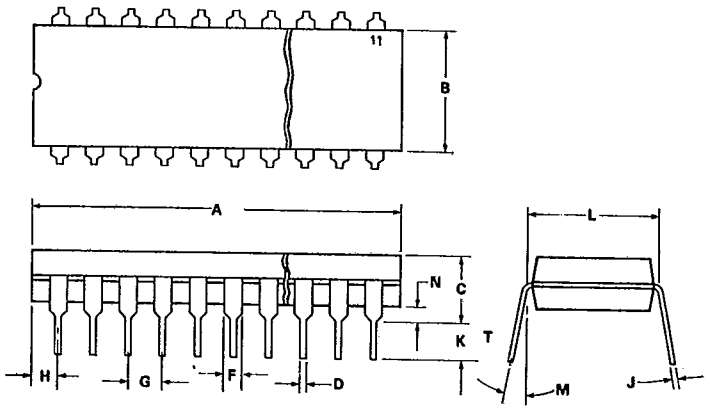


Figure 9. Page Mode Read-Modify-Write Cycle

T-90-20

PACKAGE DIMENSION

PLASTIC DIP



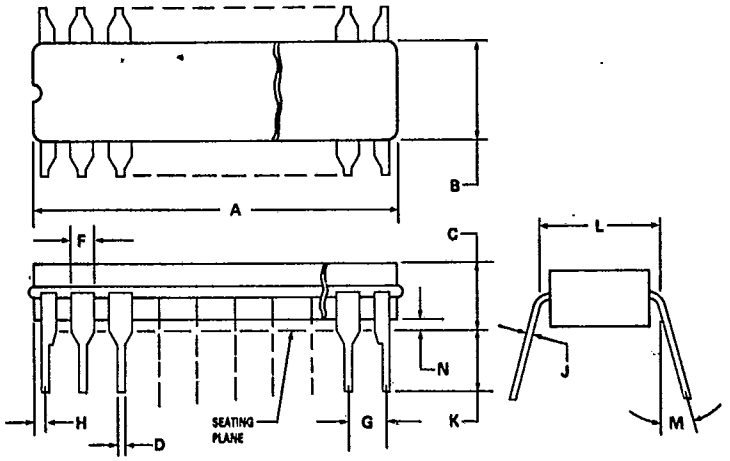
(UNIT: INCHES)

SYMBOL	16 PIN		18 PIN		20 PIN		22 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.738	0.752	0.875	0.900	1.013	1.040	1.095	1.150
B	0.245	0.255	0.245	0.255	0.263	0.273	0.260	0.287
C	0.143	0.152	0.145	0.162	0.143	0.152	0.145	0.160
D	TYP. 0.018		TYP. 0.018		TYP. 0.018		TYP. 0.018	
F	TYP. 0.063		TYP. 0.060		TYP. 0.065		TYP. 0.060	
G	0.09	0.11	0.09	0.11	0.09	0.11	0.09	0.11
H	0.015	0.030	0.04	0.05	0.058	0.066	—	0.075
J	0.009	0.014	0.009	0.015	0.009	0.010	0.009	0.010
K	0.125	0.145	0.125	0.130	0.125	0.132	0.125	0.142
L	0.300 BSC		0.300 BSC		0.300 BSC		0.300 BSC	
M	0°	10°	0°	10°	0°	10°	0°	10°
N	0.015	—	0.015	—	0.015	—	0.015	

SYMBOL	24 PIN		28 PIN					
	MIN	MAX	MIN	MAX				
A	1.243	1.260	1.415	1.460				
B	0.535	0.545	0.535	0.545				
C	0.158	0.170	0.158	0.170				
D	TYP. 0.018		TYP. 0.018					
F	TYP. 0.060		TYP. 0.060					
G	0.09	0.11	0.09	0.11				
H	0.06	0.075	0.06	0.076				
J	0.009	0.015	0.009	0.015				
K	0.125	0.132	0.125	0.132				
L	0.600	0.625	0.600	0.620				
M	0°	10°	0°	10°				
N	0.008	—	0.008	—				

PACKAGE DIMENSION

CER DIP

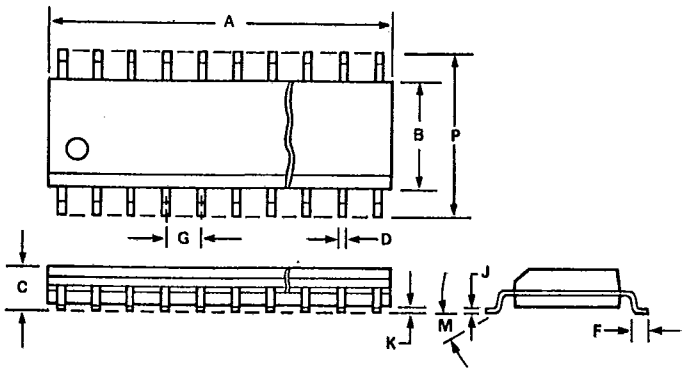


(UNIT : INCHES)

SYMBOL	16 PIN		20 PIN		24 PIN		28 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.753	0.785	0.940	0.985	1.240	1.290	1.440	1.485
B	0.272	0.294	0.265	0.306	0.514	0.526	0.514	0.598
C	0.165	0.200	0.165	0.200	0.165	0.200		0.225
D	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.023
F	0.055	0.065	0.055	0.065	0.055	0.065	0.055	0.065
G	0.09	0.11	0.09	0.11	0.09	0.11	0.09	0.11
H	0.012	0.060	0.012	0.060	0.040	0.098	0.040	0.098
J	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
K	0.125	0.20	0.125	0.20	0.125	0.20	0.125	0.20
L	0.29	0.32	0.29	0.32	0.590	0.620	0.590	0.620
M	0'	10'	0'	10'	0'	10'	0'	10'
N	0.02	0.06	0.02	0.07	0.02	0.07	0.02	0.07

PACKAGE DIMENSION

SOP



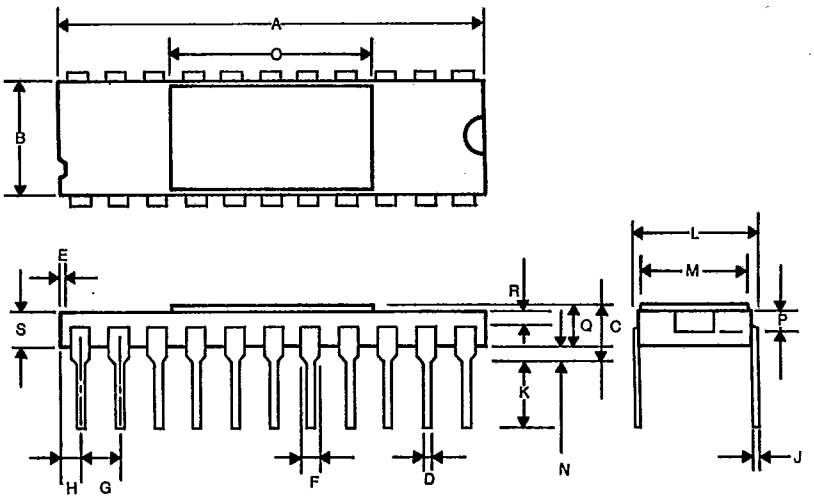
(UNIT : INCHES)

CODE NO.	20 F		24 F		24 FW			
PIN	20 PIN		24 PIN		24 PIN			
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX		
A	0.496	0.510	0.602	0.614	0.622	0.638		
B	0.292	0.299	0.292	0.299	TYP. 0.331			
C	0.097	0.104	0.097	0.104	—	0.098		
D	0.014	0.019	0.014	0.019	0.012	0.018		
F	0.018	0.035	0.018	0.035	TYP 0.039			
G	0.050 BSC		0.050 BSC		0.050 BSC			
J	0.010 BSC		0.010 BSC		0.010 BSC			
K	0.004	0.008	0.0055	0.0115	0.004			
P	0.400	0.410	0.400	0.410	*0.453	0.477		
M	0′	8′	0′	8′	—	—		

CODE NO.	28 F		28 FW					
PIN	28 PIN		28 PIN					
SYMBOL	MIN	MAX	MIN	MAX				
A	0.703	0.712	0.720	0.750				
B	0.292	0.289	TYP. 0.331					
C	0.097	0.104		0.098				
D	0.014	0.019	0.012	0.018				
F	0.018	0.035	TYP. 0.039					
G	0.050 BSC		0.050 BSC					
J	0.010 BSC		0.010 BSC					
K	0.0055	0.0115	0.004	—				
P	0.400	0.410	0.453	0.477				
M	0′	8′	—	—				

PACKAGE DIMENSION

SIDE BRAZED T-90-20



(UNIT: INCHES)

SYMBOL	22 PIN	
	MIN	MAX
A	1.088	1.112
B	0.281	0.298
C	—	0.160
D	0.016	0.020
E	0.004	—
F	TYP. 0.050	
G	0.09	0.105
H	0.035	0.065
J	0.009	0.011

SYMBOL	22 PIN	
	MIN	MAX
K	0.14	0.170
L	0.290	0.310
M	0.265	0.275
N	0.020	0.050
O	0.555	0.565
P	TYP. 0.050	
Q	0.092	0.122
R	0.005	—
S	0.08	—