WAFERSCALE INTEGRATION, INC.

WS27C512F

ADVANCE INFORMATION

T-46-13-29

HIGH SPEED 64K × 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  - — 70 ns
- **Low Power Consumption**
  - — 75 mW During Power Down
  - — 325 mW Active Power
- **EPI Processing**
  - — Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **Bipolar Speeds**

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GENERAL DESCRIPTION

The WS27C512F is an extremely HIGH PERFORMANCE 512K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at speeds as fast as 70 ns Access Time.

Two major features of the WS27C512F are its Low Power and High Speed. While operating in a TTL environment it consumes only 72 mA while cycling at full speed. Additionally, the WS27C512F can be placed in a standby mode which drops operating current below 2 mA in a TTL environment and 200 µA in a CMOS environment.

The WS27C512F also have exceptional output drive capability. It can source 1 mA and sink 4 mA per output.

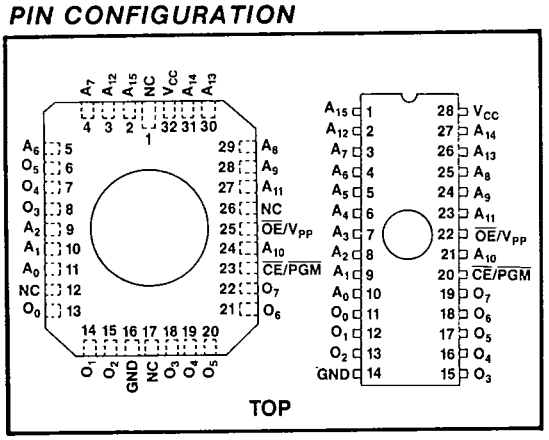
The WS27C512F is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

MODE SELECTION

PINS / MODE	$\overline{CE}$	$\overline{OE}$/V_{PP}	Vcc	OUTPUTS
Read	V_{IL}	V_{IL}	Vcc	DOUT
Output Disable	C	V_{IH}	Vcc	High Z
Standby	V_{IH}	X	Vcc	High Z
Program	V_{IL}	VPP	Vcc	DIN
Program Verify	V_{IL}	V_{IL}	Vcc	DOUT
Program Inhibit	V_{IH}	V_{IH}	Vcc	High Z
Signature*	V_{IL}	V_{IL}	Vcc	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, A_9 = 12V, A_0 is toggled, and all other address are at TTL low. A_0 = V_{IL} = MFGR 23H, A_0 = V_{IH} = DEVICE AAH.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS27C512F-70	WS27C512F-90
Address Access Time (Max)	70 ns	90 ns
Chip Select Time (Max)	70 ns	90 ns
Output Enable Time (Max)	25 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -65°C to +150°C
Voltage on any pin with
respect to GND.....-0.6V to +7V
VPP with respect to GND .....-0.6V to +13.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

Range	Temperature	V_{CC}
Comm'l.	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP}=V_{CC}$.

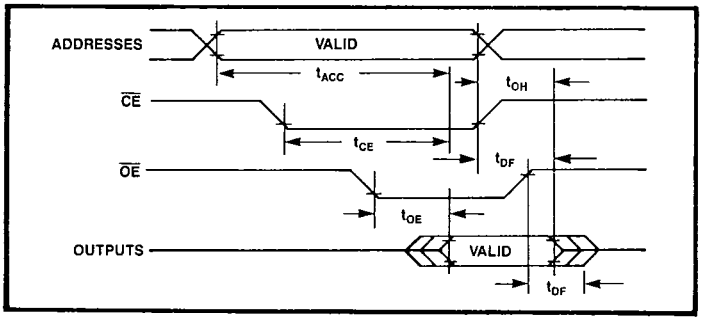
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 4 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1 mA		2.4		V
I_{SB1}	V_{CC} Standby Current CMOS	CE=V_{CC} ± 0.3V. Note 1			200	µA
I_{SB2}	V_{CC} Standby Current TTL	CE=V_{IH}. Note 2			2	mA
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l.		30	mA
			Military		40	mA
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l.		35	mA
			Military		45	mA
I_{PP}	V_{PP} Supply Current	$V_{PP}=V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC}-0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN}=5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT}=5.5V or Gnd.		−10	10	µA

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V. 3) A.C. Power component adds 3 mA/MHz.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.

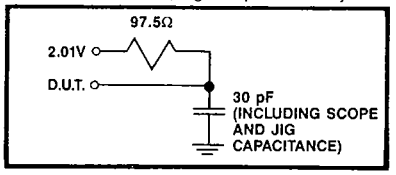
AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

PARAMETER	SYMBOL	WS27C512F-70		WS27C512F-90		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		70		90	ns
$\overline{CE}$ to Output Delay	t_{CE}		70		90	
$\overline{OE}$ to Output Delay	t_{OE}		25		30	
Output Disable to Output Float	t_{DF}		25		30	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: 0.4 and 2.4V

Reference Levels: 0.8 and 2.0V

T-46-13-29

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{CC} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{CC}		60	mA
V_{CC} Supply Current (Note 3)	I_{CC}		25	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 4 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −1 mA)	V_{OH}	2.4		V

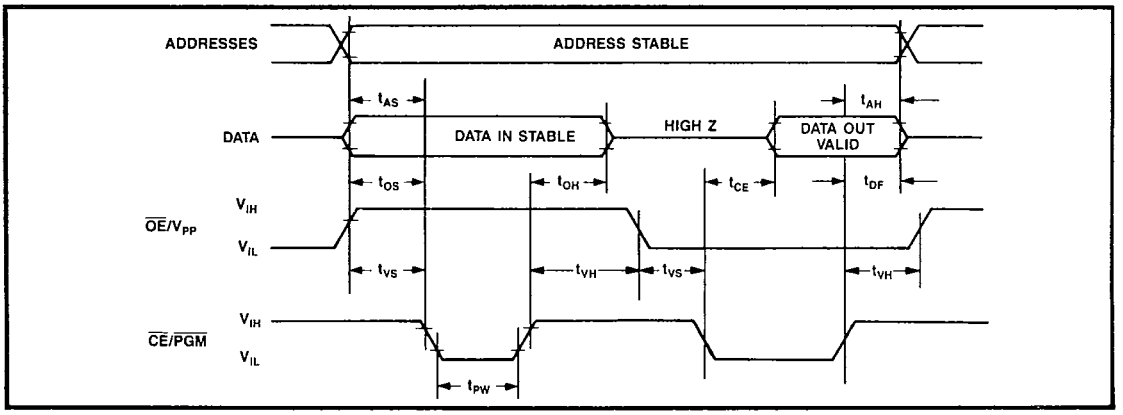
NOTES: 4) V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
5) V_{PP} must not be greater than 14 volts including overshoot. During CE = PGM = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
6) During power up the PGM pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µS
V_{PP} Hold Time	t_{VH}	2			µS
Data Setup Time	t_{OS}	2			µS
Address Hold Time	t_{AH}	0			µS
Data Hold Time	t_{OH}	2			µS
Chip Disable to Output Float Delay	t_{DF}	0		70	ns
Data Valid From Chip Enable	t_{CE}			70	ns
V_{PP} Setup Time	t_{VS}	2			µS
PGM Pulse Width	t_{PW}	1	35		ms

NOTES: 7. A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS27C512F has all 65,536×8 bits in the "1," or high state. "0's" are loaded into the WS27C512F through the procedure of programming.

The programming mode is entered when +13.5V is applied to the $\overline{OE}/V_{PP}$ pin and $\overline{CE}/\overline{PGM}$ is taken to V_{IL}. During Programming, $\overline{CE}/\overline{PGM}$ is kept at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS27C512F to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS27C512F. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000µ W/cm^2 for 20 minutes. The WS27C512F should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS27C512F and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS27C512F and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMERS

Data I/O Unipak 2B; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C512F-70C	70	32 Pad CLLCC	C2	Comm'l	Standard
WS27C512F-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS27C512F-90C	90	32 Pad CLLCC	C2	Comm'l	Standard
WS27C512F-90CM	90	32 pad CLLCC	C2	Military	Standard
WS27C512F-90CMB	90	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C512F-90D	90	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS27C512F-90DM	90	28 Pin CERDIP, 0.6"	D2	Military	Standard
WS27C512F-90DMB	90	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C