2142
1024 X 4 BIT STATIC RAM

	2142-2	2142-3	2142	2142L2	2142L3	2142L
Max. Access Time (ns)	200	300	450	200	300	450
Max. Power Dissipation (mw)	525	525	525	370	370	370

- **High Density 20 Pin Package**
- **Access Time Selections From 200-450ns**
- **Identical Cycle and Access Times**
- **Low Operating Power Dissipation .1mW/Bit Typical**
- **Single +5V Supply**
- **No Clock or Timing Strobe Required**
- **Completely Static Memory**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**

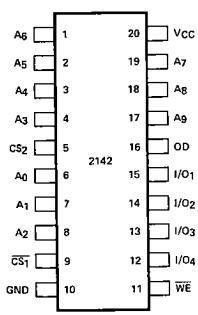
The Intel® 2142 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2142 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply.

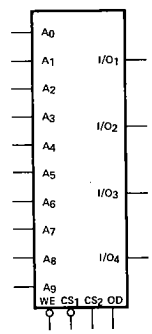
The 2142 is placed in a 20-pin package. Two Chip Selects ($\overline{CS}_1$ and CS_2) are provided for easy and flexible selection of individual packages when outputs are OR-tied. An Output Disable is included for direct control of the output buffers.

The 2142 is fabricated with Intel's N-channel Silicon-Gate technology — a technology providing excellent protection against contamination permitting the use of low cost plastic packaging.

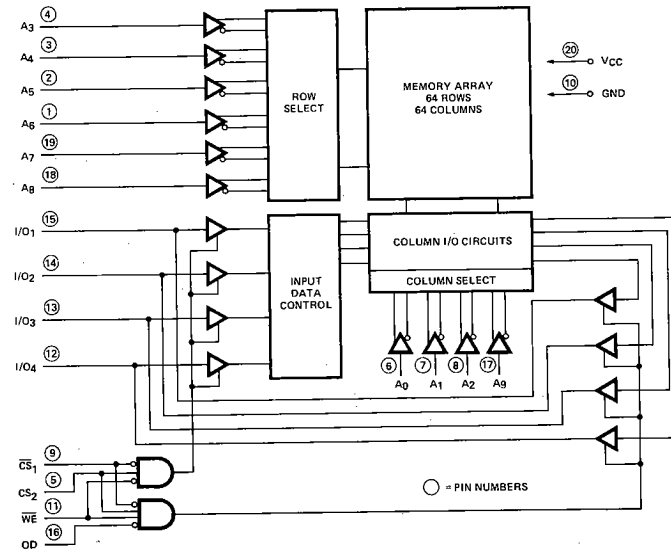
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESS INPUTS	OD	OUTPUT DISABLE
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}_1$, CS_2	CHIP SELECT	GND	GROUND
I/O_1–I/O_4	DATA INPUT/OUTPUT		

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to 80°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... -0.5V to +7V
Power Dissipation 1.0W
D.C. Output Current 10mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted.

SYMBOL	PARAMETER	2142-2, 2142-3, 2142 Min.	Typ.[1]	Max.	2142L2, 2142L3, 2142L Min.	Typ.[1]	Max.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All Input Pins)			10			10	µA	V_{IN} = 0 to 5.25V
$\|I_{LO}\|$	I/O Leakage Current			10			10	µA	$\overline{CS}$ = 2.4V, $V_{I/O}$ = 0.4V to V_{CC}
I_{CC1}	Power Supply Current		80	95			65	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 25°C
I_{CC2}	Power Supply Current			100			70	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
I_{OL}	Output Low Current	2.1	6.0		2.1	6.0		mA	V_{OL} = 0.4V
I_{OH}	Output High Current	-1.0	-1.4		-1.0	-1.4		mA	V_{OH} = 2.4V
I_{OS}[2]	Output Short Circuit Current			40			40	mA	$V_{I/O}$ = GND to V_{CC}

NOTE: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. Duration not to exceed 30 seconds.

CAPACITANCE

T_A = 25°C, f = 1.0 MHz

SYMBOL	TEST	MAX	UNIT	CONDITIONS
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels ..... 0.8 Volt to 2.4 Volt
Input Rise and Fall Times ..... 10 nsec
Input and Output Timing Levels ..... 1.5 Volts
Output Load ..... 1 TTL Gate and C_L = 100 pF

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise noted.

READ CYCLE [1]

SYMBOL	PARAMETER	2142-2, 2142L2 Min.	2142-2, 2142L2 Max.	2142-3, 2142L3 Min.	2142-3, 2142L3 Max.	2142, 2142L Min.	2142, 2142L Max.	UNIT
t_{RC}	Read Cycle Time	200		300		450		ns
t_A	Access Time		200		300		450	ns
t_{OD}	Output Enable to Output Valid		70		100		120	ns
t_{ODX}	Output Enable to Output Active	20		20		20		ns
t_{CO}	Chip Selection to Output Valid		70		100		120	ns
t_{CX}	Chip Selection to Output Active	20		20		20		ns
t_{OTD}	Output 3-state from Disable		60		80		100	ns
t_{OHA}	Output Hold from Address Change	50		50		50		ns

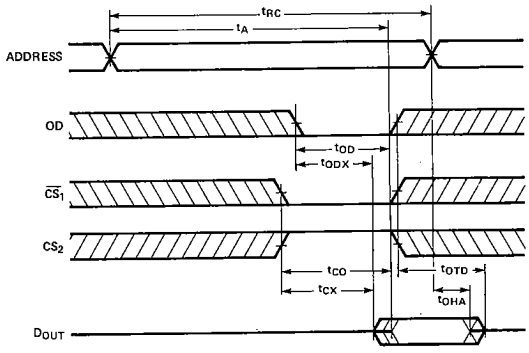
WRITE CYCLE [2]

SYMBOL	PARAMETER	2142-2, 2142L2 Min.	2142-2, 2142L2 Max.	2142-3, 2142L3 Min.	2142-3, 2142L3 Max.	2142, 2142L Min.	2142, 2142L Max.	UNIT
t_{WC}	Write Cycle Time	200		300		450		ns
t_W	Write Time	120		150		200		ns
t_{WR}	Write Release Time	0		0		0		ns
t_{OTD}	Output 3-state from Disable		60		80		100	ns
t_{DW}	Data to Write Time Overlap	120		150		200		ns
t_{DH}	Data Hold From Write Time	0		0		0		ns

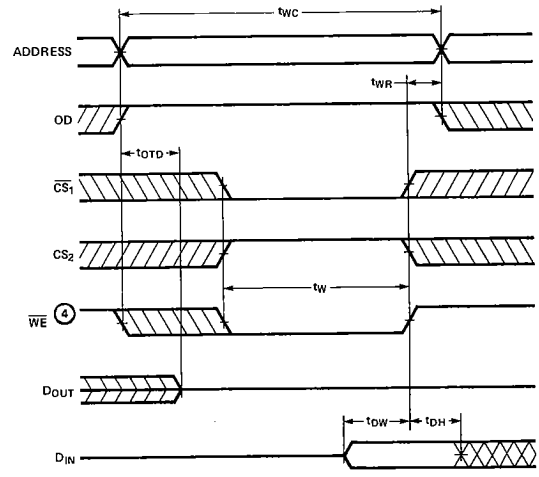
NOTES:
1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

WAVEFORMS

READ CYCLE ③



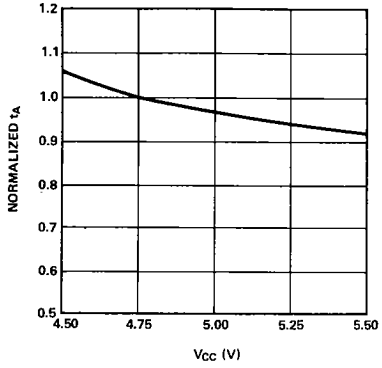
WRITE CYCLE



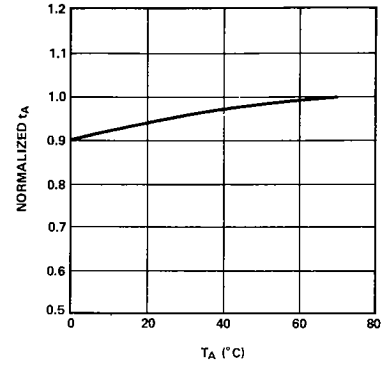
NOTES:
③ $\overline{WE}$ is high for a Read Cycle.
④ $\overline{WE}$ must be high during all address transitions.

TYPICAL D.C. AND A.C. CHARACTERISTICS

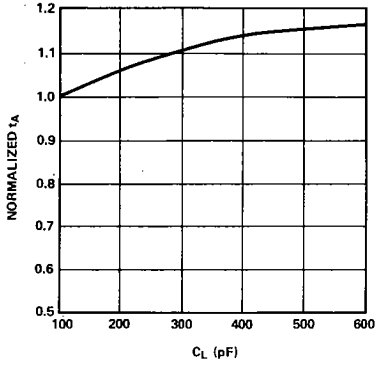
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



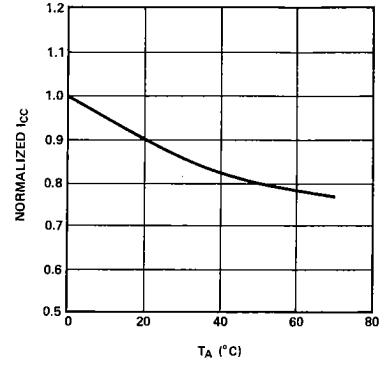
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



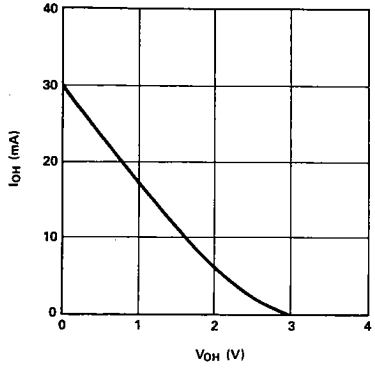
NORMALIZED ACCESS TIME VS. OUTPUT LOAD CAPACITANCE



NORMALIZED POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE