2,048 WORD × 8 BIT STATIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS PROCESS

TMM2015BP-90, TMM2015BP-12
TMM2015BP-10, TMM2015BP-15

DESCRIPTION

The TMM2015BP is a 16, 384 bits high speed and low power static random access memory organized as 2, 048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 90ns/100ns/120ns/150ns and maximum operating current of 50mA. When $\overline{CS}$ is a logical high, the device is placed in a low power standby mode in which maximum standby current is 5mA. Thus the TMM2015BP is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2015BP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

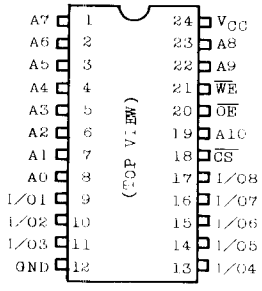
FEATURES

- Access Time and Current

Part Number \ Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2015BP-90	90ns	50mA	5mA
TMM2015BP-10	100ns	50mA	5mA
TMM2015BP-12	120ns	50mA	5mA
TMM2015BP-15	150ns	50mA	5mA

- High Density Assembly Capability:
  0.3 inch width package (24pin plastic DIP)
- Single 5V power Supply
- Fully Static Operation
- Power Down Feature: $\overline{CS}$
- Output Buffer Control: $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs Protected: All inputs have protection against static charge.

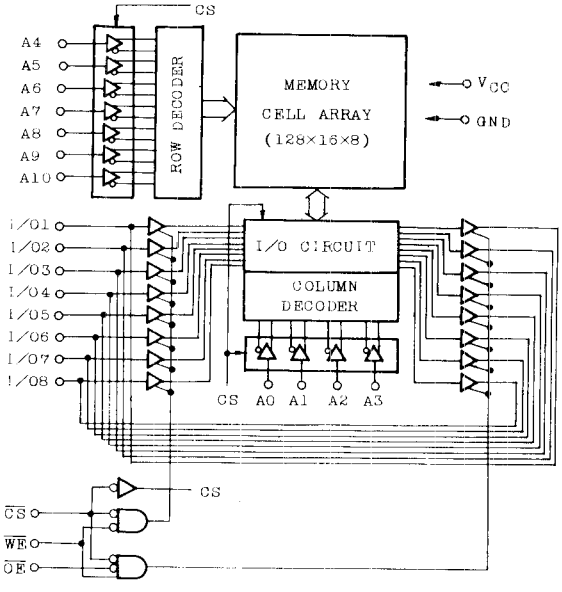
PIN CONNECTION



PIN NAMES

A_0~A_3	Column Address Inputs
A_4~A_{10}	Row Address Inputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
I/O_1~I/O_8	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5~7.0	V
V_{IN}, V_{OUT}	Input/Output Voltage	−0.5*~7.0	V
T_{OPR}	Operating Temperature	0~70	°C
T_{STG}	Storage Terperature	−55~150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation(Ta=70°C)	0.7	W

* −3.0V at Pulse width 50ns

D. C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Vovtage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.5**	—	0.8	V
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V

** −3.0V at Pulse width 50ns

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V~5.5V	−10	—	10	μA
V_{OH}	Output High Voltage	I_{OUT}=−1.0mA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OUT}=4.0mA	—	—	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V~5.5V	−10	—	10	μA
I_{SBP}	Peak Power-on Current	$\overline{CS}$=V_{CC}, I_{OUT}=0mA	—	—	10	mA
I_{SB}	Standby Current	$\overline{CS}$=V_{IH}, I_{OUT}=0mA	—	—	5	mA
I_{CC}	Operating Current	$\overline{CS}$=V_{IL}, I_{OUT}=0mA	—	—	50	mA

CAPACITANCE*** (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{IN}=0V	10	pF

*** Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS (Ta = 0~70°C, V_{CC} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TMM2015BP-90		TMM2015BP-10		TMM2015BP-12		TMM2015BP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	90	—	100	—	120	—	150	—	ns
t_{ACC}	Address Access Time	—	90	—	100	—	120	—	150	
t_{CO}	Chip Select Access Time	—	90	—	100	—	120	—	150	
t_{OE}	Output Enable Time	—	35	—	35	—	50	—	55	
t_{OH}	Output Data Hold Time from Address Change	10	—	10	—	10	—	10	—	
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	15	—	15	—	15	—	15	—	
t_{CHZ}	$\overline{CS}$ to Output in High-Z	—	40	—	40	—	40	—	55	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	5	—	5	—	5	—	5	—	
t_{OHZ}	$\overline{OE}$ to Output in High-Z	—	35	—	35	—	35	—	50	
t_{PU}	Chip Selection to power Up Time	0	—	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	50	—	50	—	60	—	60	

Write Cycle

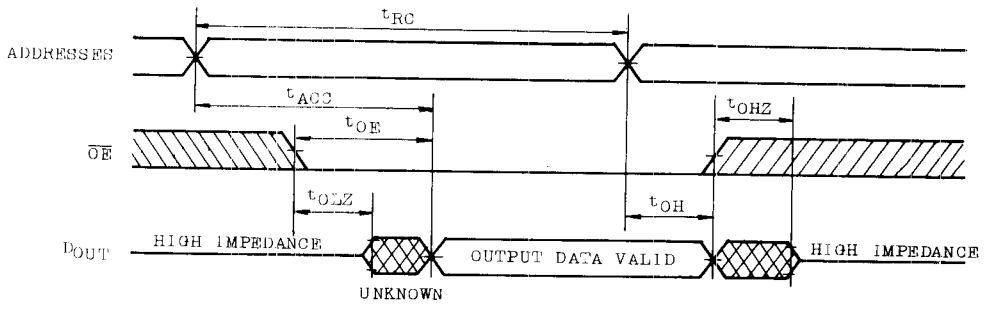
SYMBOL	PARAMETER	TMM2015BP-90		TMM2015BP-10		TMM2015BP-12		TMM2015BP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	90	—	100	—	120	—	150	—	ns
t_{CW}	Chip Selection to End of Write	60	—	70	—	85	—	100	—	
t_{AS}	Address Set Up Time	20	—	20	—	20	—	20	—	
t_{WP}	Write Pulse Width	55	—	65	—	80	—	100	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	
t_{DS}	Data Set Up Time	30	—	35	—	45	—	50	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	5	—	5	—	5	—	5	—	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	—	25	—	30	—	35	—	50	

A. C. TEST CONDITIONS

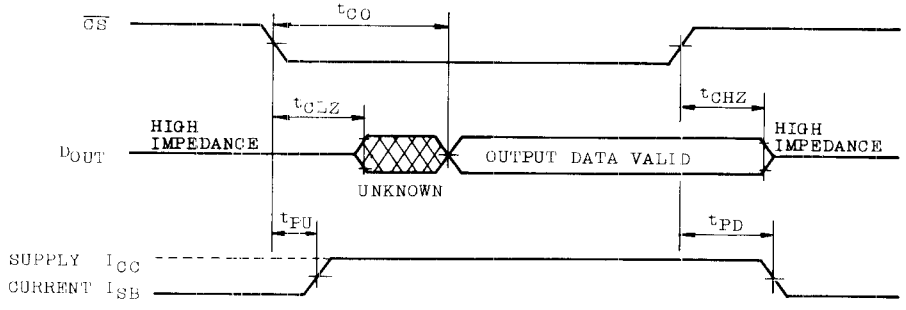
Input Pulse Levels	0~3.5V
Input Rise and Fall Time	10ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL Gate & C_L = 100pF

TIMING WAVEFORMS

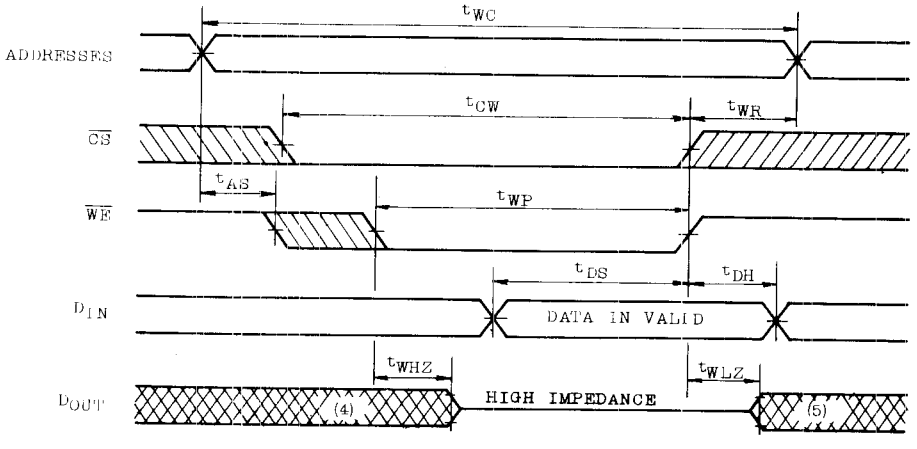
- (A) READ CYCLE [1] (1)



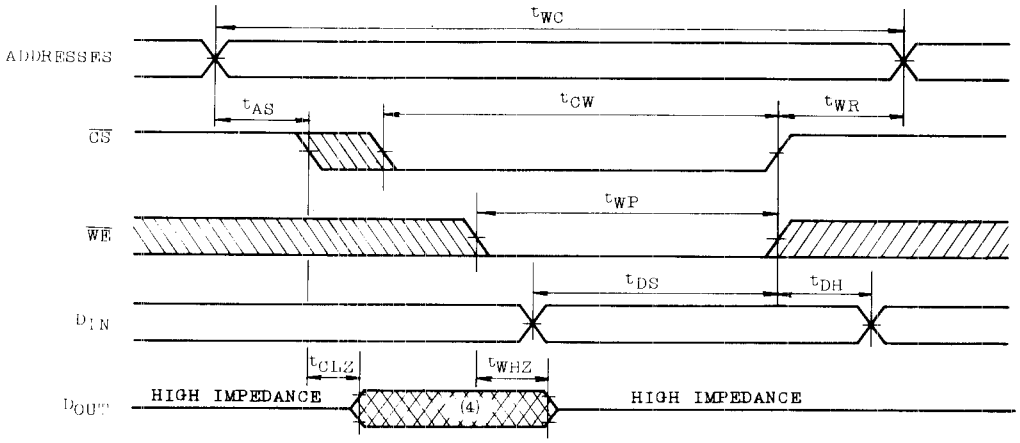
- (B) READ CYCLE [2] (1), (2)



- (C) WRITE CYCLE [1] (3)



- (D) WRITE CYCLE (2) (3)



NOTES:

(1) The $\overline{WE}$ is high for read cycle.
Device is continuously selected, $\overline{CS}$ =V_{IL} in read cycle (1)

(2) All addresses are valid prior to or simultaneously with $\overline{CS}$ transitions.

(3) A write occurs during the overlap of low $\overline{CS}$ and low $\overline{WE}$.
The t_{cw} is specified as the time from the chip selection to end of write in write cycle, and the t_{wp} is specified as the overlap time of low $\overline{CS}$ and low $\overline{WE}$.
$\overline{OE}$ is allowed to be low or high level in write cycle.
If the $\overline{OE}$ is high, the output buffers remain in a high impedance state in this period.

(4) If the $\overline{CS}$ low transition occurs simultaneously with or latter to the $\overline{WE}$ low transition, the output buffers remain in a high impedance state in this period.

(5) If the $\overline{CS}$ high transition occurs simultaneously with $\overline{WE}$ high transition, the output buffers remain in a high impedance state in this period.

These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) t_{CLZ}, t_{OLZ}, t_{WLZ} ····· Output Enable Time

(B) t_{CHZ}, t_{OHZ}, t_{WHZ} ····· Output Disable Time

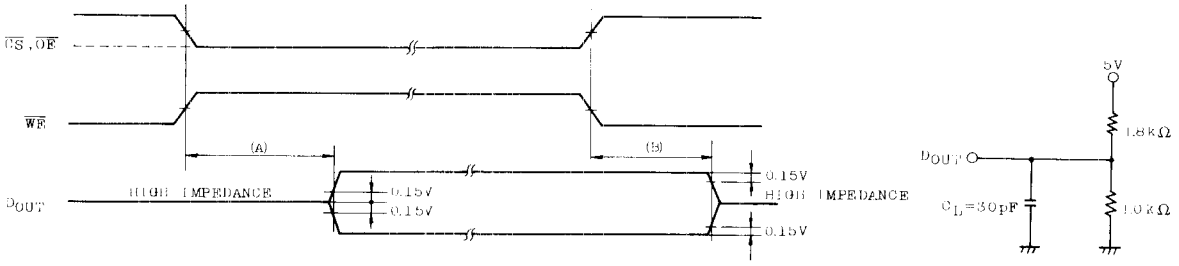
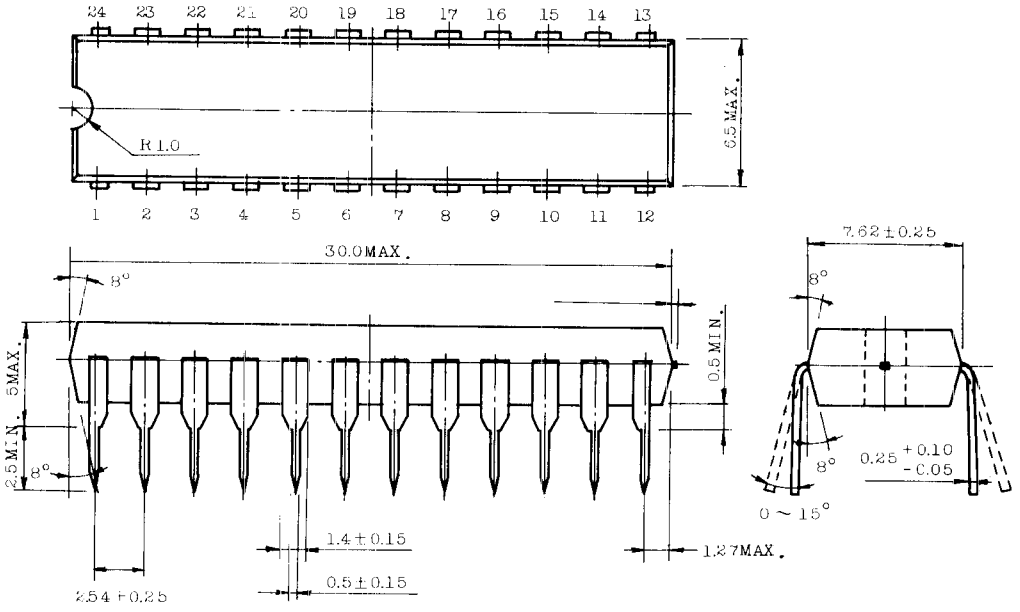


Fig. 1 Output load condition for enable disable time measurement.

OUTLINE DRAWINGS

Unit: mm



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.