INTERSIL

IM7141
4096 Bit (4096x1) NMOS Static RAM

FEATURES

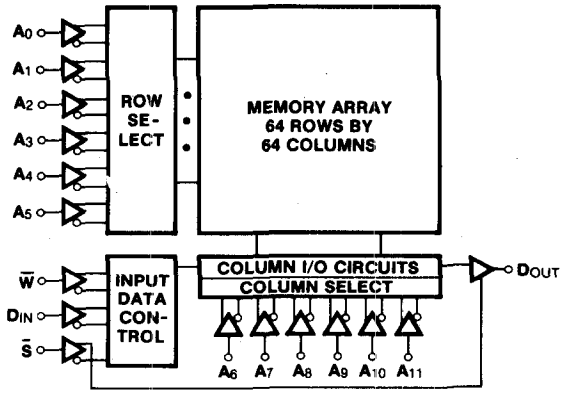
- Cycle Time Equal to Access Time
- Completely Static - No Clock Required
- Separate Data Input and Output
- TTL Compatible Inputs and Outputs
- 883A Class B Processing Available
- Single +5 Volt Power Supply
- High Density 18 Pin Package
- Maximum Access Time:
  -200ns (-2)
  -300ns (-3)
- Maximum Power Dissipation:
  – 256mW (L)
  – 370mW (Standard)

DESCRIPTION

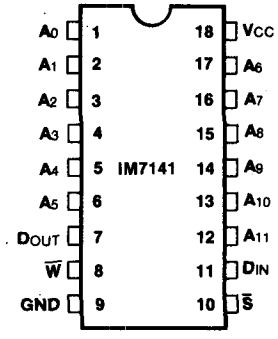
The IM7141 is a 4096-bit static Random Access Memory device organized 4096 words X 1. bit. The storage cells and decode and control circuitry are completely static; no clocks or refresh operations are required. Memory access occurs within the specified access time after all address inputs are stable. A Chip Select input is provided for simple memory array expansion.

The 7141 is assembled in a standard 18 pin DIP for maximum system packing density.

BLOCK DIAGRAM

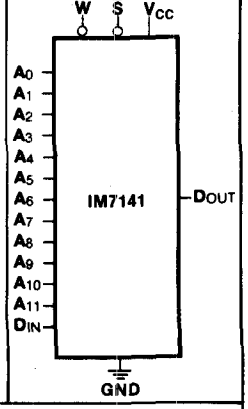


PIN CONFIGURATION



(outline dwgs JN, PN)

LOGIC SYMBOL



PIN NAMES

A_0-A_{11}	ADDRESS INPUTS
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
$\overline{W}$	WRITE ENABLE
$\overline{S}$	CHIP SELECT

ORDERING INFORMATION

POWER	ACCESS TIME			PACKAGE
	200ns	300ns	450ns	
265mW	IM7141L2CJN	IM7141L3CJN	IM7141LCJN	CERDIP
	IM7141L2CPN	IM7141L3CPN	IM7141LCPN	PLASTIC
370mW	IM7141-2CJN	IM7141-3CJN	IM7141CJN	CERDIP
	IM7141-2CPN	IM7141-3CPN	IM7141CPN	PLASTIC

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ABSOLUTE MAXIMUM RATINGS

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin to Ground ..... −0.5V to +7V
Power Dissipation 1W

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: T_A = 0°C to +70°C, V_{CC} = + 5 V ± 5 %

PARAMETER	SYMBOL	TEST CONDITIONS	7141L		7141		UNITS
			MIN	MAX	MIN	MAX	
Input Load Current (All Inputs)	I_{INLD}	V_{IN} = 0 to 5.25V		10		10	µA
Output Leakage Current	I_{OLK}	$\overline{S}$ = 2.4V, $V_{I/O}$ = 0.4V to V_{CC}		10		10	µA
Power Supply Current	I_{CC2}	VIN = 5.25, T_A = 0°C Output Open		45		65	mA
Power Supply Current	I_{CC1}	VIN = 5.25V, T_A = 0°C Output Open		50		70	mA
Input Low Voltage	V_{IL}		−0.5	0.8	−0.5	0.8	V
Input High Voltage	V_{IH}		2.0	V_{CC}	2.0	V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 3.2mA		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = −200µA	2.4	V_{CC}	2.4	V_{CC}	V

CAPACITANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNIT
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	5	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	5	pF

NOTE: These parameters are periodically sampled, not 100% tested.

DEVICE OPERATION

When $\overline{W}$ is high, the data input buffers are inhibited to prevent erroneous data from getting into the array. As long as $\overline{W}$ remains high, the data stored cannot be changed by the addresses, Chip select, or data I/O voltage levels and timing transitions. The block diagram also shows data storage cannot be changed by $\overline{W}$, the addresses, or the input data as long as $\overline{S}$ is high. Either $\overline{S}$ or $\overline{W}$ by itself, or in conjunction with the other, can prevent the extraneous writing due to signal transitions.

A READ occurs during the overlap of $\overline{S}$ low and $\overline{W}$ high. Data within the array can only be changed during a Write time, defined as the overlap of $\overline{S}$ low and $\overline{W}$ low. To prevent the loss of data, the addresses must be properly established during the entire Write time plus t_{wr}.

AC CHARACTERISTICS

TEST CONDITIONS: $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$
$t_r = t_f = 10ns$, $V_{IL} = 0.8V$, $V_{IH} = 2.0V$, Output Load = 1 TTL Gate and 100pF
Input and output timing reference level = 1.5V

READ CYCLE

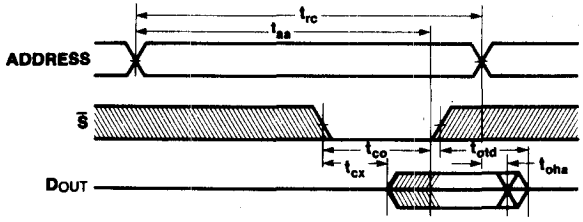
PARAMETER	SYMBOL	7141L2, 7141-2		7141L3, 7141-3		7141L, 7141		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle	t_{rc}	200		300		450		ns
Access Time	t_{aa}		200		300		450	
$\overline{S}$ to Output Valid	t_{co}		70		100		100	
$\overline{S}$ to Output Active	t_{cx}	0		0		0		
Output 3 State from Deselect	t_{otd}	0	60	0	80	0	100	
Output Hold from Address Change	t_{oha}	10		10		10		

WRITE CYCLE

PARAMETER	SYMBOL	7141L2, 7141-2		7141L3, 7141-3		7141L, 7141		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Write Time Cycle	t_{wc}	200		300		450		ns
Write Time	t_w	120		150		200		
Write Release Time	t_{wr}	0		0		0		
Output 3 State from Write	t_{otw}	0	60	0	80	0	100	
Data to Write Time Overlap	t_{dw}	120		150		200		
Data Hold from Write Time	t_{dh}	15		15		15		
Address Setup Time	t_{aw}	0		0		0		
$\overline{S}$ Select Pulse Width	t_{cw}	120		150		200		

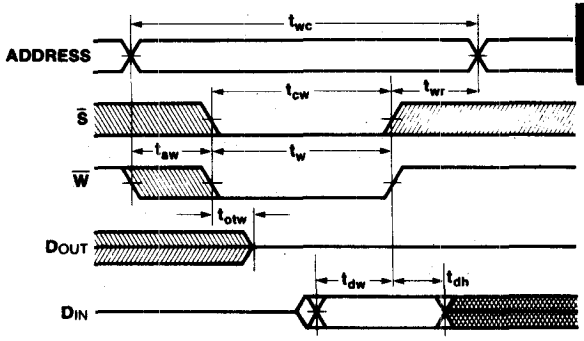
TIMING DIAGRAMS

READ CYCLE



Note: 1. $\overline{W}$ is high for a READ cycle.

WRITE CYCLE



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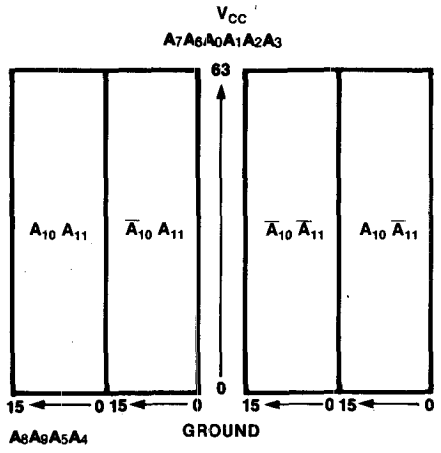
7141 BIT MAP DIAGRAM



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