t

Features

- Wide Power Supply Range, 3.0 V to 5.5 V
- Fast Read Access Time 200 ns
- Compatible with JEDEC Standard AT27C080
- Low Power 3.3-Volt CMOS Operation

20 μA max. Standby

29 mW max. Active at 5 MHz for $V_{CC} = 3.6 \text{ V}$ 165 mW max. Active at 5 MHz for $V_{CC} = 5.5 \text{ V}$

- Wide Selection of JEDEC Standard Packages
 - 32-Lead 600-mil PDIP and Cerdip
 - 32-Lead 450-mil SOIC (SOP)
 - 32-Lead TSOP
- High Reliability CMOS Technology 2000 V ESD Protection

200 mA Latchup Immunity

- Rapid Programming 50 μs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

Pin Configurations

Function

Outputs

Addresses

Chip Enable

Output Enable

Pin Name

A0-A19

00-07

OE/V_{PP}

CE

The AT27LV080 chip is a low power, low voltage 8,388,608 bit ultraviolet erasable and electrically programmable read only memory (EPROM) organized as 1 M x 8 bits. It requires only one supply in the range of 3.0 to 5.5 V in normal read mode operation, making it ideal for portable systems.

With a typical power draw of only 10 mW at 1 MHz and V_{CC} at 3.3 V, the AT27LV080 draws less than one-fifth the power of a standard 5-V EPROM. Standby mode supply current is typically less than 1 μ A at 3.3 V. (continued)

CDIP, PDIP, SOIC Top View

A19 C A16 C A15 C A7 C A6 C A3 C A3 C A1 C A1 C A1 C O1 C O2 C GND C	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	32 31 30 29 28 27 26 25 24 23 22 21 20 19 18	VCC A18 A17 A14 A13 A8 A9 A11 OE/VPP A10 CE O7 O6 O5 O4 O3

TSOP Top View Type 1

	.,,,,		
A11 10 10 1	32 04	È	OE/VPP
AB A9 3 2	31 30 20	B A10	CE
A14 A17 6 5	28 27	07 05	06
A18 4 7	26 27	P	O4
A19 A16 8 9	25	03	GND
A15 11	22 23	Þ	01
A7 A12 E 12 13	20 19	00 A1	A0
A5 ~ 4 15	18 17	A3	A2
A4 🗆 16 'S		H 70	



8 Megabit (1M x 8) Low Voltage UV Erasable CMOS EPROM

Preliminary



Description (Continued)

The AT27LV080 comes in a choice of industry standard JEDEC-approved packages, including: one-time programmable (OTP) plastic PDIP, SOIC (SOP), and TSOP, as well as windowed ceramic Cerdip. All devices feature two-line control ($\overline{\text{CE}}$, $\overline{\text{OE}}$) to give designers the flexibility to prevent bus contention.

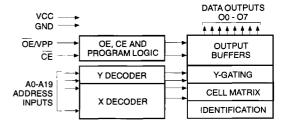
The AT27LV080 operating with V_{CC} at 3.0 V produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0 V.

Atmel's 27LV080 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50 $\mu s/byte$. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV080 programs identically as an AT27C080.

Erasure Characteristics

The entire memory array of the AT27LV080 is erased (all outputs read as VoH) after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using $12,000~\mu\text{W/cm}^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W-sec/cm². To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias40°C to +85°C
Storage Temperature65°C to +125°C
Voltage on Any Pin with Respect to Ground2.0 V to +7.0 V ⁽¹⁾
Voltage on A9 with Respect to Ground2.0 V to +14.0 V ⁽¹⁾
VPP Supply Voltage with Respect to Ground2.0 V to +14.0 V ⁽¹⁾
Integrated UV Erase Dose7258 W•sec/cm ²

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is $V_{\rm CC}$ + 0.75 V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	CE OE/V _{PP}		Ai	Vcc	Outputs
Read	VIL	VIL	Ai	Vcc	Dout
Output Disable	X	ViH	X ⁽¹⁾	Vcc	High Z
Standby	VIH	Х	Х	Vcc	High Z
Rapid Program ⁽²⁾	VIL	V _{PP}	Ai	Vcc ⁽²⁾	DIN
PGM Verify ⁽²⁾	VIL	VIL	Ai	Vcc ⁽²⁾	Dout
PGM Inhibit ⁽²⁾	ViH	Vpp	X	Vcc ⁽²⁾	High Z
Product Identification ^(2,4)	2,4) VIL VIL AC		A9=V _H ⁽³⁾ A0=V _{IH} or V _{IL} A1-A19=V _{IL}	D=VIH or VIL VCC ⁽²⁾	

Notes: 1. X can be V_{IL} or V_{IH}.

- Refer to Programming characteristics. Programming modes require V_{CC} ≥ 4.5 V.
- 3. $V_H = 12.0 \pm 0.5 \text{ V}$.

4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27LV080						
		-20	-25	-30				
Operating Temperature	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C				
(Case)	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C				
Vcc Power Supply		3.0 V to 5.5 V	3.0 V to 5.5 V	3.0 V to 5.5 V				

= Advance Information

D.C. and Operating Characteristics for Read Operation

(VCC = 3.0 V to 5.5 V unless otherwise specified)

Symbol	Parameter	Condi	tion		Min	Max	Units	
lu	Input Load Current	Vin = 0	V to Vcc			±1	μΑ	
ILO	Output Leakage Current	Vout =	= 0 V to Vcc			±5	μΑ	
"		1 (0	MOCY OF Mariana	Vcc = 3	.6 V	20	μА	
Isa	SB Vcc ⁽¹⁾ Standby Current —————	ISB1 (C	SMOS), $\overline{CE} = V_{CC} \pm 0.3 \text{ V}$	Vcc = 5	 ,5 V	100	μΑ	
136		TI) OF 0.04-1/ 0.51/	Vcc = 3	.6 V	100	μA		
	_	ISB2 (I	TL), $\overline{CE} = 2.0 \text{ to V}_{CC} + 0.5 \text{ V}$	Vcc = 5	.5 V	1	mA	
	Vcc Active Current	f = 5 MHz, lout		f = 5 MHz, IOUT = 0 mA,	Com.		8	mA
lcc		lcc ₁	$\overline{CE} = V_{IL}, V_{CC} = 3.6 \text{ V}$	Ind.		10	mA	
100			f = 5 MHz, lout = 0 mA	Com.	_	30	mA	
		ICC2	CE = VIL, VCC = 5.5 V	Ind.		40	mA	
VIL	Input Low Voltage	-		-	-0.6	0.8	V	
VIH	Input High Voltage				2.0	Vcc+0.5	V	
Vol	Output Law Valtage	loL = 2	.0 mA			.4	V	
VOL	Output Low Voltage	loL = 1	00 μΑ			.2	V	
Vall	Outnut High Valtage	Іон = -	2.0 mA		2.4		٧	
Vон	Output High Voltage	он = -	100 μ A	-	Vcc-0.2		٧	

Note: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

A.C. Characteristics for Read Operation

				AT27LV080						
				-20		-25		-30		
Symbol	Parameter_	Condition		Min	Max	Min	Max	Min	Max	Units
tACC (4) Address to Output Delay	Address to	CE = OE/V _{PP}	Com.		200		250		300	ns
	= VIL	Ind., Mil.		200		250		300	ns	
tcE (3)	CE to Output Delay	OE/VPP = VIL			200		250		300	ns
toE (3,4)	OE/V _{PP} to Output Delay	CE = VIL			70		100		150	ns
t _{DF} (2,5)	OE/V _{PP} or CE High to Output Float		-		50		50		50	ns
tон	Output Hold from Address, CE or OE/V _{PP} , whichever occurred first			0		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

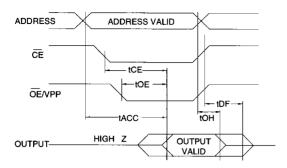
= Advance Information



3



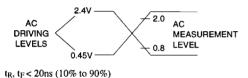
A.C. Waveforms for Read Operation (1)



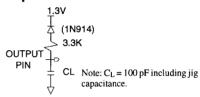
Notes:

- Timing measurement references are 0.8 V and 2.0 V. Input AC driving levels are 0.45 V and 2.4 V, unless otherwise specified.
- top is specified from OE /VPP or CE, whichever occurs first. Output float is defined as the point when data is no longer driven.
- 3. $\overline{\text{OE}}/\text{V}_{PP}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{\text{CE}}$ without impact on t_{CE}.
- 4. OE /V_{PP} may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
- 5. This parameter is only sampled and is not 100% tested

Input Test Waveforms and Measurement Levels



Output Test Load

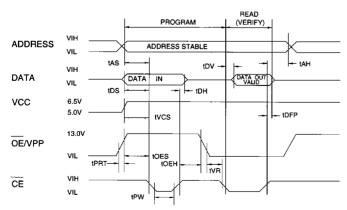


Pin Capacitance (f = 1 MHz T = 25° C)

	Тур	Max	Units	Conditions
CIN	4	8	pF	V _{IN} = 0 V
Соит	8	12	pF	Vout = 0 V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms (1)



Notes:

- 1. The Input Timing Reference is 0.8 V for V_{IL} and 2.0 V for V_{IH} .
- 2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

D.C. Programming Characteristics

 $T_A = 25 \pm 5^{\circ}C$, $V_{CC} = 6.5 \pm 0.25V$, $\overline{OE/V_{PP}} = 13.0 \pm 0.25V$

Sym-	- Test			Limits		
bol	Parameter	Conditions	Min	Max	Units	
iu	Input Load Current	VIN=VIL,VIH		10	μA	
VIL	Input Low Level	(All Inputs)	-0.6	8.0	٧	
VIH	Input High Level		2.0	V _{CC+} 1	٧	
Vol	Output Low Volt.	loL=2.1 mA		.45	٧	
Voн	Output High Volt.	Юн=-400 μА	2.4		٧	
lcc2	V _{CC} Supply Curren (Program and Veri			40	mA	
l _{PP2}	OE/V _{PP} Current	CE=V _{IL}		25	mA	
VID	A9 Product Identification Voltage		11.5	12.5	٧	

A.C. Programming Characteristics

 $T_A = 25 \pm 5^{\circ}C$, $V_{CC} = 6.5 \pm 0.25V$, $\overline{OE}/V_{PP} = 13.0 \pm 0.25V$

	0 ± 0 0, V(() = 0.0 ±				
Sym- bol	Test Conditions Parameter (see Note 1)		Lí r Min	nits Max I	Units
tas	Address Setup Time	2		μS	
toes	OE/Vpp Setup Time	e	2		μs
toeh	OE/V _{PP} Hold Time		2		μS
tos	Data Setup Time		2		μS
tan					μS
toH	Data Hold Time		2		μS
tDFP	CE High to Out- put Float Delay	(Note 2)	0	130	ns
tvcs	V _{CC} Setup Time		2		μS
tpw	CE Program Pulse Width	(Note 3)	47	53	μS
t _{DV}	Data Valid from CE	(Note 2)		1	μS
tvr	OE/V _{PP} Recovery T	ime	2		μS
tprt	OE/V _{PP} Pulse Rise Time During Progra		50		ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%)	20 ns
Input Pulse Levels 0.45 V to	2.4 V
Input Timing Reference Level 0.8 V to	2.0 V
Output Timing Reference Level 0.8 V to	2.0 V

Notes:

- V_{CC} must be applied simultaneously or before OE/V_{PP} and removed simultaneously or after OE/V_{PP}.
- This parameter is only sampled and is not 100% tested.
 Output Float is defined as the point where data is no longer driven see timing diagram.
- 3. Program Pulse width tolerance is $50 \,\mu\text{sec} \pm 5\%$.

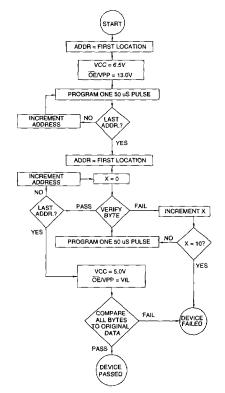
Atmel's 27LV080 Integrated Product Identification Code

		Pins							Hex	
Codes	A0	07	O6	O 5	04	О3	02	01	00	Data
Manufacturer	0	0	0	O.	1	1	1	_1_	0	1E
Device Type	1	1	0	0	0	1	0	1	0	8A

ote: 1. The AT27LV080 has the same Product Identification Code as the AT27C080. Both are programming compatible.

Rapid Programming Algorithm

A 50 μs \overline{CE} pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and \overline{OE}/V_{PP} is raised to 13.0 V. Each address is first programmed with one 50 μs \overline{CE} pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 50 μs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. \overline{OE}/V_{PP} is then lowered to V_{IL} and V_{CC} to 5.0 V. All bytes are read again and compared with the original data to determine if the device passes or fails.







Ordering Information

tacc (ns)	Icc (mA) Vcc = 3.6 V Active Standby		Ordering Code	Package	Operation Range
200	8	0.02	AT27LV080-20DC AT27LV080-20PC AT27LV080-20TC AT27LV080-20RC	32DW6 32P6 32T 32R	Commercial (0°C to 70°C)
200	10	0.02	AT27LV080-20DI AT27LV080-20PI AT27LV080-20TI AT27LV080-20RI	32DW6 32P6 32T 32R	Industrial (-40°C to 85°C)
250	8	0.02	AT27LV080-25DC AT27LV080-25PC AT27LV080-25TC AT27LV080-25RC	32DW6 32P6 32T 32R	Commercial (0°C to 70°C)
250	10	0.02	AT27LV080-25DI AT27LV080-25PI AT27LV080-25TI AT27LV080-25RI	32DW6 32P6 32T 32R	Industrial (-40°C to 85°C)
300	8	0.02	AT27LV080-30DC AT27LV080-30PC AT27LV080-30TC AT27LV080-30RC	32DW6 32P6 32T 32R	Commercial (0°C to 70°C)
300	10	0.02	AT27LV080-30DI AT27LV080-30PI AT27LV080-30TI AT27LV080-30RI	32DW6 32P6 32T 32R	Industrial (-40°C to 85°C)

Package Type				
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)			
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)			
32T	32 Lead, Plastic Thin Small Outline Package OTP (TSOP)			
32R	32 Lead, 0.450" Wide, Plastic Gull Wing Small Outline Package OTP (SOIC)			