

MB8416-20/MB8416-20L

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Cerdip	-65	150	°C
	Plastic	-40	125	
Temperature Under Bias	T _{bias}	-40	85	°C
Supply Voltage	V _{CC}	-0.5	8.0	V
Input Voltage	V _{IN}	-0.5	V _{CC} + 0.5	V
Input/Output Voltage	V _{I/O}	-0.5	V _{CC} + 0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = 0V)

Parameter	Symbol	MB8416			Unit	
		Min	Typ	Max		
Ambient Temperature	T _A	MB8416-20L	-40	—	+70	°C
		MB8416-20	-40	—	+85	
Supply Voltage	V _{CC}	4.5	5.0	5.5	V	
Input High Voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V	
Input Low Voltage	V _{IL}	-0.3	—	0.8	V	

CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit	Condition
Input Capacitance	C _{IN}	—	7	pF	V _{IN} = 0V
Input/Output Capacitance	C _{I/O}	—	10	pF	V _{I/O} = 0V

STATIC CHARACTERISTICS

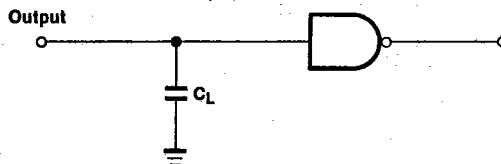
(Recommended Operating Conditions unless otherwise noted.)

Parameter	Condition	Symbol	Min	Max	Units
Standby Supply Current	E = V _{CC} - 0.2 to V _{CC} + 0.2V V _{IN} = -0.2V to V _{CC} + 0.2V	MB8416-20L	—	1	μA
		MB8416-20	—	10	
Standby Supply Current	E = V _{IH} V _{IN} = -0.2V to V _{CC} + 0.2V	I _{SB2}	—	2	mA
Active Supply Current	E = V _{IL} V _{IN} = V _{IL} or V _{IH} ; I _{OUT} = 0	I _{CC1}	—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% I _{OUT} = 0	I _{CC2}	—	60	mA
Input Leakage Current	V _{IN} = 0V to V _{CC}	I _{LI}	-1.0	1.0	μA
Output Leakage Current	V _{I/O} = 0V to V _{CC} E = V _{IH}	I _{LO}	-1.0	1.0	μA
Output High Voltage	I _{OUT} = -1.0 mA	V _{OH}	2.4	—	V
Output Low Voltage	I _{OUT} = 4.0 mA	V _{OL}	—	0.4	V

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AC TEST CONDITIONS

Input Pulse Levels: 0.6V to 2.4V
 Input Pulse Rise and Fall Times: 10 ns
 Input Timing Reference Level: 0.8V to 2.2V
 Output Timing Reference Level: 0.8V to 2.2V
 Output Load: 1 TTL Gate and
 $C_L = 100$ pF for all others.



DYNAMIC CHARACTERISTICS

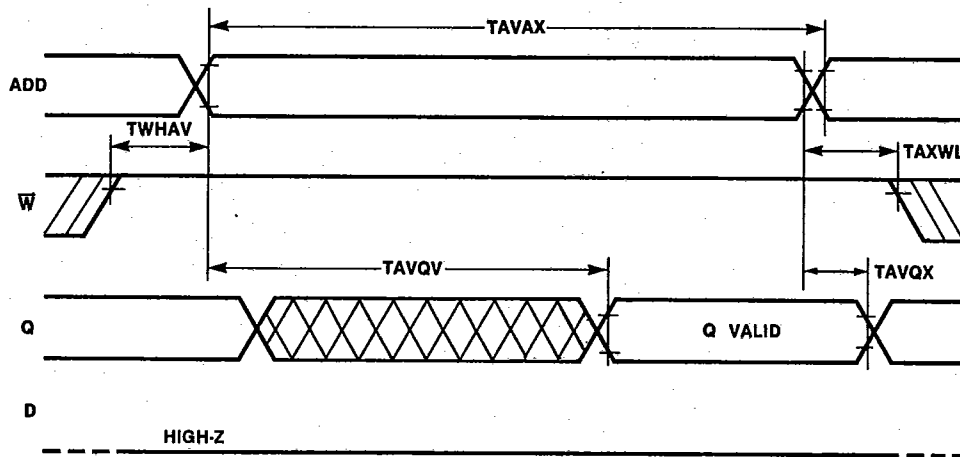
Parameter	Symbol	Min	Max	Unit
Read Cycle Time	TAVAX	200	—	ns
Write Cycle Time	TAVAX	200	—	ns
Address Access Time	TAVQV	—	200	ns
Chip Enable Access Time	TELQV	—	200	ns
Output Hold from Address Change	TAVQX	15	—	ns
Output Low Z from \bar{E}	TELQX	15	—	ns
Output High Z from \bar{E}	TEHQZ	—	60	ns
Output Low Z from \bar{G}	TGLQX	15	—	ns
Output High Z from \bar{G}	TGHQZ	—	60	ns
Output Low Z from \bar{W}	TWHQX	15	—	ns
Output High Z from \bar{W}	TWLQZ	—	60	ns
Output Enable to Output Valid	TGLQV	—	100	ns
Address Set Up Time	TAVEL, TAVWL	0	—	ns
Read Set Up Time	TWHEL, TWHAV	0	—	ns
Read Hold Time	TAXWL, TEHWL	0	—	ns
Write Set Up Time	TWLEL	0	—	ns
Write Hold Time	TEHWH	0	—	ns
Address Valid to End of Write	TAVWH	160	—	ns
Chip Enable to End of Write	TELEH	160	—	ns
Write Pulse Width	TWLWH	140	—	ns
Write Recovery Time	TWHAX, TEHAX	10	—	ns
Data Set Up Time	TDVEH, TDVWH	60	—	ns
Data Hold Time	TWHDX, TEHDX	0	—	ns

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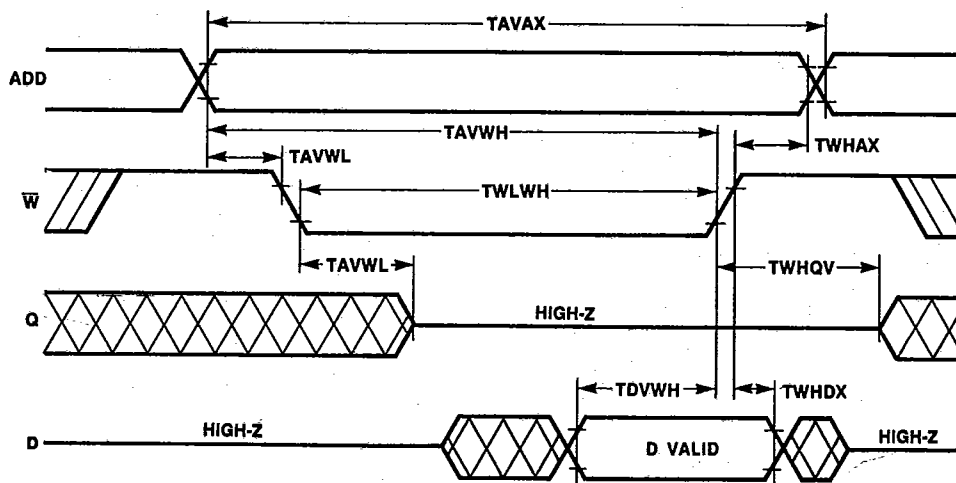
WAVEFORMS

MODE 1: \bar{W} Controlled: ($\bar{E} = \text{Low}, \bar{G} = \text{Low}$)

Read Cycle



Write Cycle

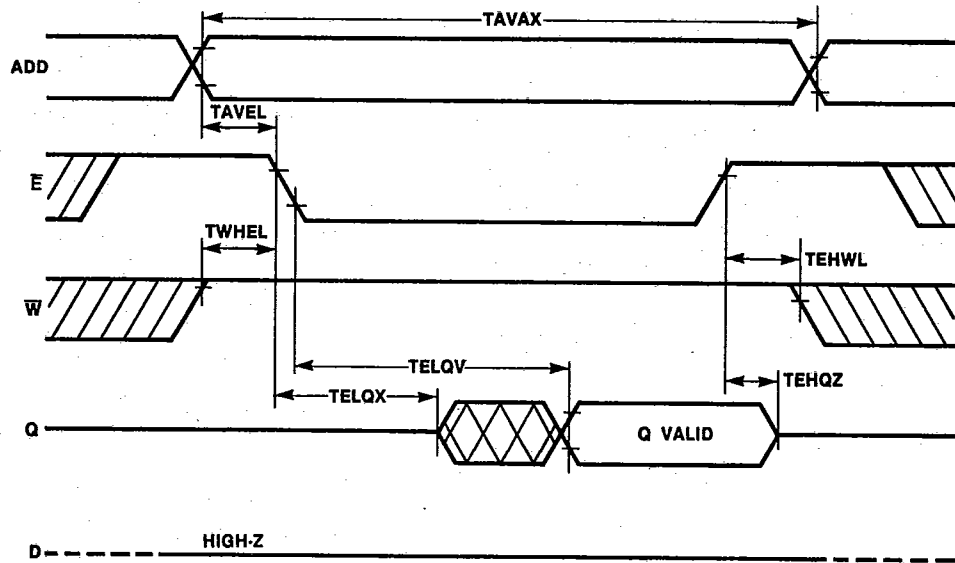


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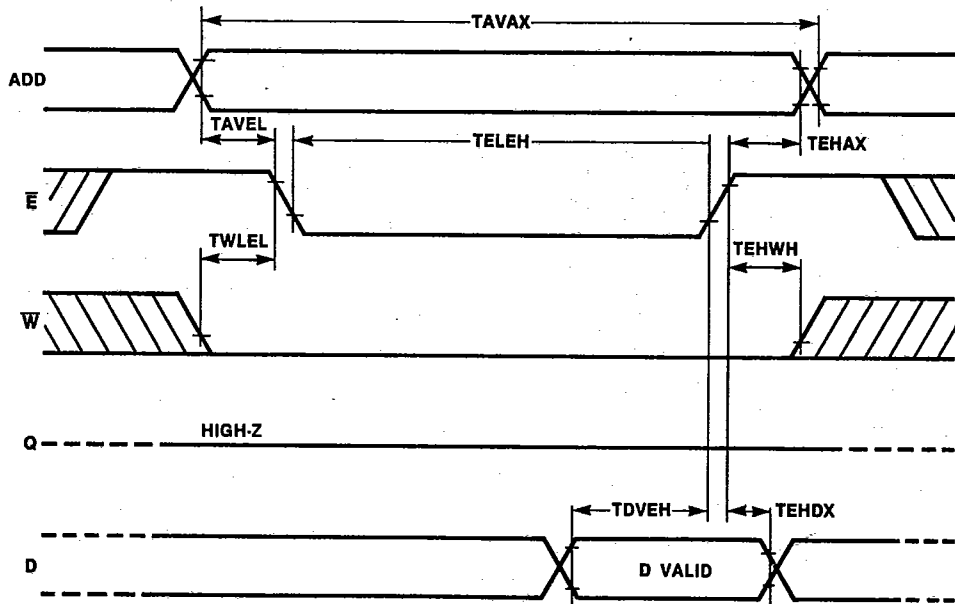
WAVEFORMS (Continued)

MODE 2: \bar{E} Controlled, ($\bar{G} = \text{Low}$)

Read Cycle



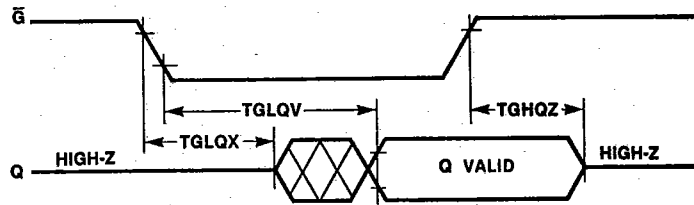
Write Cycle



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WAVEFORMS (Continued)

Enable/Disable \bar{G} Controlled; (\bar{E} = Low, \bar{W} = High)
Read Cycle



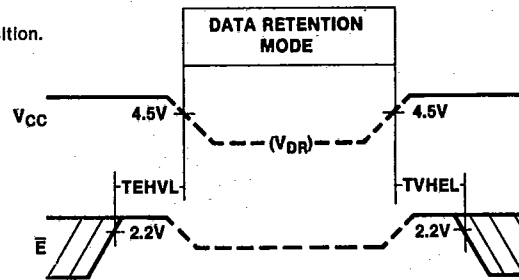
DYNAMIC CHARACTERISTICS

Data Retention Characteristics, NOTES 1, 2, 3 (Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	Min	Max	Unit	
Data Retention Supply Voltage	1	VDR	2.0	5.5	V	
Data Retention Supply Current	2	IDR	MB8416-20	—	10	μ A
			MB8416-20L	—	1	μ A
Data Retention Set Up Time	3	TEHVCL	0	—	ns	
Recovery Time	3	TVHEL	60	—	ns	

NOTES:

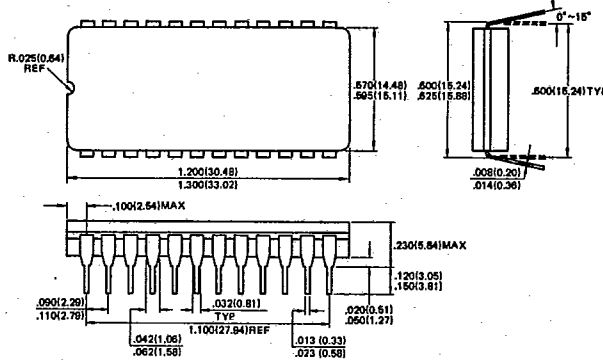
- 1. $E = 2.2V$ to $VDR + 0.3V$ when $VDR = 2.5V$ to $5.5V$
 $E = VDR \pm 0.3V$ when $VDR = 2.0$ to $2.5V$.
- 2. $V_{CC} = VDR = 2.0V$, $E = VDR \pm 0.2V$ $V_{IN} = -0.2V$ to $VDR + 0.2V$.
- 3. $V_L = 4.5V$ on the falling transition, $V_H = 4.5V$ on the rising transition.



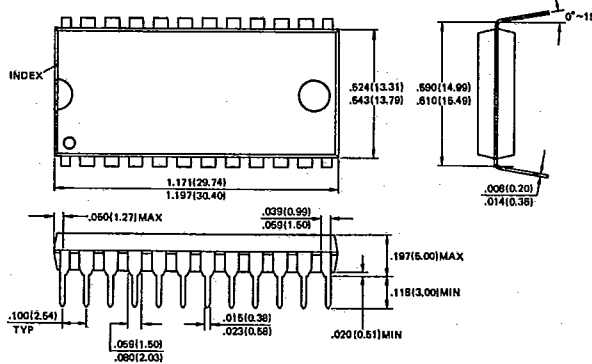
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PACKAGE DIMENSIONS Dimensions in Inches (millimeters)

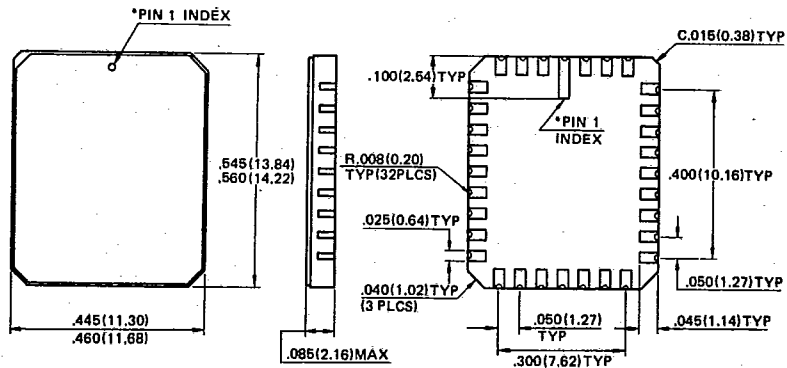
24-LEAD CERDIP DUAL IN-LINE PACKAGE
DIP-24C-C03



24-LEAD PLASTIC DUAL IN-LINE PACKAGE
DIP-24P-M02



32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
LCC-32-A02



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PACKAGE DIMENSIONS Dimensions in inches (millimeters) (Continued)

**24-LEAD PLASTIC FLAT PACKAGE
FPT-24P-M02**

