2148H
1024 x 4 BIT STATIC RAM

	2148H-2	2148H-3	2148H	2148HL-3	2148HL
Max. Access Time (ns)	45	55	70	55	70
Max. Active Current (mA)	180	180	180	125	125
Max. Standby Current (mA)	30	30	30	20	20

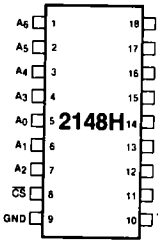
- **Automatic Power-Down**
- **Industry Standard 2114A and 2148 Pinout**
- **HMOS II Technology**
- **Functionally Compatible to the 2148**
- **Completely Static Memory — No Clock or Timing Strobe Required**
- **Equal Access and Cycle Times**
- **High Density 18-Pin Package**
- **Common Data Input and Output**
- **Three-State Output**
- **Single +5V Supply**
- **Fast Chip Select Access 2149H Available**

The Intel® 2148H is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits using HMOS II, a high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

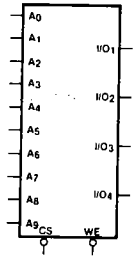
$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high — disabling the 2148H — the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are disabled. A non-power-down companion, the 2149H, is available to provide a fast chip select access time for speed critical applications.

The 2148H is assembled in an 18-pin package configured with the industry standard 1K x 4 pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data.

PIN CONFIGURATION



LOGIC SYMBOL



PIN NAMES

A_0-A_9	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
$\overline{CS}$	CHIP SELECT
I/O_1-I/O_4	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)
GND	GROUND

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	D_{IN}	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

Figure 1. Pin Configuration, Logic Symbol, Pin Names and Truth Table

BLOCK DIAGRAM

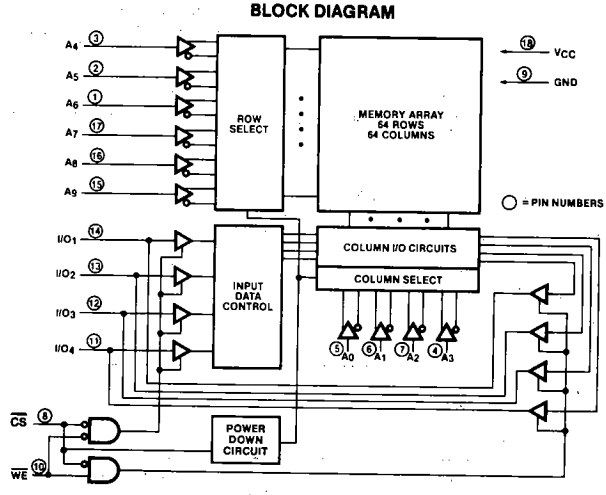


Figure 2. 2148H Block Diagram

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... −3.5V to +7V
D.C. Continuous Output Current ..... 20 mA
Power Dissipation 1.2W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS[1]

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$ unless otherwise noted.

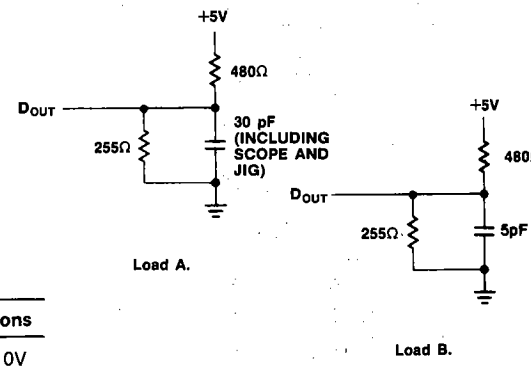
Symbol	Parameter	2148H-2/H-3/HL-3 Min.	Typ[2]	Max.	2148HL/HL-3 Min.	Typ[2]	Max.	Unit	Test Conditions
$\|I_{LI}\|$	Input Load Current (All Input Pins)		0.01	10		0.01	10	μA	V_{CC} = max, V_{IN} = GND to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		0.1	50		0.1	50	μA	$\overline{CS}$ = V_{IH}, V_{CC} = max, V_{OUT} = GND to 4.5V
I_{CC}	Operating Current		120	180		90	125	mA	V_{CC} = max, $\overline{CS}$ = V_{IL}, Outputs Open
I_{SB}	Standby Current		15	30		10	20	mA	V_{CC} = min to max, $\overline{CS}$ = V_{IH}
I_{PO}[3]	Peak Power-On Current		25	50		15	30	mA	V_{CC} = GND to V_{CC} min, $\overline{CS}$ = Lower of V_{CC} or V_{IH} min
V_{IL}	Input Low Voltage	−3.0		0.8	−3.0		0.8	V	
V_{IH}	Input High Voltage	2.1		6.0	2.1		6.0	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2.4			2.4			V	I_{OH} = −4.0 mA
I_{OS}	Output Short Circuit Current		±250	±275		±250	±275	mA	V_{OUT} = GND to V_{CC}

Notes:

1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute. Typical thermal resistance values of the package at maximum temperatures are:
   θ_{JA} (@ 400 f_{PM} air flow) = 40° C/W
   θ_{JA} (still air) = 70° C/W
   θ_{JC} = 25° C/W
2. Typical limits are at V_{CC} = 5V, T_A = +25°C, and Load A.
3. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during power-on. Otherwise, power-on current approaches I_{CC} active.

A.C. TEST CONDITIONS

Input Pulse Levels	GND to 3.0 Volts
Input Rise and Fall Times	5 nsec
Input and Output Timing Reference Levels	1.5 Volts
Output Load	See Load A.



CAPACITANCE [4]

$T_A = 25°C$, f = 1.0 MHz

Symbol	Parameter	Max.	Unit	Conditions
C_{IN}	Address/Control Capacitance	5	pF	V_{IN} = 0V
C_{IO}	Input/Output Capacitance	7	pF	V_{OUT} = 0V

Note 4. This parameter is sampled and not 100% tested.

A.C. CHARACTERISTICS

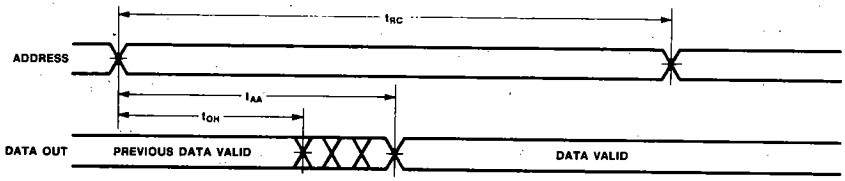
$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise noted.

READ CYCLE

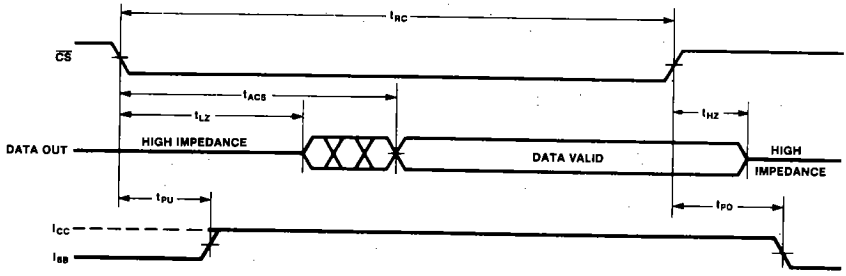
Symbol	Parameter	2148H-2 Min.	2148H-2 Max.	2148H-3/HL-3 Min.	2148H-3/HL-3 Max.	2148H/HL Min.	2148H/HL Max.	Unit	Test Conditions
t_{RC}	Read Cycle Time	45		55		70		ns	
t_{AA}	Address Access Time		45		55		70	ns	
t_{ACS1}	Chip Select Access Time		45		55	70		ns	Note 1
t_{ACS2}	Chip Select Access Time		55		65		80	ns	Note 2
t_{OH}	Output Hold from Address Change	5		5		5		ns	
t_{LZ}	Chip Selection Output in Low Z	20		20		20		ns	Note 6
t_{HZ}	Chip Deselection to Output in High Z	0	20	0	20	0	20	ns	Note 6
t_{PU}	Chip Selection to Power Up Time	0		0		0		ns	
t_{PD}	Chip Deselection to Power Down Time		30		30		30	ns	

WAVEFORMS

READ CYCLE NO. 1[3, 4]



READ CYCLE NO. 2[3, 5]



Notes:

1. Chip deselected for greater than 55 ns prior to $\overline{CS}$ transition low.
2. Chip deselected for a finite time that is less than 55 ns prior to $\overline{CS}$ transition low. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)
3. $\overline{WE}$ is high for Read Cycles.
4. Device is continuously selected, $\overline{CS} = V_{IL}$.
5. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
6. Transition is measured ±500mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested.

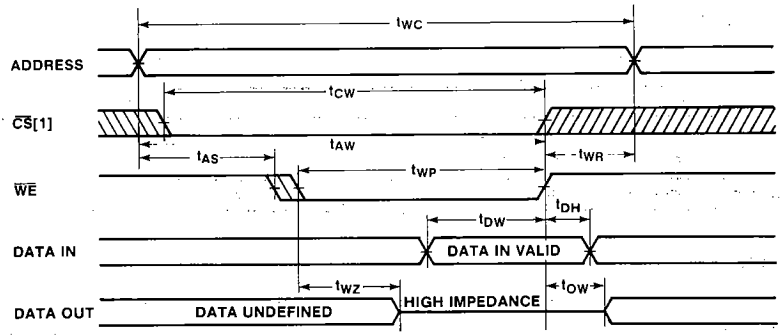
A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

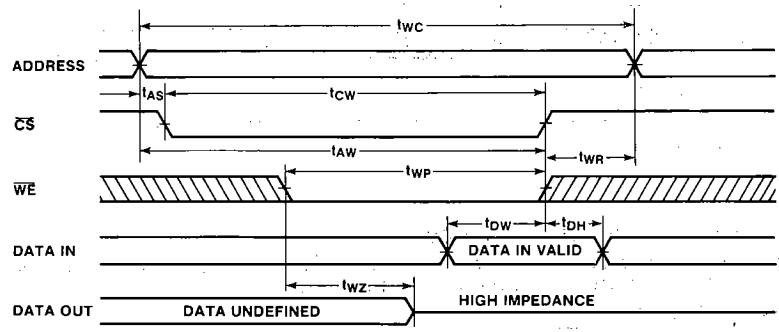
Symbol	Parameter	2148H-2 Min.	2148H-2 Max.	2148H-3/HL-3 Min.	2148H-3/HL-3 Max.	2148H/HL Min.	2148H/HL Max.	Unit	Test Conditions
t_{WC}	Write Cycle Time	45		55		70		ns	
t_{CW}	Chip Selection to End of Write	40		50		65		ns	
t_{AW}	Address Valid to End of Write	40		50		65		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{WP}	Write Pulse Width	35		40		50		ns	
t_{WR}	Write Recovery Time	5		5		5		ns	
t_{DW}	Data Valid to End of Write	20		20		25		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	15	0	20	0	25	ns	Note 2
t_{OW}	Output Active from End of Write	0		0		0		ns	Note 2

WAVEFORMS

WRITE CYCLE No. 1 ($\overline{WE}$ CONTROLLED)



WRITE CYCLE No. 2 ($\overline{CS}$ CONTROLLED)



Notes: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

2. Transition is measured ±500mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested.